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Design and Simulation of a Low Power 384-channel Actively Multiplexed Neural Interface

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Abstract

Brain computer interfaces (BCIs) provide clinical benefits including partial restoration of lost motor control, vision, speech, and hearing. A fundamental limitation of existing BCIs is their inability to span several areas (> cm^2) of the cortex with fine (<100 μm) resolution. One challenge of scaling neural interfaces is output wiring and connector sizes as each channel must be independently routed out of the brain. Time division multiplexing (TDM) overcomes this by enabling several channels to share the same output wire at the cost of added noise. This work leverages a 130-nm CMOS process and transfer printing to design and simulate a 384-channel actively multiplexed array, which minimizes noise by adding front end filtering and amplification to every electrode site (pixel). The pixels are 50 μm × 50 μm and enable recording of all 384 channels at 30 kHz with a gain of 22.3 dB, noise of 9.57 μV rms, bandwidth of 0.1 Hz – 10 kHz, while only consuming 0.63 μW/channel. This work can be applied broadly across neural interfaces to create high channel-count arrays and ultimately improve BCIs.

Keywords

neural interfaces; active electrode; time division multiplexing; brain computer interfaces

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I. Introduction

Brain computer interfaces (BCIs) are used clinically to restore partial motor function, speech, vision, and hearing to patients [1]–[10]. The neural populations targeted by BCIs can span mm^2 to cm^2, while the individual neurons that constitute these populations exist on the scale of 10s − 100s of μm. Ideally, a neural interface is able to span mm^2 to cm^2 with individual electrode resolution of 10 – 100 μm in order to capture targeted neural populations at a scale approaching the single neuron level [11]. However, existing neural interfaces are limited in the number of recording sites due to electrode wiring, resulting in a tradeoff between coverage and density. Active arrays address this limitation by adding a transistor at each electrode to enable time division multiplexing (TDM), which increases the number of channels without increasing the number of output wires [12]–[14]. A primary limitation of TDM, however, is the increased noise added to the signal due to thermal noise aliasing, which decreases the signal-to-noise ratio (SNR) and thus BCI performance [15].

An approach to overcome this increased noise is to add an amplifier and anti-aliasing filter before the multiplexing transistor, which improves SNR by increasing the signal amplitude and reducing aliased noise [16]. This is achieved by placing an amplifier and filters beneath or adjacent to the electrode, which limits the circuit area to 100 – 10,000 μm^2. This spatial constraint poses significant limitations on circuit complexity due to the area required to create low noise, band-passed output signals. Additionally, thermal damage to the brain may occur in devices that cause a > 2°C temperature rise to the surrounding tissue. The power density value for implanted circuits recommended by the Association for the Advancement of Medical Instrumentation (AAMI) was derived from experiments in muscle tissue, which demonstrated that a power density of ~40 mW/cm^2 caused a 2°C increase in local tissue temperature [17]. This power density corresponds to a power consumption of 1 μW for a 50 μm × 50 μm area.

This paper outlines the design and simulation of a low power intracortical electrode array designed in a 130-nm CMOS silicon-on-insulator (SOI) process. The array is composed of twelve shanks with 32 electrodes per shank for a total of 384 channels, all of which can be sampled at up to 30,000 samples per second (SPS) to accommodate both local field potential (LFP) and action potential (AP) recordings. Each electrode is equipped with a high pass filter (HPF), amplifier, low pass filter (LPF), buffer, and multiplexing transistor beneath the sensing electrode in a 50 μm × 50 μm “pixel” area. The present work describes the design of the pixel circuit, followed by the simulated performance of the pixel’s noise, gain, operating frequency, bandwidth, and power consumption.

II Array Overview & Pixel Architecture

A. Array Design and Fabrication Plan

The proposed design is shown in Figure 1A. Shanks are designed on a 10 mm^2 silicon die in a 130-nm, 1.2V, 6-metal layer SOI process. Each shank has 32 electrodes arranged in a single column with a 50 μm pitch and an overall shank size of 70 μm × 2.4 mm. Each shank has 8 I/O pads, 7 of which are shared across shanks. The remaining I/O pad is the single analog output shared by all 32 electrodes using a 32:1 in-pixel multiplexer

(MUX). Thus, the number of traces required per electrode is decreased by a factor of 32X as compared to passive electrodes. This enables electrode arrays to scale in channel-count beyond limitations imposed by individual electrode wiring.

Once fabricated from the CMOS foundry (Fig. 1a), shanks will be released from the bulk silicon using transfer printing [18] to selectively remove only the SOI layer, silicon device layer, and the 6 metal/insulation layers, which total to a thickness of 12 μm. The shanks will then be printed onto a polyimide substrate where electrodes and IO pads will be exposed followed by metal layer deposition to route the signals in/out of the shank. Finally, the shape of the shank will be defined by etching the polyimide substrate and the array will be released from the substrate (Fig. 1b).

Electrodes are located on the top metal layer, while electronics sit beneath the electrode. The rectangular electrode can be customized during post processing to range from 10 μm – 38 μm per side by adjusting the insulation layer.

B. Circuit Overview

An overview of the circuit is shown in Fig. 2. The signal enters the pixel through V_{in} while a reference signal enters through V_{ref}. The reference can be selected as an electrode on the tip of the shank or the circuit ground, which is electrically connected to the brain. The signals are then high pass filtered at 0.1 Hz to remove DC offsets and are differentially amplified by a gain of 22.3 dB (13X magnitude). Next, the output is low pass filtered with an adjustable −3dB point of 10 kHz – 30 kHz. The signal is then buffered and sampled using a MUX. The MUX control signal is generated by on-shank digital logic, which is controlled by two digital signals. A final buffer drives the single output per shank to the headstage where the signal is further buffered, amplified, and digitized using a 12-bit ADC. Lastly, the digital outputs travel to a computer for software de-MUXing and analysis.

C. High Pass Filter

A transistor level schematic of the pixel is shown in Fig. 3. A key challenge of the area-constrained design is the HPF due to the large values of resistance and capacitance required to achieve a −3dB cutoff of 0.1 Hz. Ideally, the capacitor would be as large as possible to lower noise and minimize any DC offsets that may arise from leakage current across the resistor. However, the capacitor with the lowest leakage current and highest capacitance per area available in this process node is the metal-insulator-metal (MIM) capacitor. Using MIM capacitors, the maximum capacitance achieved for two in-pixel capacitors is 1.2 pF per capacitor. Thus, a 1.3 TΩ value resistor is required to obtain a −3dB cutoff of 0.1 Hz. The 1.3 TΩ resistor was created using two PMOS devices biased by $V_{HPFreset}$ to be in the cutoff regime. The two PMOS devices form reverse-biased diodes with their resistance determined by their source-drain leakage current. The devices' width-to-length ratio (W/L) was optimized to produce the 1.3 TΩ resistor. However, this high resistance is difficult to accurately model using CMOS resistors. To overcome this challenge, $V_{HPFreset}$ can be used to tune the resistance post-fabrication by adjusting the source-drain leakage current to accommodate discrepancies between the simulated and actual value of the resistance.

The high resistance poses an additional challenge – any leakage current (the dominant source being the gate-source leakage of M_3 or M_5) produces a DC offset between the input into the differential amplifier and ground equal to the leakage current (I_{leak}) multiplied by the equivalent resistance of the reverse biased PMOS diodes (~1.3 TΩ). To overcome this issue, $V_{HPFreset}$ was periodically switched to turn the PMOS devices on to re-bias the node to ground. When the PMOS devices are on, their resistance drops to several hundred ohms and thus the node voltage resets rapidly. For additional design optimization post-fabrication an optional connection to the drain of M_2 and M_8 was added to tune the DC input value to the differential amplifiers.

D. Differential Amplifier

The differential amplifier was selected due to its high common mode rejection ratio (CMRR). The NMOS differential amplifier was selected due to sizing constraints, which prohibited a PMOS design with equivalent transconductance. During common mode operation, the gate voltages of M_3 and M_5 are equal and the bias current through M_9 (set by V_{ibias}) is equally divided amongst the two halves of the differential amplifier. However, a change in the gate voltage of M_3 forces a proportional and opposite current change in the drain of M_5, which in turn changes the voltage on the drain of M_5 and produces a gain equal to:

$$A_{dm} = g_{m5}(r_{o5} \parallel r_{o6}) \tag{4}$$

where g_{m5} is the transconductance of M_5 and r_{o5}/r_{o6} are the output resistances of M_5 and M_6, respectively. The parallel combination of the output resistances of M_5 and M_6 is equal to the inverse of the sum of the output transconductances ($g_o = 1/r_o$). The total differential mode gain is thus given by:

$$\mathrm{A_{dm}} = \frac{\mathrm{g}_{m5}}{\mathrm{g}_{05} + \mathrm{g}_{06}} \tag{5}$$

and can be simplified by $g_o = I_d\lambda$ as:

$$A_{\mathrm{dm}} = \frac{g_{m5}}{I_{\mathrm{d}}(\lambda_{\mathrm{m5}} + \lambda_{\mathrm{m6}})} \tag{6}$$

where λ_{m5} and λ_{m6} are the channel-length modulation parameters for M_5 and M_6, respectively.

To set the gain, the W/L ratios of all transistors in the differential amplifier were optimized, as well as the bias current. During device operation, the bias current is controlled by an on-shank 1:32 current mirror (not shown) and can be tuned by adjusting V_{ibias} indirectly. By adjusting the bias current, the bandwidth of the differential amplifier can be tuned.

E. Low Pass Filter

The LPF is critical for removing aliased thermal noise in multiplexed signals and was designed to range in −3 dB from 10 kHz – 30 kHz to enable neural spiking recording. The

LPF is formed by the output impedance of the differential amplifier and C_3. The −3 dB point of the filter is given by:

$$f_{-3dB} = \frac{1}{2\pi(r_{o5} \parallel r_{o6})C_3} \tag{7}$$

and can be simplified by plugging in the value of $(r_{05}||r_{06})$ derived in (8) as:

$$f_{-3dB} = \frac{I_d(\lambda_{m5} + \lambda_{m6})}{2\pi C_3} \tag{8}$$

Thus, the current can also be used to adjust the −3 dB point of the LPF. To ensure the range of operation was within the current limits imposed by power density constraints, C_3 was designed to be 7.5 pF using the largest capacitance per area capacitor available – the NMOS varactor. This device was not chosen for C_1 nor C_3 due the extreme sensitivity of the gate bias of M_3 and M_5 to leakage current. However, the output of the differential amplifier is less sensitive to leakage current. The varactor capacitance magnitude varies by less than 2% in the range of DC values of the output of the differential amplifier, which ensures low variation in −3dB cutoff frequency of the LPF.

F. Source Follower & Multiplexer

To create a low output impedance and preserve the −3 dB point of the LPF, the output of the differential amplifier is buffered by a source follower formed by M_{10} and a current source located on the shank (not shown) when the multiplexer (M_{11}) is closed. The digital signal that samples the pixel (V_{MUX}) is unique to every pixel and is generated by an on-shank shift register (Fig. 2). The output (V_{out}) is shared by all 32 pixels, as is the current source that completes the source follower circuit. The W/L values of M_{10} and M_{11} as well as the current value were optimized to maintain the gain of the source follower to be > 0.9 and the 99.9% settling time between channels to be ≤ 1 μs. This settling time value was chosen to ensure the 32 channels could be sampled at 30 kSPS per channel, which requires a 960 kHz sampling rate and a settling time ≤ 1.04 μs. A final buffer on the shank (shown in Fig. 2, shared by all channels) drives the output of the shank.

III Simulation Results

Final optimzation results are shown in Table 1 and were simulated using Cadence Virtuoso® and Spectre®. In all analyses, the W/L ratio values of transistors, current values, resistances, and capacitances were optimized to meet the design specifications. Table 1 contains the results of a mismatch and process corner Monte Carlo analysis with 2000 iterations, and a gaussian distribution of mismatch parameters of 4σ. The results are shown as an average ± standard deviation

A. AC analysis

The AC response with a differential amplifier bias of 0.5 μA is shown in Fig. 4. The mid-band gain is 22.3 ± 0.8 dB and was optimized to be as high as possible while keeping the noise low. A lower current produces a higher gain as shown in (6) but increases thermal

noise, which is the dominant noise source beyond 10 Hz. Additionally, if the current is too low, the bandwidth of the amplifier will decrease (8) and may be less than 10 kHz, which could filter out neural signals. Lastly, the low voltage process (1.2V) limits the headroom of M_6 on the output node of the differential amplifier. Thus, 22.3 dB was selected based on simulation results. This value provides enough gain to send the signal to the head stage for further gain and minimize the overall contribution of circuit noise between the shank and the head stage on SNR.

The HPF optimization resulted in a −3dB point of 0.13 ± 0.001 Hz, which is high enough to remove DC offsets that arise from the electrode tissue interface and low enough to accommodate LFP recordings that contain information down to single Hz values [19]. The HPF reset ($V_{HPFreset}$) eliminated the voltage drift in <10 μs and required switching after 1.57 s (0.63 Hz), which does not interfere with LFP recordings.

The value of C_3 (Fig. 3) was set at 7.5 pF resulting in a LPF −3 dB frequency of 10.6 ± 0.7 KHz at a bias current of 0.5 μA. The LPF −3dB point can be tuned by adjusting the bias current of the differential amplifier and can range from 10 – 30 kHz. The increased bandwidth may enable finer reconstruction of AP to improve spike sorting.

B. Noise and Power

Noise analysis was performed using a noise source on the input (V_{in}) while grounding V_{ref} (Fig. 3) and probing the output of the shank buffer (Fig. 2). Noise optimization resulted in an input referred full bandwidth (1 – 30 kHz) noise of 9.54 ± 0.3 μV rms, 5.49 ± 0.2 μV rms in the LFP band (1 – 300 Hz), and 4.06 ± 0.2 μV rms in the AP band (300 Hz – 6 kHz).

The source follower current optimization resulted in a bias of 1 μA to achieve a maximum 99.9% settling rate between channels of ≤ 1 μs. This current was shared between all channels. The overall power consumption of the pixel was 0.63 μW with the differential amplifier at a 0.5 μA bias (0.6 μW from the pixel, 0.03 μW from the shared source follower).

C. Source Follower and MUX

A critical function of the source follower is to drive the output load quickly while maintaining a gain close to its ideal value of 1. To sample 32 channels at 30 kSPS, the output value of the pixel must settle to 99.9% of its final value in ≤ 1 μs. A Monte Carlo analysis was performed to determine the maximum DC difference between differential amplifier outputs of adjacent pixels. The average value was found to be 347 mV ± 30 mV with an absolute range of 250 – 450 mV. Thus, a 200 mV DC offset between adjacent pixels was assumed in sampling simulations. The current and W/L ratio of the source follower and MUX transistors in the pixel were optimized to settle within 99.9% of their final value within ≤ 1 μs with a 0.95 gain using a current of 1 μA. Initially, this source follower was designed to drive the output load of the connector and headstage, but the large output load (estimated as R = 5 KΩ and C = 20 pF) required an area larger than available in the pixel. Thus, adding an additional source follower to handle the output load on the base of the shank in addition to the in-pixel source follower enabled ≤ 1 μs switching between channels.

IV. Discussion and Conclusions

This work details the design and simulation of an actively multiplexed intracortical electrode array with 384 recorded channels. The pixel design leverages TDM to enable scalable neural recording and decreases aliased noise by adding novel front-end filtering and amplification to the electrode site. The pixel achieves a 22.3 dB gain over a band of 0.1 Hz – 10 kHz with noise < 10 μV rms while consuming 0.63 μW/channel, which is less than the 1 μW/pixel area (40 mW/cm^2) recommended by the AAMI [17]. This value can be decreased using a sampling rate lower than 30 kSPS/channel.

The front-end pixel design outlined in this work has 5 – 10X lower power consumption per channel than TDM-based active arrays with in-pixel amplification [16], [22]. Additional channels can be added to shanks by extending the length of the shank by 6.5X to 10 mm, which is the length of the Neuropixel [23]. Unlike the Neuropixel, channels in this work can be actively multiplexed during recordings as opposed to a fixed selection before recording, which reduces the number of output wires by the multiplexing ratio (32). This scaling is enabled by the addition of in-pixel amplification and low pass filtering, which removes the TDM limitation of aliased noise.

Overall, this architecture paves the way for significantly higher channel count neural interfaces and can be adapted broadly across devices including intracortical and μECoG arrays.

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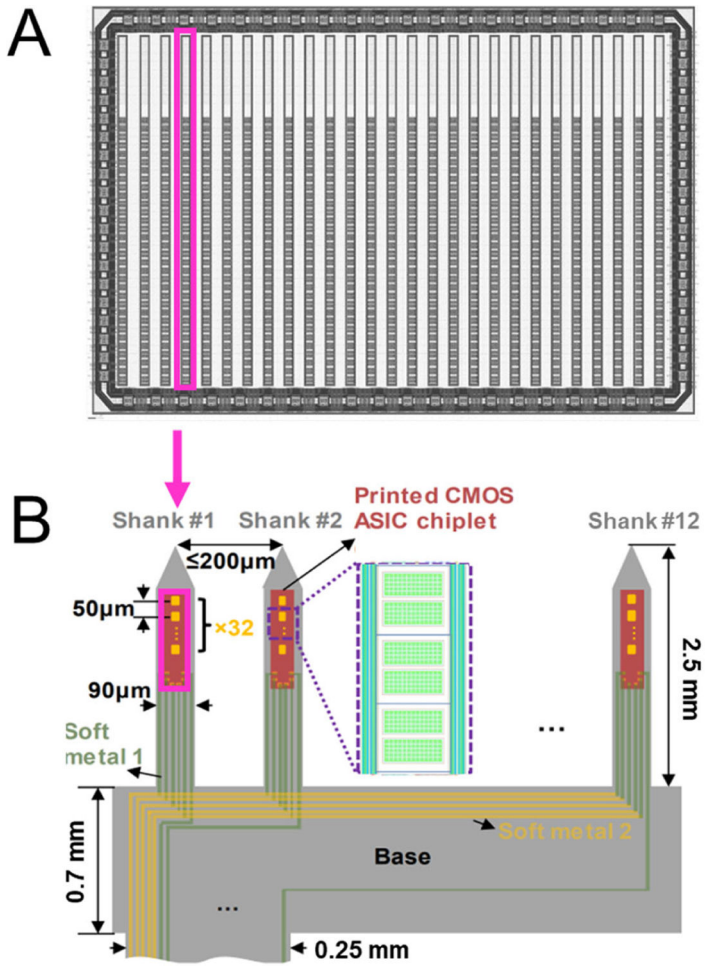

Fig. 1:

a) The top-level layout of the CMOS die is shown. 27 shanks are aligned in a row. A single shank to be transfer printed is highlighted in magenta. b) The final device is composed of 12 shanks transfer printed onto a polyimide substrate. The shank from the die shown in a) is highlighted. Three pixels are shown in the inlet on shank #2.

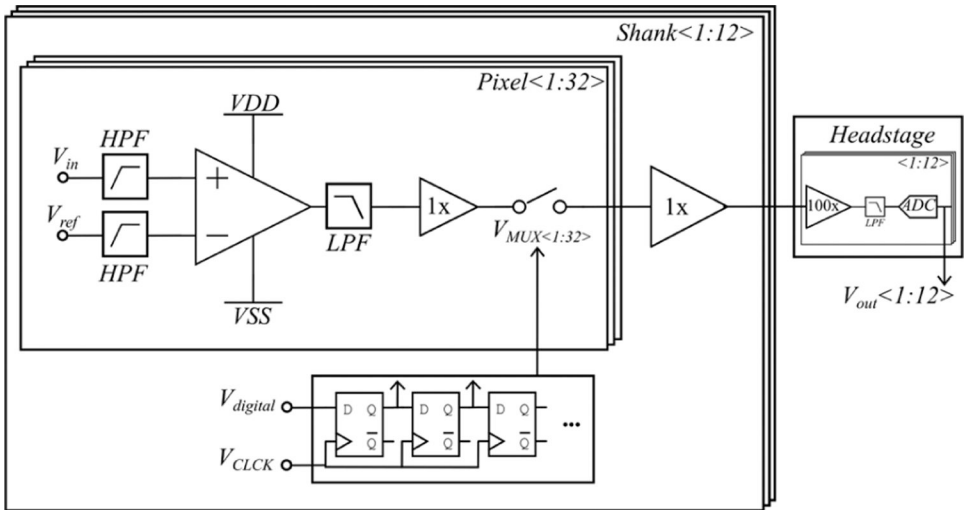

Fig. 2:

Circuit overview. In each of the 32 pixels, the signal and reference are high pass filtered before differential amplification followed by a low pass filter, buffer, and multiplexer. The signal is then buffered to create a single output/shank. Digital controls on the shank generate the MUX signal based on two digital inputs. The output of the shanks are then routed to a headstage where they undergo further buffering, amplification, filtering, and analogto-digital conversion.

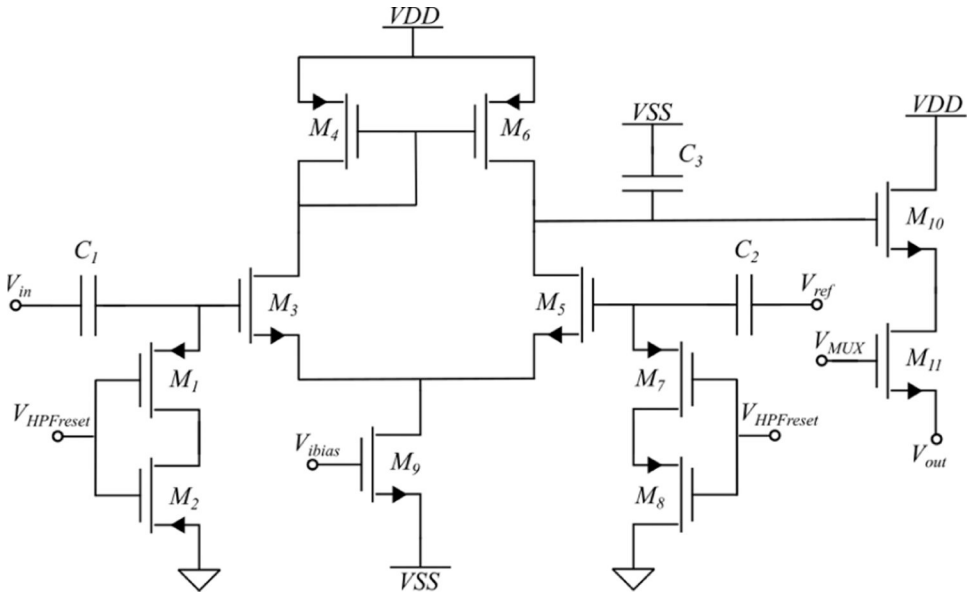

Fig. 3:

The transistor level pixel schematic is shown. The signal and reference enter the pixel and pass through a HPF before entering a differential amplifier. The output passes through a LPF and is buffered before multiplexing.

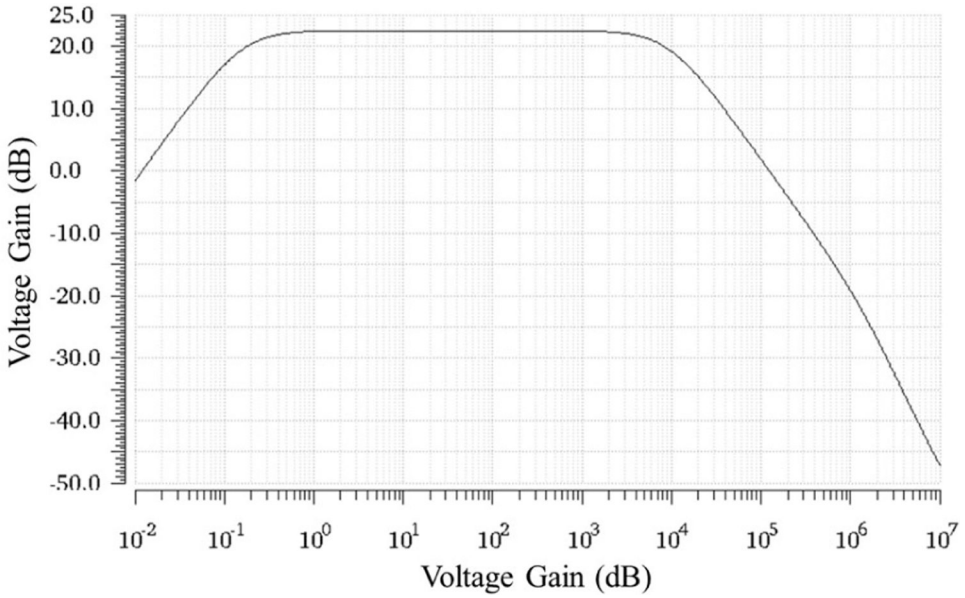

Fig. 4:

The AC response of the differential amplifier is shown using a current of 0.5 μA. The mid-band gain is 22.3 dB. The HPF −3dB frequency is 0.13 Hz while the LPF −3dB frequency is 10.6 kHz.

TABLE 1.

Circuit Performance

	Design	Simulation
Gain	> 20 dB	22.3 ± 0.8 dB
HPF − 3dB	0.1 Hz	0.13 ± 0.001 Hz
LPF − 3dB	20 kHz	10.6 ± 0.7 KHz
Noise (1 Hz− 30 kHz)	< 10 μV	9.54 ± 0.3 μV
Noise LFP (1 − 300 Hz)	-	5.49 ± 0.2 μV
Noise AP (300 Hz − 6 kHz)	-	4.06 ± 0.2 μV
Power consumption/ch	1 μW	0.63 ± 0.03 μW
Maximum MUX rate	1 MHz	1 MHz