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An AC-Coupled 1st-order Δ-ΔΣ Readout IC for Area-Efficient Neural Signal Acquisition

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Abstract

The current demand for high-channel-count neural-recording interfaces calls for more area- and power-efficient readout architectures that do not compromise other electrical performances. In this paper, we present a miniature 128-channel neural recording integrated circuit (NRIC) for the simultaneous acquisition of local field potentials (LFPs) and action potentials (APs), which can achieve a very good compromise between area, power, noise, input range and electrode DC offset cancellation. An AC-coupled 1^{st}-order digitally-intensive $\Delta - \Delta\Sigma$ architecture is proposed to achieve this compromise and to leverage the advantages of a highly-scaled technology node. A prototype NRIC, including 128 channels, a newly-proposed area-efficient bulk-regulated voltage reference, biasing circuits and a digital control, has been fabricated in 22-nm FDSOI CMOS and fully characterized. Our proposed architecture achieves a total area per channel of 0.005 mm^2, a total power per channel of 12.57 μW, and an input-referred noise of 7.7 ± 0.4 μV_{rms} in the AP band and 11.9 ± 1.1 μV_{rms} in the LFP band. A very good channel-to-channel uniformity is demonstrated by our measurements. The chip has been validated *in vivo*, demonstrating its capability to successfully record full-band neural signals.

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All animal procedures were approved by the Animal Ethics Committee of the KU Leuven, following the national guidelines on the use of laboratory animals (Belgian Royal Decree of 29 May 2013) and the European Union Directive for animal experiments (2010/63/EU).

Keywords

Neural recording; high-density; electrophysiology; analog-to-digital converter; brain-machine interface; continuous-time delta-sigma conversion

I. INTRODUCTION

FULLY-integrated and high-density neural recording probes are becoming vital neuroscience tools to perform massive recording of single-cell neural activity across different brain regions [1]-[5]. Thanks to the progress in neural recording devices, an exponential Moore's-Law-like growth in recording density has been observed in the last decades [6]. However, this growth is still insufficient to enable large brain coverage with implantable probes. To further scale the capabilities of existing CMOS neural probes, several design challenges need to be tackled. First, higher channel area and power efficiencies need to be achieved to enable higher-density recording. For this, system-level co-optimization is crucial to obtain the best trade-off with other important specifications such as input range and noise. Since the frequency bandwidth of the neural local filed potentials (LFPs, 0.5-1000 Hz) lies in the flicker noise band and the bandwidth of the neural action potentials (APs, 0.3-10 kHz) is affected by thermal noise, the power-area-noise trade-off is not easy to address. The second challenge comes from the electrode DC offset (EDO) present at the electrode-tissue interface. This offset can be as large as tens or even hundreds of mV, and it can vary over time due to the electrochemical changes and reactions happening during a chronic implant. Since this offset is much larger than the neural-signal amplitudes (APs: 10's of μV to ~1 mV; LFPs: 100's of μV to ~5 mV [7]), it can easily saturate the readout circuits. Finally, the recording electrodes may also be subject to artifacts caused by body movement or concurrent electrical stimulation. The amplitudes of such artifacts are very difficult to quantify because they depend on many factors such as the electrode size, impedance and location, the type of motion the animal is doing, the location of the reference electrode, the distance between the recording and stimulation electrodes, and the amplitude of the stimulation current. Thus, the input range of the readout channel should be large enough to accommodate the LFP signals plus a certain amount of motion/stimulation artifacts without saturation. The input range will then determine the type of experiments that can be supported by the readout system (e.g. freely-moving animal or concurrent micro/macro stimulation experiments).

To tackle the forementioned challenges, diverse circuit techniques have been proposed. The most common neural readout architecture consists of multiple amplification channels which are multiplexed into one analog-to-digital converter (ADC) [3], [5], [8]-[23]. The amplification stage is typically implemented as an AC-coupled instrumentation amplifier (IA) which can easily reject the EDO. The electrical performance and robustness of such architecture have been extensively validated in large-scale and long-term recordings [24], [25], but it has not achieved yet a good trade-off between the different performance metrics. For instance, a very power- and area-efficient AC-coupled readout channel has been recently reported in [13], but its input range is too limited to tolerate possible movement/stimulation artifacts. In order to reduce the channel area, a multiplexed AC-coupled readout has been

proposed in [26]. By multiplexing at the input of the channel, the equivalent area and power per electrode get significantly reduced by the multiplexing ratio. However, due to the lack of anti-aliasing filters before the multiplexer, the biological and electrode noise gets folded into the Nyquist band, thus increasing its contribution proportionally to the square root of the multiplexing ratio [4], [27]. Although this noise will dominate the total noise of the recording system, especially when using small and large-impedance electrodes, this contribution has not been properly included in the noise reported in [26]. Additionally, directly multiplexing at the electrode results in switching currents injected to/from the tissue, potentially posing safety issues in large-scale neural recording.

Direct-digitization topologies have been proposed as good alternatives to dramatically reduce the readout area and provide scalability in advanced technology nodes [2], [19], [28]-[44]. These architectures normally use ΔΣ or ΔΣ-like modulators since they can achieve good noise performance by combing oversampling and noise-shaping techniques. The low-noise front-end stage is then embedded in the mixed-signal loop of the modulator. Impressive area reductions have been achieved in some of these designs [2], [30], [37]. In [30], a 2^{nd}-order DC-coupled Δ – ΔΣ ADC achieves a large dynamic range, small area and low noise, while the EDO is tolerated by the large input range of the ADC. However, the required high-order modulation loop and complex decimation filter lead to high power consumption. This limitation has been tackled in [37] by introducing an EDO compensation loop. In this way, a simplified first-order modulation loop could be implemented. However, the noise contribution from the extra compensation loop is not negligible, resulting in high noise in the presence of large EDOs. Fig. 1 compares the channel power and noise performances versus area for recently reported neural readout chips. The IA+ADC architectures can be made more power and noise efficient, but the smallest areas are achieved with direct-digitization architectures.

In this paper, we propose an AC-coupled 1^{st}-order Δ – ΔΣ neural recording integrated circuit (NRIC). By implementing a novel combination of system and block-level topologies, we achieve a good compromise between power, area, noise, input range and EDO tolerance. In this design, a G_m – C integrator together with a current digital-to-analog converter (IDAC) are used to offer high-input impedance and enable AC-coupling for rail-to-rail EDO rejection. Delta-modulation around a ΔΣ core is used to extend the input range. The Δ-modulation loop is implemented in the digital domain, thus requiring no extra IDAC and benefitting from scaled technologies. To validate the proposed architecture and demonstrate its performance and scalability, a 128-channel prototype chip has been fabricated in a 22-nm FDSOI CMOS technology. The prototype chip has been used to develop a small and lightweight headstage (HS) that can enable saline and *in vivo* measurements with passive neural probes. This paper is an extension of our previous report [45]. The rest of the paper is organized as follows. The complete system-level design and the working principle of the proposed architecture is presented in Section II. Section III covers the detailed circuit implementation of the main building blocks. The measurement results are summarized in Section IV and conclusions are drawn in Section V.

II. System Design

A. High-level NRIC Architecture

The complete system architecture of the NRIC is shown in Fig. 2. It consists of 128 recording channels, a reference and bias generator, and a digital control. The latter includes a digital serializer, an I^2C interface, and a clock and control-signal generator to operate the channels. The NRIC operates with a supply voltage of 0.8 V and is clocked by a master clock of 48 MHz from which the internal clocks are derived.

Each recording channel is based on a hybrid discrete-time continuous-time (DT-CT) $\Delta - \Delta\Sigma$ modulator. Here, a $G_m - C$ based 1^{st}-order $\Delta\Sigma$ core is embedded into a Δ-modulation loop to provide multi-bit feedback from a one-bit quantizer. An up-down counter is used to form a digital integrator in the feedback loop and to achieve the Δ-modulation. The quantizer consists of only a comparator, thus eliminating the need for a power-hungry reference buffer. Finally, data weighted averaging (DWA) provides 1^{st}-order mismatch shaping for the elements in the IDAC. Compared with a single-bit $\Delta\Sigma$ modulator (e.g. [2]), the proposed $\Delta - \Delta\Sigma$ topology increases the dynamic range and reduces the quantization error [30],[21]. Furthermore, the multi-bit feedback IDAC reduces the sensitivity to clock jitter which negatively affects CT modulators [46]. The input range of the modulator is determined by the total feedback current and the G_m transconductance.

An AC-coupled stage is placed in front of the modulator to provide rail-to-rail EDO cancellation in a power- and area-efficient way. This enables the connection of the readout channel to any type of electrode, thus decoupling the circuit design constraints from the electrode performance. AC-coupling further reduces the area and power consumption of the whole modulator since only AC signals are digitized. The feedback integrator used for Δ-modulation, as well as the summation with the $\Delta\Sigma$ feedback, are implemented in the digital domain to fully benefit from the scaled technology. First-order noise-shaping is used to minimize the power and area of the digital decimation filter and eliminate the need for additional integrators. All the above characteristics enabled a significantly lower power and smaller area compared with our previous DC-coupled 2^{nd}-order design in [30], which has other important architectural differences such as the analog-domain delta-modulated feedback and the power-hungry 3^{rd}-order decimation filter.

B. Proposed Hybrid CT-DT $\Delta - \Delta\Sigma$ Front-End

Figure 3 shows the DT-equivalent model of the proposed $\Delta - \Delta\Sigma$ modulator. The feedback path employs a non-delaying integrator, thus corresponding to a cascade-of-resonators-feedback (CRFB) structure with zero coefficients for positive feedback [47]. Here, the DT equivalent of the CT integrator, formed by the G_m operational transconductance amplifier (OTA) and C_{INT}, is determined considering the following correspondence valid over a full clock-cycle:

$$\frac{1}{z-\alpha} \leftrightarrow \frac{\frac{S_k}{e^{s_k T_S}-1}}{s-s_k} = \frac{\frac{k_I}{T_s}}{s+\frac{1}{\tau_I}}, \tag{1}$$

where $T_s = 1 / f_S$, $\alpha = e^{s_k T_S}$, $s_k = -1 / \tau_I$, and $k_I = s_k T_s / (e^{s_k T_S} - 1)$. The parameter $\alpha \neq 1$ accounts for the leaky integration with time constant $\tau_I = R_{out,Gm} C_{INT}$, where $R_{out,Gm}$ is the output impedance of the OTA. Note that when this pole is at a much lower frequency compared with the sampling rate f_S, $e^{s_k T_S} \approx 1 + s_k T_S$, hence $k_I \approx 1$.

The signal transfer function (STF) and noise transfer function (NTF) of the modulator can be derived from (1) and are given by:

$$STF(z) = \frac{Y}{X} = \frac{z}{(z-1)} \frac{Y_\Delta}{X} = \frac{k_q b_2 z}{D(z)}, \tag{2}$$

$$NTF(z) = \frac{Y}{Q} = \frac{z}{(z-1)} \frac{Y_\Delta}{Q} = \frac{(z-\alpha)z}{D(z)}; \tag{3}$$

Where k_q is the quantizer gain and:

$$D(z) = (z-1)^2 + (k_q a_2 + k_q a_1 + 1 - \alpha)(z-1) + k_q a_1 . \tag{4}$$

The input-referred quantization error $\overline{v_{n,q}^2}$ can be determined using (3). In fact, the single-sided power spectral density (PSD) of the quantization error at the quantizer output is:

$$S_q(f) = \frac{2}{f_s} \frac{\Delta^2}{12}, \tag{5}$$

where $\Delta = 2$ is the quantization step of the single-bit quantizer. Therefore, when referred to the input of the modulator, the quantization error is shaped according to:

$$S_{q,in}(f) = \frac{2}{f_s} \frac{\Delta^2}{12} \left| \frac{NTF(f)}{STF(f)} \right|^2 . \tag{6}$$

Because of the high oversampling ratio (OSR = 160) chosen in this design, $f \ll f_S$ in the signal band, hence $z = e^{2\pi f / f_S} \approx 1 + \frac{j2\pi f}{f_s}$ and:

$$\begin{aligned} S_{q,in}(f) &= \frac{2}{f_s} \frac{\Delta^2}{12} \left| \frac{1-\alpha+j\frac{2\pi f}{f_s}}{k_q b_2} \right|^2 \\ &= \frac{2}{f_s} \frac{\Delta^2}{12} \left[\left(\frac{1-\alpha}{k_q b_2} \right)^2 + \left(\frac{2\pi f}{k_q b_2 f_s} \right)^2 \right]. \end{aligned} \tag{7}$$

The in-band noise power is then:

$$\begin{aligned}\overline{v_{n,q}^2} &= \int_0^{f_{BW}} S_{q,in}(f)\,df \\ &= \frac{\left(\frac{\Delta}{k_q}\right)^2}{12}\left[\left(\frac{1-\alpha}{b_2}\right)^2 OSR + \frac{1}{3}\left(\frac{\pi}{b_2}\right)^2 OSR^3\right] \\ &\approx \frac{\left(\frac{\Delta}{k_q}\right)^2}{12}\left[\frac{OSR}{(G_m R_{out,Gm})^2} + \frac{\pi^2 OSR^3}{3(G_m C_{INT} f_{Ss})^2}\right],\end{aligned} \tag{8}$$

where $OSR = (2f_{BW}) / f_s$. Note that Δ / k_q is the least-significant bit (LSB) of the quantizer as referred to its input. When τ_I is very large ($\tau_I \gg T_S$), we can approximate $\alpha = e^{-T_S / \tau_I} \approx 1 - T_S / \tau_I$. Thus, the noise shaping degradation due to the leaky integration amounts to the fraction:

$$\frac{3(1-\alpha)^2}{\pi^2 OSR^2} \approx \frac{3\left(\frac{T_s}{\tau_I}\right)^2}{\pi^2 OSR^2} = \frac{3}{(2\pi f_{BW}\tau_I)^2}, \tag{9}$$

which can be maintained negligible if the corner frequency of the integrator $f_{INT} = 1 / 2\pi\tau_I = 1 / (2\pi R_{out,Gm} C_{INT})$ is significantly smaller than $f_{BW} / \sqrt{3}$. To ease the design of the G_m stage, this constraint can be relaxed at the expense of noise degradation. In our case, we designed for $R_{out,Gm} > 50\,\text{M}\Omega$ MΩ while C_{INT} is 107 fF.

A high-level Simulink model of the channel modulator is employed to assess the maximum stable amplitude (MSA) and the stability of the modulator, estimating the quantizer gain k_q from simulations [47]:

$$k_q = \frac{\sum_i |\, v[i] \,|}{\sum_i v[i]^2}, \tag{10}$$

where $v[i]$ are the samples of quantizer input. Three different values of k_q are used to determine the pole-zero map and the STF and NTF (for an ideal integrator) as shown in Fig. 4. These values correspond to 3 different input amplitudes (0 V, 1 mV_{pp} and 20 mV_{pp}), indicating that k_q must be considered to ensure stability over different conditions.

Other non-idealities such as the bandwidth of the OTA (BW_{Gm}), the output impedances of the OTA ($R_{out,Gm}$) and IDAC ($R_{out,IDAC}$), the excessive loop delay (ELD), and the IDAC mismatch were included in a Verilog-AMS model to determine the requirements of the main analog sub-blocks of the channel (OTA, IDAC and comparator). Fig. 5 shows the high-level simulation results where the input-referred noise (V_{Qn}) and the input-referred noise plus distortion (V_{Qn+D}) are used to determine the design specifications. The effectiveness of the DWA was also assessed in these simulations. Based on the simulation results, the final specifications are set as: $BW_{Gm} > 10$ MHz, $R_{out,Gm} > 50$ MΩ, $R_{out,IDAC} > 100$ MΩ, $ELD < 5$ ns and IDAC mismatch < 30%, for which we can achieve a $V_{Qn} < 0.78\ \mu V_{rms}$ and a $V_{Qn+D} < 4.2\ \mu V_{rms}$. For the ELD, a value of 5 ns, corresponding to 2.48% of a clock cycle,

was found to not affect stability, as verified through both Verilog-AMS and transistor-level simulations.

To validate our Verilog-AMS model, we have performed circuit-level STF/NTF simulations using the final circuit specifications (Fig. 5 bottom-right). The STF is obtained by sweeping the input frequency and calculating the output magnitude of the modulator. The spectrum of the quantization noise floor is simulated, and the NTF is fitted in Matlab. As shown, the high-frequency part is close to the ideal NTF, while the lower frequency part is flat due to the non-idealities analyzed in Fig. 5. The detailed circuit implementation will be discussed in the following section.

III. Circuit Implementation

A. AC-Coupled Transconductance Stage

Figure 6 shows the schematic of the AC-coupled input stage. The input EDO gets filtered by the differential high-pass filter (HPF) formed by a pair of 5-pF MOM capacitors connected to thick-oxide PMOS pseudo-resistors. The cutoff frequency of the HPF is set to 0.1 Hz to enable the recording of both neural LFPs and APs, while limiting the noise contribution of the pseudo-resistor and the settling time of the channel. The area contribution of this HPF is negligible since the MOM capacitors are placed on top of the active circuits in the layout (i.e. no area overhead), and the pseudo-resistors are sized very small ($W / L = 0.2\,\mu m / 0.8\,\mu m$). Since the voltage across the pseudo-resistors is only the small input signal, only limited linearity degradation is expected.

The G_m stage is implemented with a resistively-degenerated OTA. A pair of flipped voltage followers [48] ($M_{1a,b}$-$M_{4a,b}$) drives the polysilicon resistor R_{TC}. The low-impedance terminals V_{Sa} and V_{Sb} allow the feedback currents from the IDAC (I_{FB+} and I_{FB-}) to be subtracted from the G_m's current ($I_{IN} = (V_{IP} - V_{IN}) / R_{TC}$). The resulting current is conveyed to the integrating capacitor, C_{INT} via unity-gain current mirrors ($M_{3a,b}$ and $M_{6a,b}$). Degeneration resistors R_S are employed to further minimize the noise from the bias transistors $M_{5a,b}$. The input transistors $M_{1a,b}$ are implemented with thick-oxide devices to minimize the gate leakage flowing through the pseudo-resistors, which may affect the input DC bias of the G_m stage, increase the HPF cut-off frequency and degrade the noise performance. Since the thick-oxide transistors in this scaled technology still exhibit a small amount of gate leakage, the size of $M_{1a,b}$ is chosen as a trade-off between area, noise, and high-pass corner frequency. To control the output common-mode (CM) voltage, a differential-difference-amplifier (DDA) based CM feedback (CMFB) circuit is utilized. It senses the output differential voltage and compares it with a reference voltage V_{CM} before feeding it back to the gate terminals of the NMOS transistors $M_7 - M_8 (V_{CMFB})$. Additionally, at frequencies beyond the bandwidth of the CMFB loop, there are CM ripples induced by the oversampling clock of the modulator. Hence, the integrating capacitor is split into two CM capacitors ($C_{INT,S1/2}$) and one differential-mode (DM) capacitor ($C_{INT,DM}$) where the mid-node V_{CMFB} of the CM capacitors provides high-frequency CMFB. This configuration helps reduce the clock-induced CM ripples. Our circuit-level simulations show that the G_m stage achieves a bandwidth of 10.35 MHz and an output impedance of 59.5 MΩ.

B. Current-Steering DAC

The IDAC in the feedback path includes 32 thermometric elements, each featuring a 2-level DAC. The circuit schematics of the IDAC and its unit element are shown in Fig. 7. Each unit cell is implemented by a small PMOS current source biased by V_{BP}. Thus, the entire 32-unit IDAC suffers from mismatch. This mismatch, together with the current glitches generated by the driving clock ($\Phi_{1,2}$), contribute to the overall modulator distortion. To limit this contribution, a latch driver (red box) is inserted to perfectly align the clocks, thereby reducing the current glitches. Additionally, DWA is applied to minimize the effect of the current-source mismatch. The simulated IDAC output impedance is 404 MΦ, with a unit mismatch factor of 6.3%.

C. Comparator

The dynamic comparator (Fig. 8(a)) employs an Elzakker's topology [49] to reduce the kickback noise. The use of a non-delaying integrator requires tighter timing (shorter delay) for the comparator decision and for the following digital block in the feedback loop. Therefore, the delay of the comparator, from the input clock Φ_{CLK} to the output D, needs to be controlled to minimize the ELD and avoid generating a wrong digital code for the IDAC.

The comparator delay varies with the input signal, with longer delays expected for smaller input signals (up to metastability). Since the input of the comparator in this architecture is pseudorandom (i.e., quantization noise), the delay of the comparator is also pseudo-random. This phenomenon can degrade the noise-shaping akin to clock jitter [50]. To minimize this effect, the output of the comparator, which triggers the acquisition in the digital feedback via *Rdy*, is delayed by a fixed amount of time t_d. A longer decision time is allowed through the *Done* signal (which indicates that the latch outputs Q_P and Q_N have settled to logic levels) to resolve sporadic input signals with very small amplitude. A timing diagram of the relevant signals is shown in Fig. 8(b). This scheme causes some residual delay variations, but the occurrences of these events are only a small percentage of all comparisons as confirmed by our Monte-Carlo simulations. Thus, the in-band quantization error does not get significantly degraded. Since the ELD is increased temporarily only during very few and sparse clock cycles, the average values of the modulator coefficients (and hence the loop-gain) are only slightly modified [51]. Therefore, the stability of the modulator is not compromised.

D. Digital Feedback and Decimation Filter

An up-down counter integrates the captured bitstream from the comparator output D into a 5-bit signed signal at each clock cycle (with the clock given by the *Rdy* signal). The *Rdy* signal becomes active-high shortly after the rising edge of Φ_{CLK} to indicate that the comparator decision is settled. With this behavior, the up-down counter is implemented as a non-delaying integrator. The adder sums the captured D and the output of the counter with minimum delay once the counter's output is settled. The final output is fed into the *DWA* to provide the mismatch shaping characteristic to the *IDAC*. The digital backend synthesis indicates a worst-case *ELD* of 2.9 ns in the digital feedback, which is sufficiently low for our design.

A 2-stage cascaded integrator-comb (CIC) decimation filter is inserted at the counter's output to suppress the out-of-band quantization noise and provide anti-aliasing filtering of the out-of-band signals and noise (e.g. circuit noise, electrode noise and background biological activity). This filter is configured with an input bit-width of 5 bits and an output bit-width of 14 bits, for an output sampling rate of 30 kS/s. Compared to the typical 1st-order analog low-pass filter employed in conventional channel architectures, this digital filter does not require bulky passives, is not susceptible to process-voltage-temperature variations and provides a steeper filtering characteristic.

F. Reference Generator

To reduce the complexity of the external acquisition system interfacing with our NRIC, the voltage and current references required to operate all the channels are integrated on chip. Therefore, the reference generator is also a critical block that contributes to the total area and power consumption. A bandgap reference (BGR) is a widely used architecture to generate a temperature insensitive reference voltage. It can achieve a good line sensitivity, but it is usually bulky and power hungry [52]. A much more compact voltage reference can be designed with the two-transistor (2T) structure proposed in [53]. It achieves a very small area and low power, but the line sensitivity of the output reference voltage is rather poor.

In this work, we propose a compact bulk-regulated voltage-reference circuit to overcome the abovementioned challenges (see Fig. 9 (a)). Transistors $M_1 - M_3$ form the reference generator, while the output reference voltage (V_{ref}) is further scaled to generate the 0.4-V CM voltage (V_{CM}) for all channels. Two trimming bits are implemented to tune the resistance R_1, enabling the compensation of possible process variations. The CM voltage is then used to generate eight $3 - \mu A$ reference currents for the eight channel groups present in the design. In order to facilitate the layout and optimize the drivability of the common bias voltages distributed to the G_m stages and IDACs, each channel group consists of 16 channels and includes an independent biasing generator.

The working principle of the reference generator is the leakage-current-based 2T architecture formed by the stacked transistors M_1 and M_2. Similar to [53], the reference voltage V_{ref} can be derived as:

$$V_{ref} = \underbrace{V_{TH1} - \frac{m_1}{m_2} V_{TH2}}_{CTAT} + \underbrace{m_1 ln \frac{\mu_2 W_2 L_1 (m_2 - 1)}{\mu_1 W_1 L_2 (m_1 - 1)} V_T}_{PTAT} \tag{11}$$

where V_T is the thermal voltage, $V_{TH1,2}$ is the threshold voltage, $\mu_{1,2}$ is the electron mobility, $m_{1,2}$ is the subthreshold slope factor, and $W_{1,2}$ and $L_{1,2}$ are the width and length of the two transistors. Eq. (11) can be divided into a complementary-to-absolute-temperature (CTAT) term and a proportional-to-absolute-temperature (PTAT) term. By properly sizing the $M_{1,2}$ parameters, V_{ref} can be made temperature insensitive. In our design, M_1 is a thick-oxide NMOS transistor, while M_2 is a flipped-well NMOS device (i.e. NMOS transistor in N-well).

The transistor M_3 is used here to regulate the drain-source voltage of M_2. This is done by connecting V_{ref} to the bulk of M_3, which is also a flipped-well device. In this way, the perturbations from the supply voltage to the drain of M_2 are reduced, and the line regulation of the output voltage improved [54]. Fig. 9 (b) shows the simulation comparison of the conventional 2-T reference generator and the proposed reference generator. The line regulation is improved from 0.0303% to 0.0004%.

The proposed 3-transistor (3T) reference generator consumes less than 0.1 nW at body temperature (37°C) and operates in deep weak inversion (aka 'super cut-off') region. The supply current flowing through all transistors is defined by M_2, which has negative bulk-source and zero gate-source potentials. In this bias condition, only a few tens of pA can flow through the transistors, which is negligible compared to the power consumption of a conventional BGR.

IV. Measurement Results

A prototype 128-channel NRIC was fabricated in a GlobalFoundries 22-nm FDSOI technology. It occupies a total active area of 0.66 mm^2, including the 128 readout channels, the reference generator, the biasing circuits, and the digital control. Fig. 10. shows the chip micrograph and the area breakdown per channel. The channel area is only 70 × 65 μm^2, which includes both the analog and digital (integrator, adder, DWA and decimation filter) parts of the channel. As shown in the breakdown, 61% of the total channel area is occupied by the analog part of the modulator, which includes the $G_m - C$ integrator, the comparator, the IDAC and the AC-coupled input stage. Deep-NWELL isolation is used to shield the sensitive analog part of the channel from the substrate noise injected by the digital circuits. The total chip area per channel is 0.0051 mm^2 when also considering the biasing circuits, the V/I reference generator and the digital control.

A. Electrical Characterization

To characterize the electrical performance of our NRIC, the dies were packaged on custom daughter printed-circuit boards and connected to a motherboard containing the required local components and connectors to operate the chip. The measurement setup is illustrated in Fig. 11. The boards are battery-powered, and a Stanford Research DS360 function generator is used to generate input sinusoidal signals. A Stanford Research SR560 low-noise amplifier is used to further filter-out the noise and mains interference of the sinusoidal signals, which are then applied to all the channel inputs. Finally, a National Instruments PXI-6544 acquisition card communicates with the chip through the I2C interface and collects the serial output data. A master clock of 48 MHz, provided by an external crystal oscillator, is used to generate on chip the 4.8-MHz oversampling clock and the 30-kHz down-sampling clock.

With a supply voltage of 0.8 V, the measured total power consumption of the chip is 1.61 mW when all the 128 channels are active. This includes the power consumption of the GPIOs (541.4 μW) during serial-data transmission. Therefore, the total power per channel is 12.57 μW, of which 3.29 μW (26%) are consumed by the channel analog circuit, 4.73 μW

(38%) are consumed by the digital blocks and 4.23 μW (34%) are from the GPIO. Table I shows a detailed power partitioning of the prototype NRIC.

The measured input-referred noise spectrum of the 128 channels in a full bandwidth of 10 kHz are shown in Fig. 12 (left). This was measured by connecting the inputs of all the channels to ground. The histograms of the total input-referred integrated noise in the LFP (0.5 Hz - kHz) and AP (300 Hz - 10 kHz) frequency bands are shown in Fig. 12 (right). The mean LFP noise is 11.90 ± 1.13 μV_{rms} (n = 128, 1 σ), while the mean AP noise is 7.71 ± 0.36 μV_{rms} (n = 128, 1 σ). A good channel-to-channel noise uniformity is observed in this measurement. Table II summarizes the estimated AP-noise partitioning of the channel based on our post-layout simulation results. The main noise contribution (97%) comes from the G_m stage. Both the AP and LFP noise performances of our NRIC are within the acceptable levels of the application, and similar to other widely used neural recording tools [1], [3].

Figure 13 (a) shows the reconstructed transient waveforms of the 128 channels when a 1-kHz, 10-mV_{pp} sinusoidal signal is applied to all the inputs. As can be observed, all the channels are fully functional and the gain variation across channels is 6.2% (1 σ). The channel offset is also extracted from the measured output waveforms and the histogram is shown in Fig. 13 (b). The mean offset is 0.09 ± 0.66 mV (n = 128, 1 σ). Since the channels are divided into 8 groups, each with an independent bias generator, a mismatch in the LSB of each channel group is expected. This is because the IDAC unit current is derived from the bias generator. To characterize this effect, the input-referred ADC LSB has been calculated for each channel from the measurements in Fig. 13 (c). The boxplot demostrates the distribution of LSB values for each channel group. It can be observed that the LSB variation in each group is very small, but the means across the 8 groups have a larger variation due to the mismatch between the 8 indepedent bias generators.

The measured output spectrum of one channel is shown in Fig. 14 (left). Here, a 1-kHz, 21.5-mV_{pp} input sinewave is applied. The measured SNR, SNDR and THD are 54.74 dB, 52.36 dB and −56.11 dB, respectively, over a 10-kHz bandwidth. Fig. 14 (right) shows the histogram of the SNR and THD across all the 128 channels. The mean SNR is 55.25 ± 0.32 dB, while the mean THD is −52.74 ± −2.17 dB. A good channel-to-channel uniformity is observed here.

Figure 15 shows the measured SNR and SNDR versus input amplitude for a 1-kHz signal. The SNR and SNDR increase with the input amplitude until ~20 mV_{pp}. Distortion starts to appear at large amplitudes due to the non-linearity of the G_m stage (including the HPF) and the residual distortion of the IDAC caused by the non-idealities of the clock generator. However, the SNR keeps increasing until a maximum amplitude of 43 mV_{pp}. Since extracellular neural signals have maximum amplitudes of 5-10 mV_{pp} [55], the extended input range improves the tolerance to motion artifacts during *in vivo* neural recording. It is important to notice that the THD remains below −40 dB (1%) for input amplitudes of up to 30 mV_{pp}, which is the acceptable non-linearity limit for this application.

B. In Vivo Measurement

To enable *in vivo* experiments with the proposed NRIC, a small ($2.5 \times 2.5\ cm^2$) and light (3.2 g) HS was built to provide connectivity to a computer (Fig. 16 (a) (left)). The HS consists of the NRIC, a serializer chip to transmit the data to a Neuropixels OneBox, LDO's to generate the required supply voltages, an oscillator to generate the master clock (48 MHz), decoupling capacitors and connectors.

We have performed acute *in vivo* experiments to further demonstrate the complete functionality of the NRIC. For this, a passive probe with 128 TiN electrodes of $13.5 - \mu m$ diameter (impedance: $182.6 \pm 21.4\ k\Omega$ @ 1 kHz) was implanted in the retrosplenial cortex of a C57Bl/6 J mouse. The animal was head-fixed while running on a treadmill. An illustration of the *in vivo* setup is shown in Fig. 16 (a) (right), while Fig. 16 (b) shows a 1.7-second extract of the recorded spontaneous activity in 25 channels. Both the full band and the software-filtered AP band are shown, demonstrating that the proposed architecture is able to record neural APs and LFPs [7].

C. Comparison with State-of-the-Art NRICs

Table III summarizes the features and measured performance of the proposed NRIC and compares them with recently-reported state-of-the-art neural readout architectures that cover both the LFP and AP frequency bands. Our design achieves one of the smallest areas (similar to [37]) and lowest power efficiency factors (PEFs). At the same time, our NRIC achieves rail-to-rail EDO cancellation, good noise performance and an improved input range compared to [2], [3], [13], [37]. The latter makes our design more suitable for recording experiments with freely-moving animals or in combination with near-by microstimulation. Although the AP noise is not as low as in [30], the performance is similar to [3] which is a well-established neurophysiology tool. The larger LFP noise is not a concern since LFP signals have much larger amplitudes than APs [55], and they are assessed by the power variation in the low-frequency range.

Differently from [13], the performance of our chip is fully characterized across all the channels. Our measurement results show a very good channel-to-channel uniformity, which is a crucial characteristic in high-channel-count neural interfaces. By combining AC-coupling, 1^{st}-order noise shaping and digital processing, our design achieves an excellent compromise between the most important performance metrics for this application: area, power, noise, input range and EDO cancellation.

When compared to other $\Delta - \Delta\Sigma$ designs (see Table IV), our design achieves the smallest area with competitive noise density and power/bandwidth. It is clear from the table that lower bandwidth designs [29], [34] are optimized to achieve very low noise and power at the expense of area. Although [21] achieves impressive noise and power performances in a large bandwidth, its area is too large to enable further channel-count scaling.

V. Conclusion

To further increase the density of existing neural-recording tools, more area- and power-efficient readout architectures are needed. However, system co-optimization is crucial to

ensure that other performance metrics such as noise, input range and electrode DC offset cancellation are also simultaneously achieved. We have reported an AC-coupled 1^{st}-order $\Delta - \Delta\Sigma$ architecture for the simultaneous acquisition of local field potentials and action potentials. To fully profit from the power and area benefits of the used scaled technology, we have pursued a digitally-intensive architecture with a novel combination of: i) AC-coupling for EDO rejection, ii) 1^{st}-order noise shaping, iii) fully-digital feedback integrator (up-down counter) and $\Delta\Sigma$ feedback summation, iv) 2^{nd}-order decimation, v) ultra-small bulk-regulated reference generator, vi) small-unit IDAC, and vii) DWA mismatch shaping. Because of these design choices, our design achieves one of the smallest channel areas compared with the state of the art, while also showing a very good compromise between all the above-mentioned metrics. We also demonstrated that the fabricated 128-channel prototype achieves a very good channel-to-channel uniformity, which is very important for ensuring good quality recording in high-density interfaces. The proposed digitally-intensive direct- digitization architecture holds the promise of enabling even higher density neural recording tools than those existing today.

Acknowledgment

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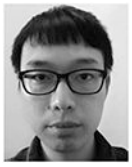

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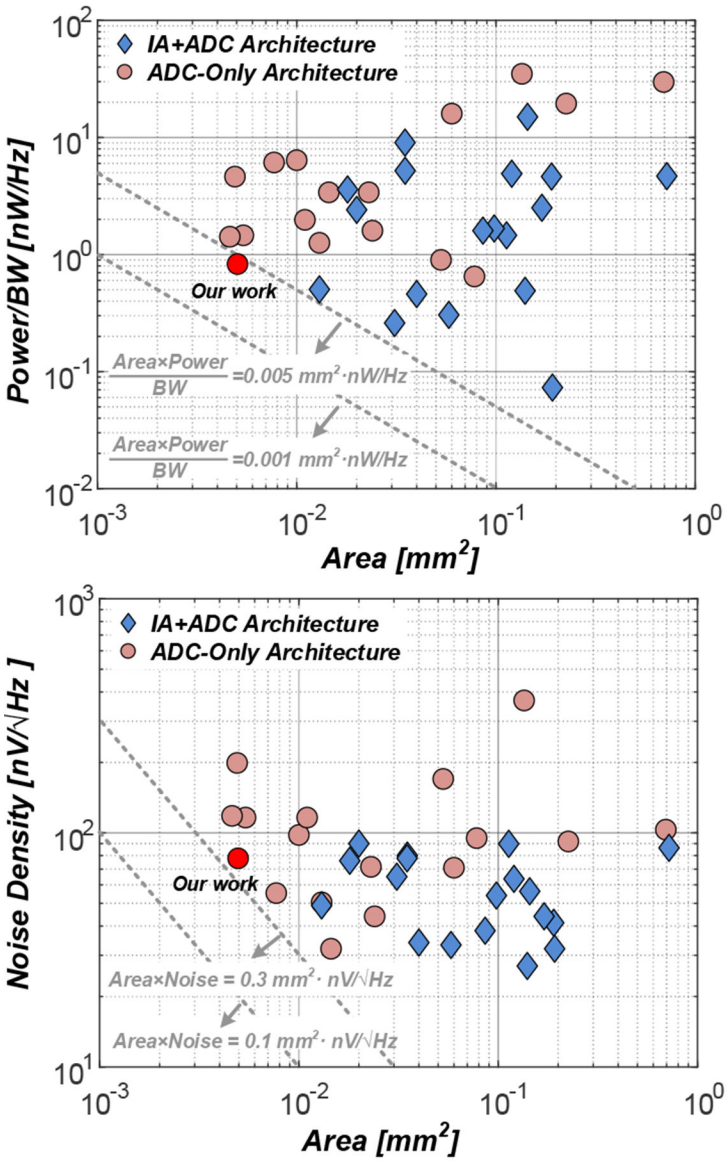

Fig. 1.

Performance comparison of state-of-art neural recording integrated circuits: IA+ADC architectures vs. ADC-only architectures. Data obtained from [1]-[3], [5], [8]-[23], [28]-[45]. Architectures with input multiplexers are not considered here since their noise performance is dominated by the aliased electrode/tissue noise.

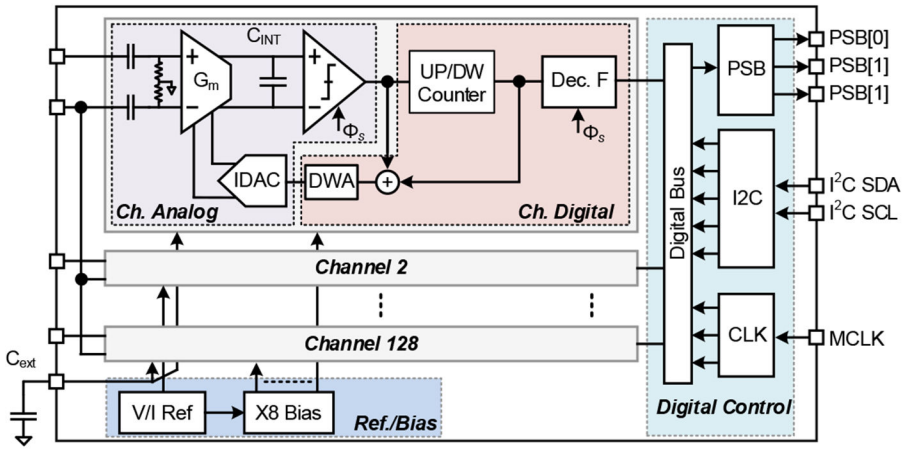

Fig.2.
System architecture of the prototype NRIC

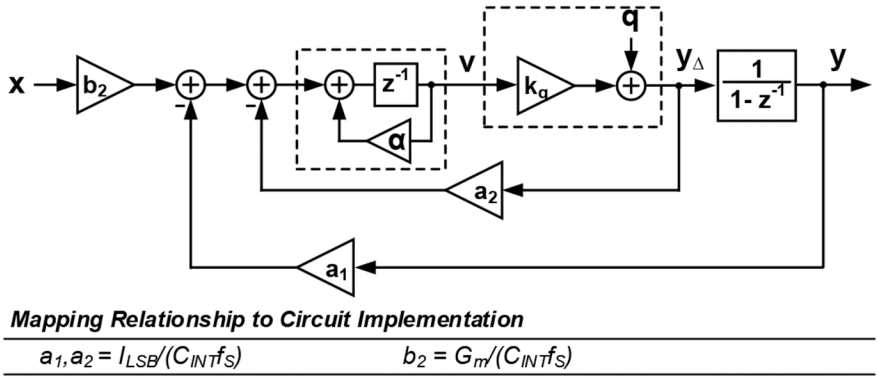

Fig. 3.

DT equivalent model of the proposed 1st-order hybrid DT-CT Δ – ΔΣ modulator and its mapping relationship with the circuit implementation.

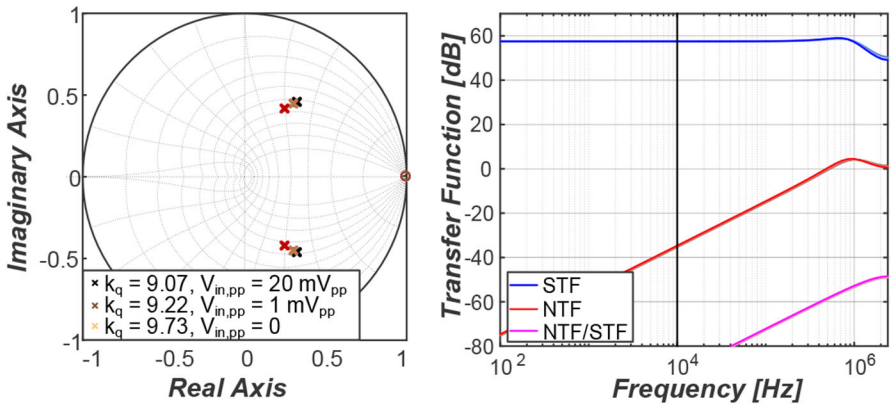

Fig. 4.

Pole-zero map with different quantizer gains k_q under different input amplitudes and the corresponding signal and noise transfer functions.

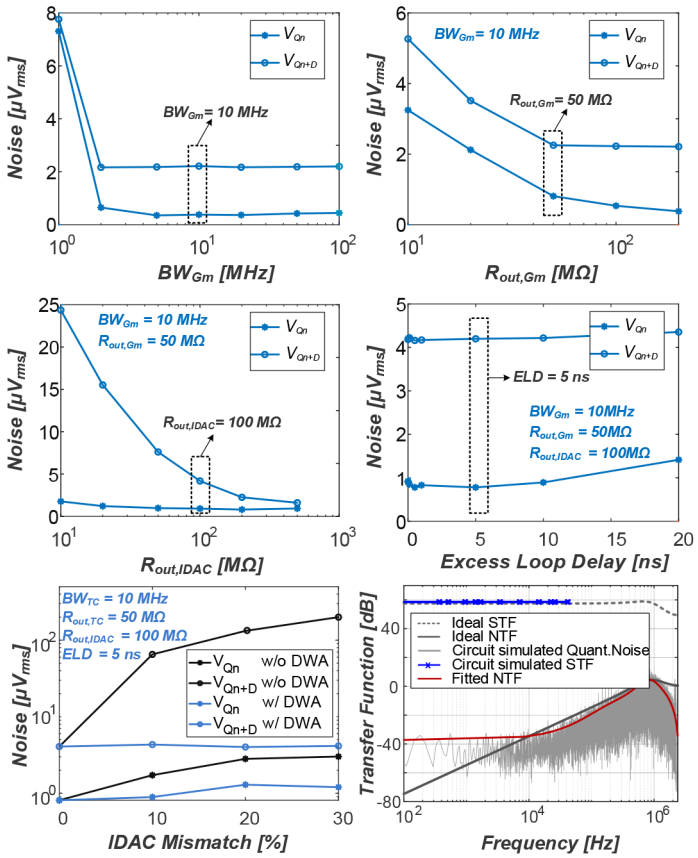

Fig. 5.

System-level simulations of the input-referred quantization noise (V_{Qn}) and distortion (V_{Qn+D}) across different OTA bandwidths, OTA output impedances, IDAC output impedances, excess loop delays and IDAC mismatches with and without DWA, where the black-dashed rectangles show the selected design specifications. Bottom-right: circuit-level simulations of the NTF/STF with the final circuit specification.

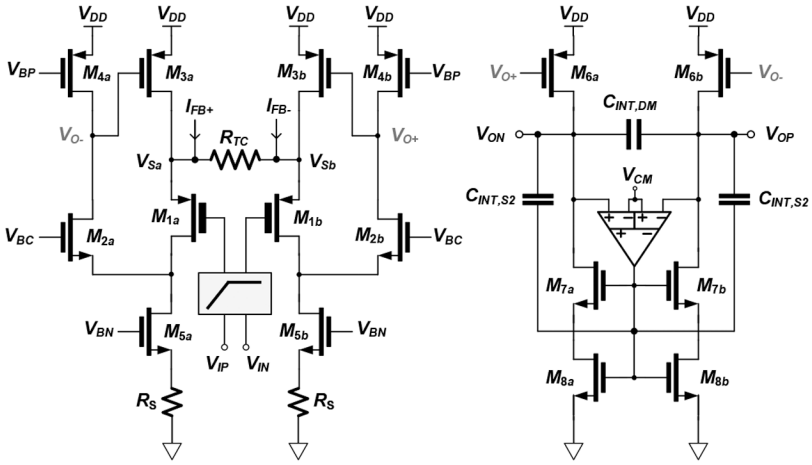

Fig. 6.
Schematic of the AC-coupled OTA stage.

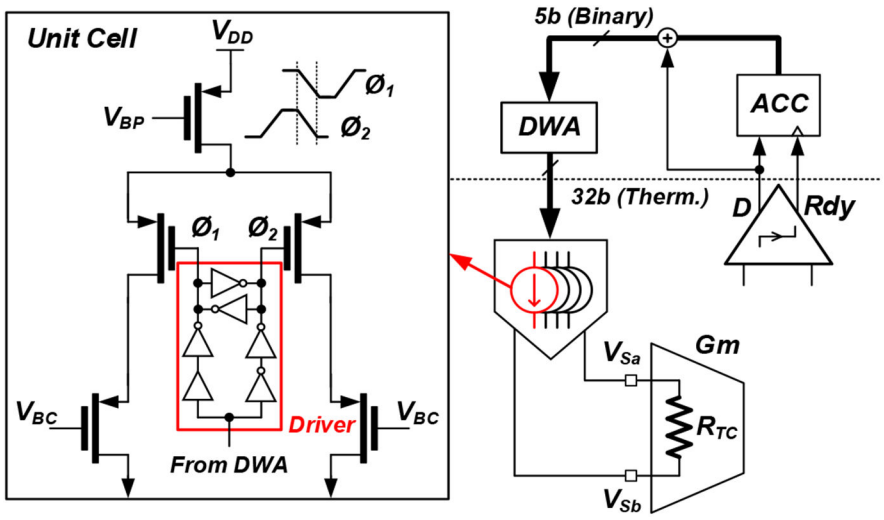

Fig. 7.
Schematic of the current-steering DAC.

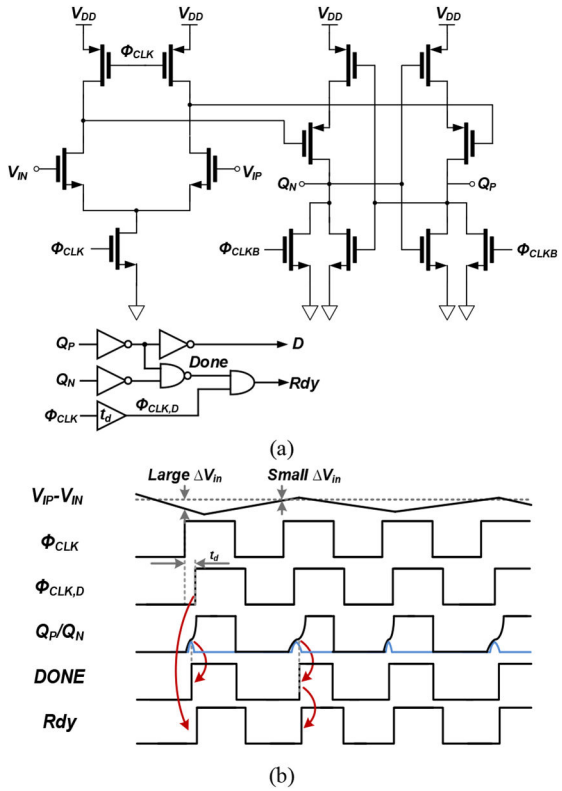

Fig. 8.
(a) Schematic of the 1-bit quantizer (comparator). (b) Timing diagram of the quantizer.

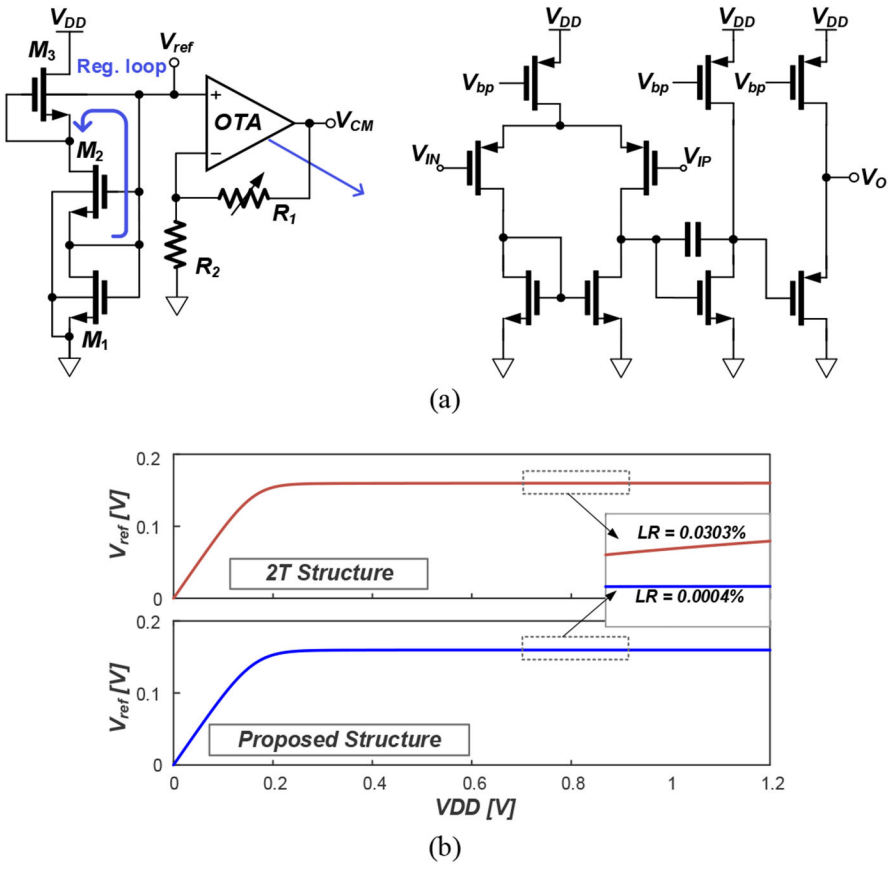

Fig. 9.

(a) Schematic of the proposed bulk-regulated reference generator. (b) Simulation results of the conventional 2T-structure and the proposed bulk-regulated reference generator where $LR = \Delta V_{ref} / \Delta VDD \times 100\,\%$.

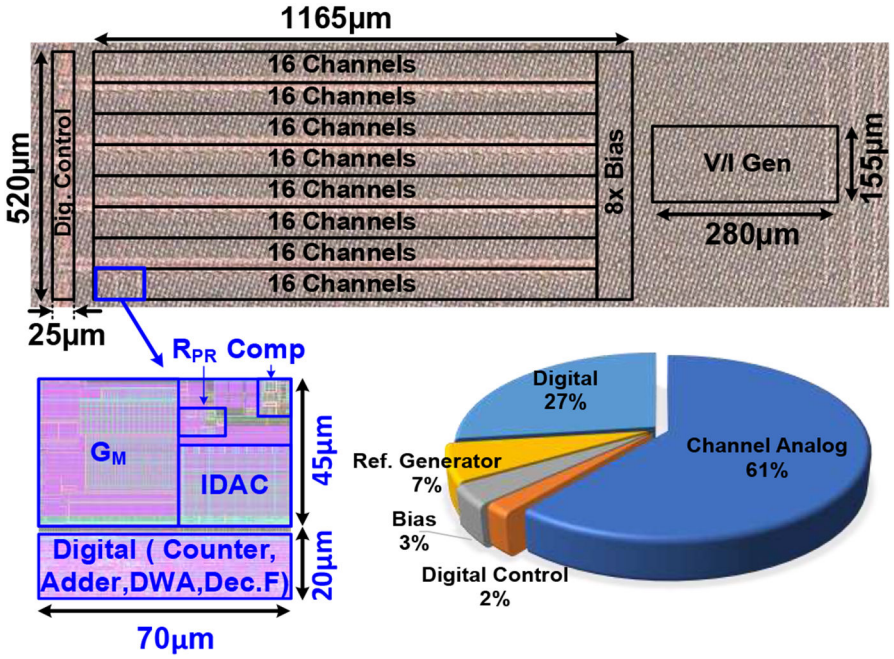

Fig. 10.

Micrograph of the fabricated 128-channel NRIC and the total channel area breakdown.

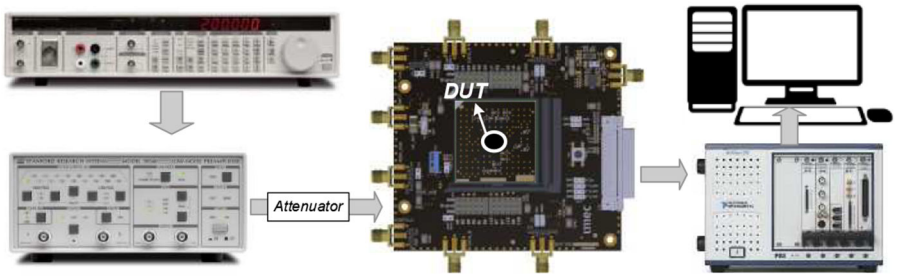

Fig. 11.
Measurement setup for chip electrical characterization.

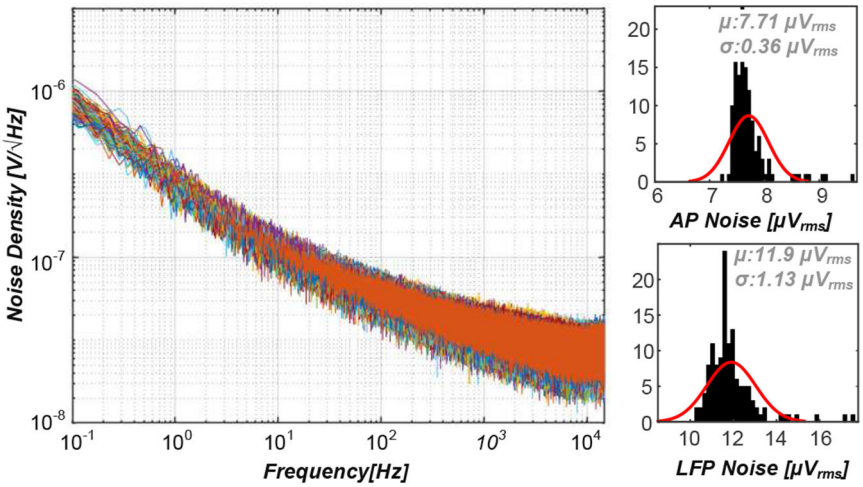

Fig. 12.

Measured input-referred noise spectra of the 128 channels (left) and histograms of the integrated AP and LFP noise across channels (right).

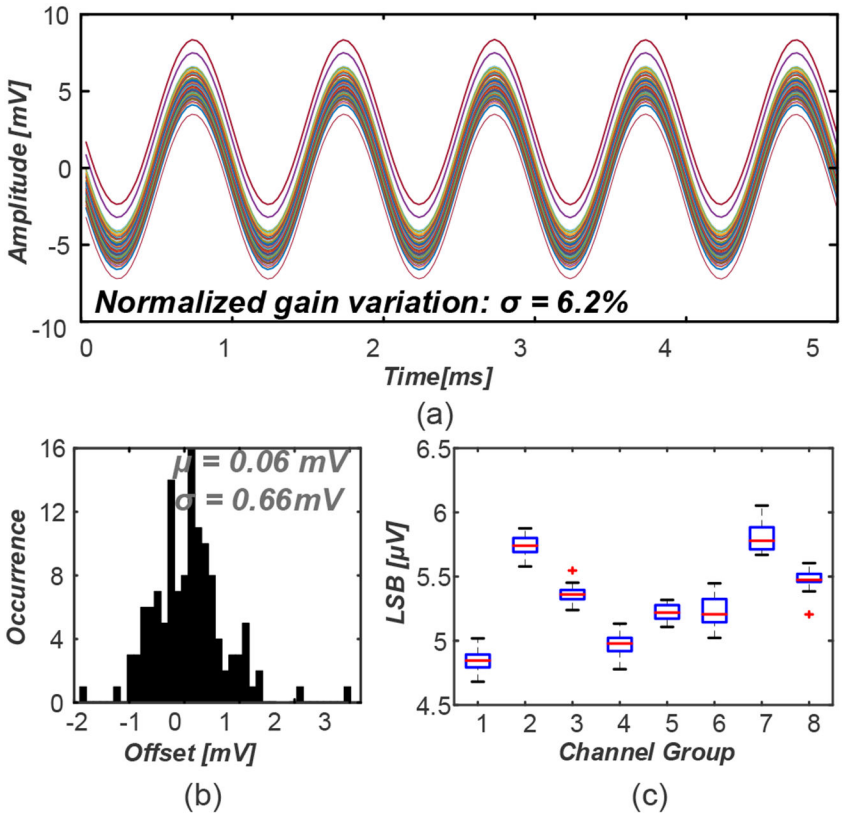

Fig. 13.

(a) Reconstructed transient output waveform for all the 128 channels. (b) Channel offset histogram. (c) Input-referred ADC LSB boxplot across all the channels in the 8 different channel groups.

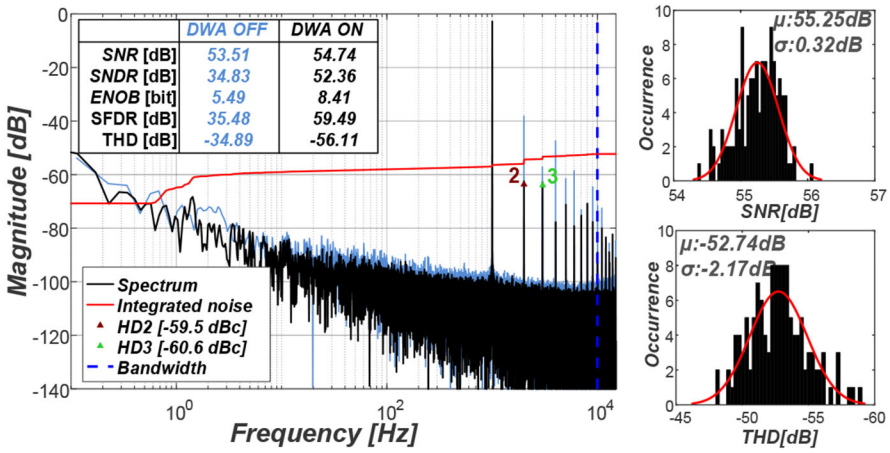

Fig. 14.

Left: channel spectrum analysis with a 21.5-mV_{pp}, 1-kHz sinewave input, with and without DWA. Right: histograms of the SNR and THD across 128 channels.

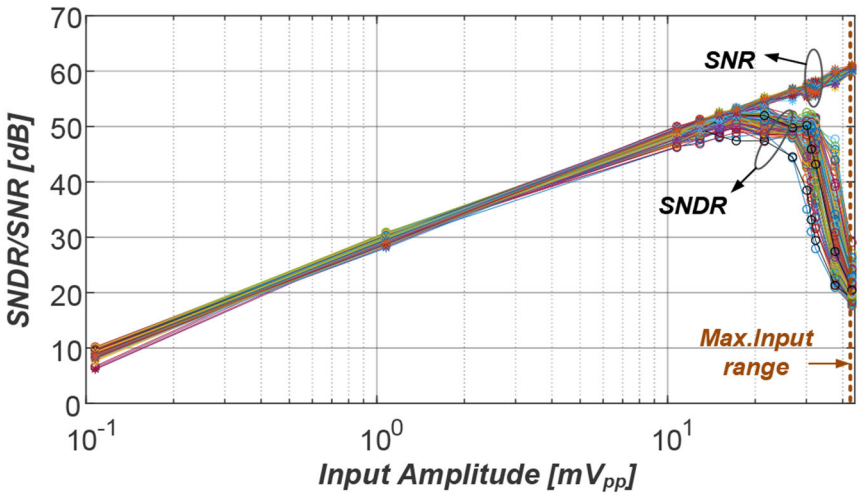

Fig. 15.
Measured SNR and SNDR vs. input amplitude

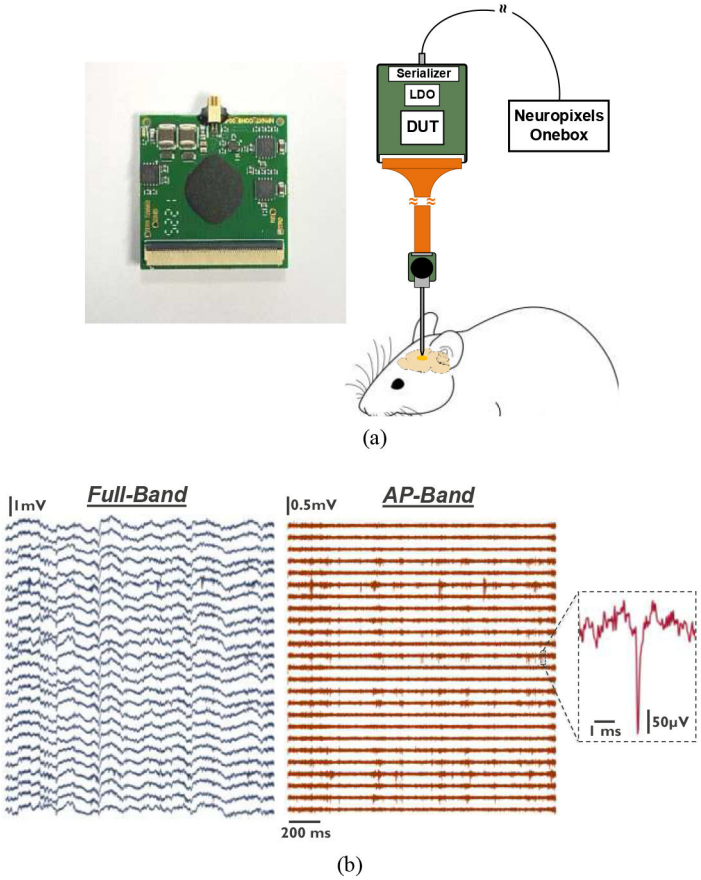

Fig. 16.

(a) Diagram of the setup for *in vivo* measurements. (b) Measured neural signals.

TABLE I

Power Partitioning per Channel

Block	Measured Power
Channel Analog	$3.29\,\mu W$
DWA	$1.47\,\mu W$
Dec. F	$0.45\mu W$
Other Digital	$2.81\mu W$
Ref/Bias Gen	$0.32\mu W$
GPIO	$4.23\mu W$
Total	$\mathbf{12.57\mu W}$

TABLE II

AP Noise Partitioning per Channel

Source	Estimated Noise [a]
Gm	$7.50\ \mu V_{rms}$
HPF	$0.45\ \mu V_{rms}$
IDAC	$1.12\ \mu V_{rms}$
Quant. Noise	$1.29\ \mu V_{rms}$
Total	$\mathbf{7.71\ \mu V_{rms}}$

[a] Estimated from post-layout simulation

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TABLE III

Performance Summary and Comparison with Prior State-of-the-Art

	This work	Wang [30]	Yoon [13]	Wang [3]	Wendler [37]	De Dorigo [2]	Lee [31]
Technology [nm]	22	55	65	130	180	180	110
Supply [V]	0.8	1.2	1.2[e]	1.2	1.8	1.8	1.0
Topology	AC-coupled 1st order $\Delta-\Delta\sum$	DC-coupled 2nd order $\Delta-\Delta\sum$	AC-coupled, IA + SAR ADC	AC-coupled, IA + SAR ADC	DC-coupled, 2 Step, $I\Delta\sum$	DC-coupled $I\Delta\sum$	DC-coupled 2nd order $\Delta\sum$
No.of Channels	128	16	1024	384	8	144	1
Area/Ch [mm^2]	**0.0045**	0.0077	0.0062	0.035	0.0046	0.0049	0.078[c]
Total area/Ch [mm^2]	0.0051	0.0298	0.02	0.0497	-	-	0.078[c]
AP Noise[μV_{rms}] (0.3-10kHz)	7.71±0.36	5.53±0.36	8.89[b]	7.43±0.72	4.46/11.83[f]	13.43	9.5 (1-10kHz)
LFP Noise[μV_{rms}] (0.5HZ-1kHz)	11.9±1.13	2.88±0.18	6.8[b] (5Hz-1kHz)	7.78±0.93	2.51/9.21[f]	9.95	
Bandwidth [Hz]	0.1-10k	0.5-10k	5-10k	0.5-10k	0.5-10k	0.5-10k	1-10k
Power/Ch[μW]	6.02[g]	61.2	2.72[h]	45.3[h]	14.62	39.14	6.5[c]
Total power/Ch[μW]	12.57	-	24.08	95.1	25.75	46.08	-
Channel PEF[a](AP Band)	54.55	285.28	33	381.2	306[f]	1076.1	93.55[c,d]
Total PEF[a](AP Band)	113.9	-	290.09	800.26	539[f]	1267	-
THD	0.15-0.41% @21.5mVpp	0.05-0.44% @20mVpp	0.57% @-0.79dBFS	0.17% @10mVpp	0.078%/1.24%[f] @10mVpp	0.22% @10mVpp	0.095% @285mVpp
AC Input Range [mV_{pp}]	43	148	0.75-4.87[e]	12.5	14	22.5	300
EDO Tolerance [mV]	Rail-to-Rail	±70	Rail-to-Rail	Rail-to-Rail	±60	<22.5	±50

[a] PEF calculated by $V_n^2 x(2xP / V_T 4k_B T\pi BW)$

[b] No statistical data provided

[c] Decimation filter not included

[d] PEF with full bandwidth

[e] Estimated

[f] When a ±60mV offset appears in the input

[g] Includes channel analog, DWA, decimation filter, up/down counter and adder (the last 2 are estimated from digital back-end)

[h] Includes analog channel + ADC.

TABLE IV

Comparison with Prior $\Delta - \Delta\sum$ Architectures

	This work	Kassiri [29]	Reza [34]	Wang [30]	Park [21]
Application	**AP+LFP**	ECoG	ECoG	AP+LFP	AP+LFP
No. of Channels	**128**	64	32	16	128
Technology[nm]	**22**	130	130	55	180
Supply[V]	**0.8**	1.2	1.2	1.2	0.5/1.0
Area/Ch [mm^2]	0.0045	0.013	0.023	0.0077	0.058
Noise[μVrms]	**7.71**	1.13[b]	1.6	5.53	3.32
Noise bandwidth [Hz]	**300-10k**	0.1-500	1-500	300-10k	0.5-10.9k
Noise Density [nV/√Hz]	**78.28**	50.54	71.63	56.15	31.80
Channel Power[μW]	**6.02**	0.63[a]	1.7	61.2	3.05
Bandwidth [Hz]	**0.1-10k**	0.01-500	1-500	0.5-10k	0.5-10.9k
Power/Bandwidth [nW/Hz]	**0.62**	1.26	3.41	6.31	0.28
Channel PEF	**54.55**	9.80	12.90	285.29	4.56
Input Impedance[Ω]	**∞ @ DC**	99k-102k[b]	1.47G @ DC	663M @ 10Hz	∞ @ DC
THD	**0.15-0.41% @21.5mVpp**	-	-	0.05-0.44% @20mVpp	0.019% @3mVpp

[a] Decimation filter is not included

[b] Calculated with OSR = 1000