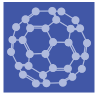 nanomaterials

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A Design of High-Efficiency: Vertical Accumulation Modulators Based on Silicon Photonics

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Abstract: On-chip optical modulators, which are capable of converting electrical signals into optical signals, constitute the foundational components of photonic devices. Photonics modulators exhibiting high modulation efficiency and low insertion loss are highly sought after in numerous critical applications, such as optical phase steering, optical coherent imaging, and optical computing. This paper introduces a novel accumulation-type vertical modulator structure based on a silicon photonics platform. By incorporating a high-K dielectric layer of ZrO_2, we have observed an increase in modulation efficiency while maintaining relatively low levels of modulation loss. Through meticulous study and optimization, the simulation results of the final device structure demonstrate a modulation efficiency of 0.16 V·cm, with a mere efficiency–loss product of 8.24 dB·V.

Keywords: silicon photonics; plasma dispersion effect; optical modulator; modulation efficiency; loss-efficiency product

Citation: Zhou, Z.; Li, Z.; Qiu, C.; Chen, Y.; Xu, Y.; Zhang, X.; Qiao, Y.; Wang, Y.; Liang, L.; Lei, Y.; et al. A Design of High-Efficiency: Vertical Accumulation Modulators Based on Silicon Photonics. *Nanomaterials* **2023**, *13*, 3157. https://doi.org/10.3390/nano13243157

Academic Editors: Werner Blau, Mingming Tan, Feng Wen and Tianhua Xu

Received: 14 November 2023
Revised: 6 December 2023
Accepted: 11 December 2023
Published: 16 December 2023

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1. Introduction

Optical modulators are critical enablers in the fields of optical telecommunications, optical interconnects, optical sensing, and detection. Due to their low power consumption, high modulation bandwidth, rapid modulation speed, and mass-production capabilities, on-chip silicon photonic-based modulators have emerged as the most promising candidates, offering extraordinary solutions [1,2]. Their applications extend to optical linear matrix multiplications and optical phase steering, thereby necessitating densely deployed phase modulators [3–5]. Devices that demonstrate muscular modulation strength, high modulation efficiency, and low optical loss, as well as the potential for dense deployment with minimal crosstalk, are in high demand.

Generally, photonic modulators based on the thermo-optical effect can provide strong modulation with relatively low optical loss due to significant thermo-optical coefficients [6]. However, these thermal methods are less precise and suffer from significant crosstalk between channels, thereby hindering further advances in integration density. In contrast, electro-optic (EO)-based modulators offer precise optical phase control with minimal crosstalk, making them indispensable for large-scale, compact photonic circuits. The state-of-the-art silicon photonic EO modulators, based on plasma dispersion [7,8], exhibit the highest modulation strength. These operate with an accumulation-type structure, where carriers accumulate near the SiO_2 dielectric layer between the N-doped and P-doped waveguides under an applied electric potential. However, the modulation efficiency of this approach remains insufficient, and optical loss is not negligible. The best-reported

modulation performance is approximately 0.2 V·cm [9], with the efficiency–loss product limited to around 20 dB·V [10–13].

To address these issues, we propose a novel vertical structural accumulation-type silicon photonic modulator. Our approach, which differs from conventional capacitance accumulation modulators, introduces a dielectric layer of ZrO_2 to replace SiO_2. ZrO_2, a high K (HK) material, exhibits a significantly larger dielectric constant than SiO_2 [14,15], enhancing carrier accumulation capacity. Well-studied as an HK metal gate material in advanced MOSFET structures [16,17], ZrO_2 can be easily incorporated using standard CMOS-compatible processes. Integrating ZrO_2 into the design of carrier accumulation modulators improves modulation efficiency to 0.16 V·cm. Compared to traditional carrier accumulation modulators, our proposed design offers a 20% enhancement in modulation efficiency and a 40% decrease in the efficiency–loss product. This research addresses the challenges of low modulation efficiency and integration complexities in densely deployed modulators (Figure 1).

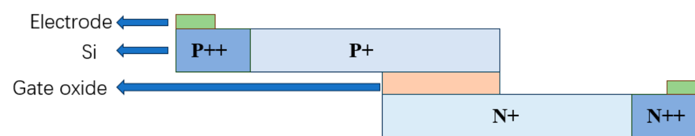

Figure 1. Schematic diagram of conventional accumulation-type electro-optic modulator.

2. Principles and Methods

2.1. Principles

In silicon-based modulators, the plasmonic dispersion effect is the fundamental principle employed. Three primary modulation structures are utilized: (i) carrier injection-based [18], (ii) carrier depletion-based [19,20], and (iii) carrier accumulation-based [9,12,13]. In injection-type structures, modulation is attained by altering the semiconductor's refractive index and absorption coefficient through electron and hole injection. These modulators are typically noted for their high modulation efficiency. However, their overall performance may be negatively influenced by the carrier lifetime limitations inherent in these systems. Depletion-based modulation, often achieved through reverse biasing of PN junctions, results in the highest modulation speed but suffers from a larger footprint, increased power consumption, and comparatively lower modulation efficiency.

In contrast, optical modulators based on carrier accumulation do not modulate carrier concentration through electrically controlled injection. Instead, they incorporate a dielectric layer within the waveguide, facilitating the accumulation of free carriers on either side of this layer. This design allows such devices to bypass the limitations imposed by minimal carrier lifetime, enhancing modulation speed. Conversely, accumulation-based modulation offers a balanced performance, achieving high modulation efficiency while optimizing speed, power consumption, and footprint [21].

When the wavelength is 1550 nm, the refractive index change is empirically related to the carrier concentration as follows [22]:

$$\Delta n = -5.40 \times 10^{-22} N_{\mathrm{e}}^{1.011} - 1.53 \times 10^{-18} N_{\mathrm{h}}^{0.838} \quad (1)$$

$$\Delta \alpha = 8.88 \times 10^{-21} N_{\mathrm{e}}^{1.167} + 5.84 \times 10^{-20} N_{\mathrm{h}}^{1.109} \quad (2)$$

where N_{e} represents the electron concentration, N_{h} represents the hole concentration, and the above is referred to as the Soref–Bennett formula.

The vertical structure is frequently regarded as one of the optimal choices for efficient modulators. Currently, this structure is predominantly constructed using Poly-Si-oxide-silicon. The peak modulation efficiency attained with this design is around 0.2 V·cm [9]. The key factor influencing modulation efficiency is the carrier accumulation capability, which is determined by material characteristics, such as (i) the dielectric constant of the oxide layer, (ii) the band gap in the oxide layer, and (iii) the affinity of electrons in the oxide

layer. Of these, the dielectric constant plays the most crucial role. Therefore, employing high-K materials with a higher dielectric constant increases capacitance and enhanced carrier accumulation.

In the design of high-efficiency modulators that utilize carrier accumulation, three primary types are identified based on their gate electrode materials: ITO–oxide–silicon [23,24], III–V materials–oxide–silicon [25,26], and silicon–oxide–silicon [9,12,13]. Here, the choice of gate electrode material significantly influences the refractive index change. Modulators with ITO gate electrodes often exhibit high modulation efficiencies but suffer considerable modulation loss, limiting their efficiency benefits. Modulators using III–V gate electrode materials, while achieving higher efficiency and minimal losses, often require complex bonding operations in their fabrication, which pose challenges for large-scale integration. In contrast, silicon–oxide–silicon-based modulators, particularly those using SiO_2 as the oxide layer, have reached the efficiency limits, prompting the need for innovative approaches to enhance their performance.

Figure 2 illustrates the design of the intended optical modulator using SOI (silicon-on-insulator) technology, which is compatible with CMOS processes. SOI technology is a prevalent methodology in fabricating silicon photonic chips and is extensively employed in producing various optoelectronic devices [27]. The design comprises three distinct layers: a top layer, a middle layer, and a bottom layer. These layers consist of polysilicon (poly-Si), an oxide layer, and crystal silicon. Both the poly-Si and the single-crystal silicon are doped with a concentration of 1×10^{18} cm^{-3} to reduce resistance, enhance the electro-optic (EO) bandwidth, and provide an abundance of free carriers for accumulation. The oxide layer, with a thickness of 5 nm, is made from zirconium dioxide (ZrO_2). The poly-Si layer measures 150 nm thick, while the single-crystal silicon layer is 220 nm thick. The top electrode, which is positioned 900 nm from the optical field center, aligns with the bottom electrode, strategically placed along the left side of the single-crystal silicon. This configuration significantly mitigates losses, as indicated in reference [28].

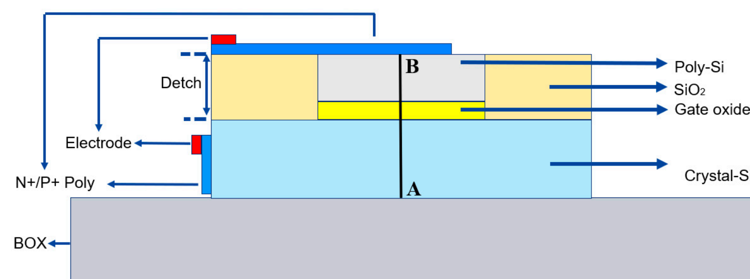

Figure 2. Schematic diagram of the initial design model.

2.2. Methods

The simulation work introduces the overall simulation tools, boundary conditions, grid division, and settings of the excitation port. This simulation adopts the finite element analysis method, which is divided into two parts: electrical simulation and optical simulation.

The electrical stimulation primarily involves applying different voltages at the excitation port to obtain varying distributions of carriers in semiconductor materials. The changes in the refractive index and absorption rate caused by the carrier variations are incorporated into the optical model for optical mode simulation using the Soref–Bennett formula. Except for the excitation port, all other boundaries are considered ideal insulators in the electrical simulation. The semiconductor material model is a steady-state model, which is calculated primarily from the following formula:

$$\nabla \cdot \mathrm{J}_n = 0 \tag{3}$$

$$\nabla \cdot \mathrm{J}_p = 0 \tag{4}$$

$$\mathrm{J}_n = qn\mu_n \nabla E_c + qD_n \nabla n - qnD_n \nabla \ln(N_c) + qnD_{n,\,\mathrm{th}} \nabla \ln(T) \tag{5}$$

$$J_p = qp\mu_p \nabla E_v - qD_p \nabla p + qpD_p \nabla \ln(N_v) - qpD_{p,\,\mathrm{th}} \nabla \ln(T) \tag{6}$$

in the optical simulation, the working wavelength is set to 1550 nm. A comprehensive optical mode simulation is conducted after introducing the refractive index changes caused by the carriers into the optical model. The boundary conditions for this simulation are ideal conductors. Since this is an optical field mode analysis simulation, no fixed excitation exists. The primary formula used during the optical mode simulation process is:

$$\nabla \times (\nabla \times \mathrm{E}) - k_0^2 \epsilon_r \mathrm{E} = 0 \tag{7}$$

$$\alpha = j\beta + \delta_z = -\lambda \tag{8}$$

$$\mathrm{E}(x, y, z) = \widetilde{\mathrm{E}}(x, y) e^{-\alpha z} \tag{9}$$

finally, the grid division is consistent in both the electrical and optical simulations, utilizing a grid size with a side length of 1 nanometer (nm). This acceptable grid density helps to enhance the reliability of the simulation results.

Moreover, in designing the optical modulator, several key parameters are prioritized as our primary criteria for design and optimization. First, the magnitude of the applied voltage is critical, as it directly affects compatibility with the standard voltage used in the CMOS-process-integrated circuits. This parameter is essential for enhancing the density of the optoelectronic co-design. Second, the modulation efficiency, represented as $V\pi L$ (V·cm), the optical loss (measured in dB/cm), and the optimal figure of merit (FOM), which combines specific values to balance both aspects, are central to our evaluation. The lower the numerical value for the modulation efficiency, the higher the integration capability of the modulator. Similarly, a lower efficiency–loss product ($\alpha V\pi L$) indicates greater cost-effectiveness in the design context.

3. Results

To assess the differences in carrier accumulation capacities between high K (HK) materials and conventional SiO_2 dielectric materials, we conducted a comparative analysis under a −2 V voltage condition for materials. Figure 3 illustrates that using HK material significantly increases carrier accumulation on both sides of the dielectric layer. Based on empirical formulas, this marked increase will lead to enhanced modulation efficiency and corresponding changes in the effective mode refractive index.

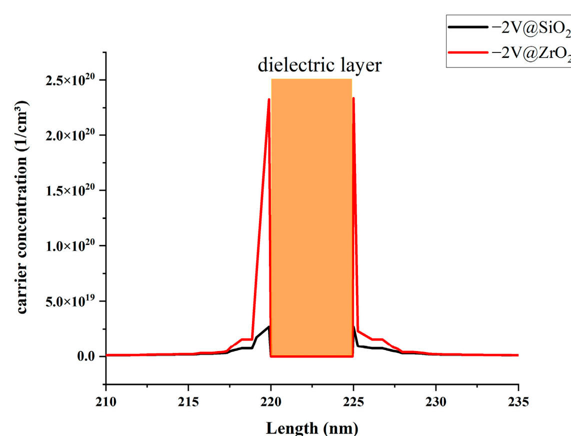

Figure 3. Traditional material vs. HK material carrier accumulation comparison.

Having demonstrated the superior carrier accumulation capabilities of high-K (HK) materials, our research next focused on exploring the relationship between applied voltage and modulation performance. The range of applied electrode voltages spanned from −4 V to 0 V. Our simulations, illustrated in Figure 4, show a consistent decrease in the $V\pi L$ value as voltage increases. Notably, at −1.4 V, a critical juncture is observed where $\alpha \cdot V\pi L$

reaches an optimal point. At this voltage, the modulation efficiency peaks at 0.29 V·cm, accompanied by a relatively low optical loss of 38.31 dB/cm and an efficiency–loss product of 11.12 dB·V. These metrics significantly outperform those of traditional silicon-based SiO_2 dielectric materials that are typically used in modulator devices. Capitalizing on this critical voltage point opens avenues for further performance enhancement through structural optimizations.

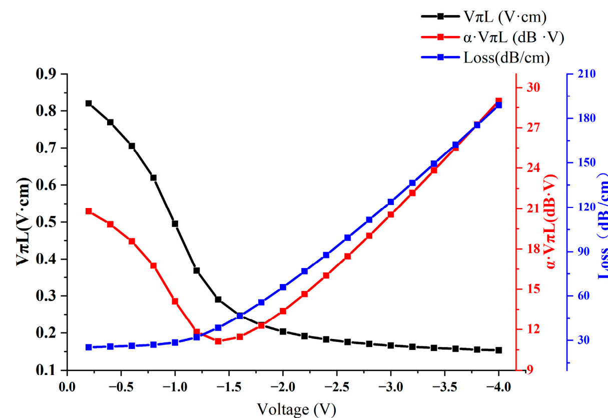

Figure 4. Voltage–modulation performance relationship chart.

Three principal factors determine the modulation efficiency of optical modulators. Firstly, the characteristics of the dielectric layer, which include intrinsic properties, such as dielectric constant, electron affinity, and bandgap width, are critical, as well as dimensional attributes, including layer thickness. These factors directly influence the capacitor's value and the capacity for carrier accumulation. Secondly, doping concentration significantly impacts modulation efficiency, especially regarding carrier density in monocrystalline and poly-Si. Lastly, there is a notable correlation between the modulator's geometric variables, such as the thickness and etching depth of poly-Si, and its modulation efficiency. Collectively, these factors substantially impact the modulation efficiency, optical loss, and efficiency–loss product of the modulator.

Our approach to designing and optimizing modulators is meticulously structured into three distinct phases, with each phase focused on enhancing the performance aspects mentioned above. Through this phased methodology, we aim to enhance the modulator's performance by precisely adjusting these variables. This approach aims to achieve higher modulation efficiency and the lowest possible product of loss–efficiency.

3.1. Dielectric Layer Thickness

Firstly, the impact of the dielectric layer thickness is approached by defining the planar capacitor formula:

$$C = A\frac{\varepsilon_0 \varepsilon_r}{d} \tag{10}$$

where A denotes the planar surface area, d represents the distance between the two electrode plates, ε_0 stands for the vacuum permittivity, and ε_r is the dielectric constant of the oxide layer material.

According to the formula, an increase in the oxide layer thickness leads to a reduction in capacitance, which, in turn, diminishes the capacity for carrier accumulation. To investigate the relationship between the thickness of the oxide layer and modulation performance, we generated performance graphs for each modulator with various oxide layer thicknesses, from 5 to 11 nanometers, and under different voltage conditions. The results of these tests are depicted in Figure 5a,b.

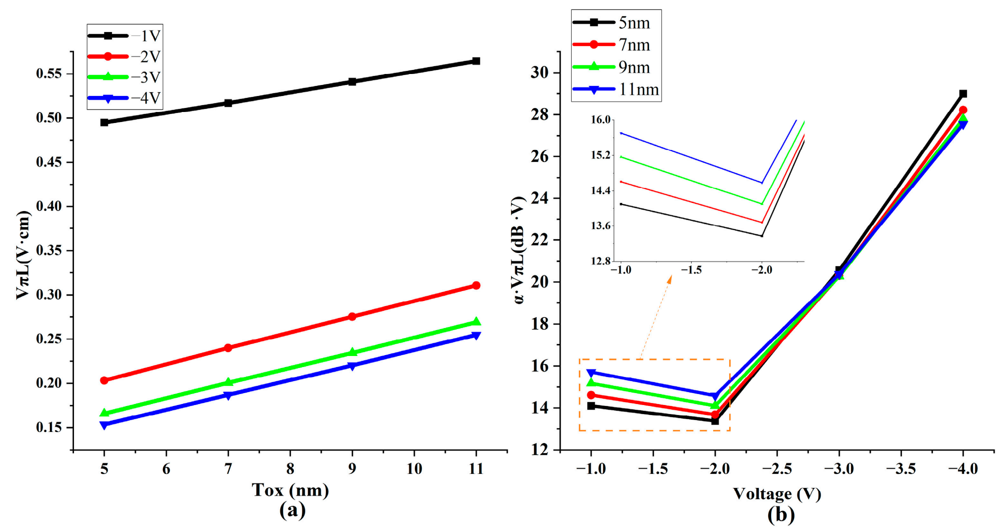

Figure 5. Relationship between oxide layer thickness (Tox) and modulation performance. (**a**) Schematic diagram of modulation efficiency changing with oxide layer thickness (**b**) Efficiency–loss product changing with voltage and oxide layer thickness.

The observed outcomes align with the predictions made by the capacitance formula. As the thickness of the dielectric layer increases, capacitance decreases, resulting in reduced carrier accumulation. When evaluating the modulation efficiency and efficiency–loss product parameters, using thicker oxide layers than the optimized voltage range proves counterproductive. Such thicknesses lead to a higher efficiency–loss product and lower modulation efficiency. Considering the complexities inherent in manufacturing processes, the optimal thickness of the oxide layer was 5 nm.

3.2. Doping Concentration

The next step in our study involved evaluating the impact of doping, a critical parameter that directly affects modulation capabilities. Higher doping concentrations introduce a more significant number of carriers, thereby enhancing modulation abilities. However, empirical formulas indicate that holes, compared to electrons, result in more considerable refractive index changes and reduced losses. To confirm this observation, we analyzed the variations in losses and efficiency–loss product at different concentrations of P-doping and N-doping, specifically at the critical voltage of −1.4 V. The results of this analysis are presented in Figure 6a,b.

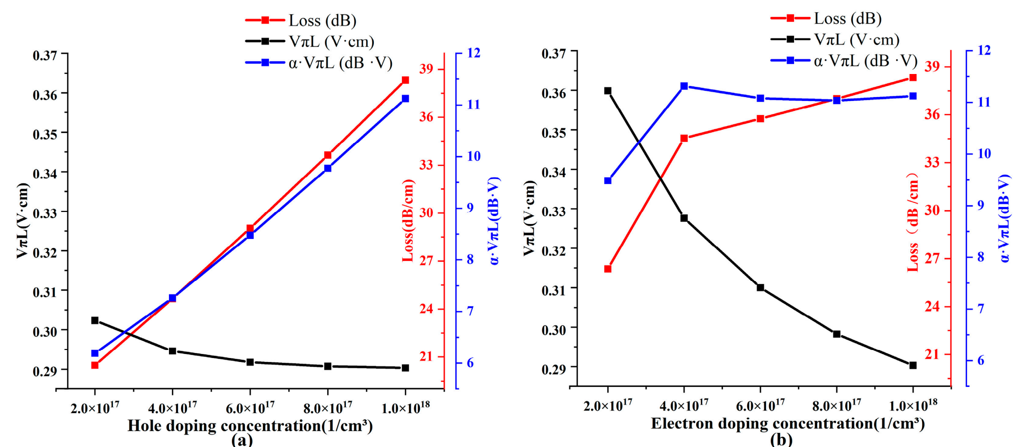

Figure 6. Performance variation under different doping conditions. (**a**) P-doping and (**b**) N-doping.

Both P-doping and N-doping demonstrate increased losses. However, lower losses and efficiency–loss products are attainable when reducing the P-doping concentration. At a P-doping concentration of 2×10^{17} $1/\text{cm}^3$, the losses were merely at 20.46 dB, resulting in an exceedingly low efficiency–loss product of 6.19 dB·V. In contrast, within the same range of concentration variations, the minimum efficiency–loss product for N-doping was confined to 9.5 dB·V. Therefore, our data suggest that minimizing P-doping near the pole voltage in our designed structure can yield superior modulation performance.

Moreover, according to empirical formulas, holes demonstrate lower absorption than electrons. However, they generate more significant changes in the refractive index. Consequently, maintaining hole concentrations that are too low might result in a decrease in modulation capabilities.

3.3. Modulator Geometric Factors

The last crucial factor affecting modulation efficiency is the influence of geometry. The distance between the region where carriers amass high charge density, and the center of the optical mode considerably affects both the modulation efficiency and the product of the loss–efficiency. The highest modulation efficiency occurs when these elements perfectly align, as suggested by the following formula:

$$n_{\text{eff}}(V) = n_{\text{eff},i} + \frac{\int E^*(y) \cdot \Delta n(y,V) E(y) \text{d}y}{\int E^*(y) \cdot E(y) \text{d}y} \cdot \frac{\text{d}n_{\text{eff}}}{\text{d}n_{\text{co}}} \tag{11}$$

here, the equation denotes $n_{\text{eff},i}$ as the effective refractive index of the non-doped optical waveguide, $\text{d}n_{\text{eff}}/\text{d}n_{\text{co}}$ as the ratio of the mode change effective refractive index to the change in refractive index of the optical waveguide core layer, which is very close to 1, and $E(y)$ as the 1D electric field distribution obtained via the effective refractive index method.

The primary influencers of the modulator's ultimate performance are derived from the formula mentioned above and the current geometric configuration. The key aspects are predominantly the ridge height (aligned with the thickness of the poly-Si) and the depth of etching (relating to the alteration in the refractive index within the single-crystal silicon region).

We initiated the investigation by analyzing the etching depth. Subsequently, based on our model configuration and the manufacturing process, we can convert the silicon on both sides of the waveguide into silicon dioxide through an etching operation. Therefore, we can assume an etching depth of 155 nm at the initial state, as depicted in Model Figure 2. Here, the sides of the poly-Si are entirely composed of silicon dioxide. However, in this research, we investigated the impact of silicon dioxide confinement on the overall modulation performance by increasing the etching depth to transform the monocrystalline silicon region into silicon dioxide. The results are illustrated in Figure 7a,b.

An increased etching depth facilitates the transformation of single-crystal silicon adjacent to the center of the optical field into silicon dioxide. This change alters the refractive index, resulting in a more concentrated electric field intensity on both sides of the dielectric layer. Our graph directly correlates with increased etching depth and enhanced modulation efficiency. Thus, we analyzed a normalized light field intensity profile along line AB to support this hypothesis, overlaid with carrier concentration data at a voltage of 4 V. This analysis is visually represented in Figure 8, where it is evident that a greater etching depth is associated with higher normalized light field intensity values on both sides of the dielectric layer, leading to increased modulation efficiency.

In our investigation of the efficiency–loss product, we performed scans of this parameter at various etching depths using four different voltage settings. A clear and consistent pattern emerged from this analysis: At all voltage levels, the efficiency–loss product decreased as the etching depth increased. This finding confirms that augmenting the etching depth effectively reduces the loss–efficiency product, thus, improving the modulator's performance.

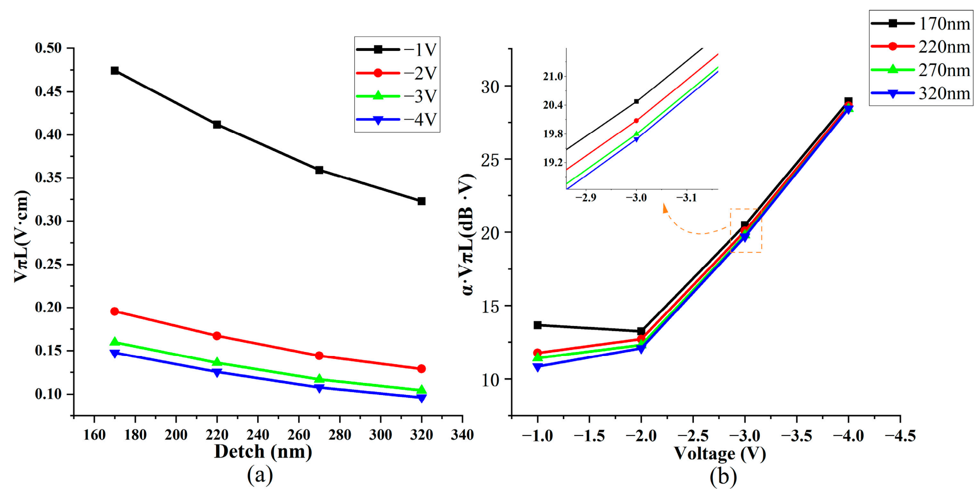

Figure 7. Schematic of modulation performance at different etching depths (Detch). (**a**) Schematic diagram of modulation efficiency changing with etching depth and voltage. (**b**) Loss efficiency product changing with voltage and etching depth.

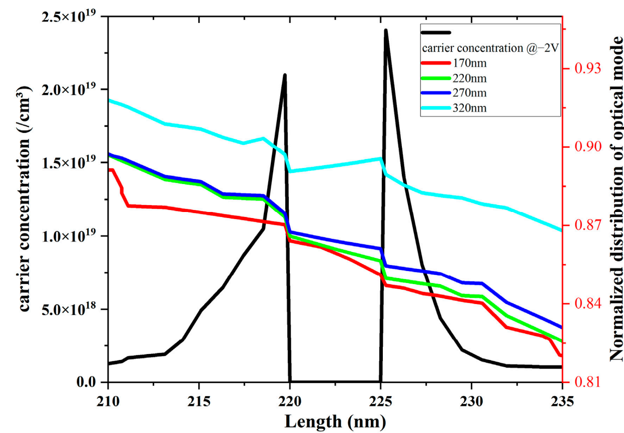

Figure 8. Schematic of overlapping normalized electric field intensity with carriers.

Another critical factor causing modulation performance variations is the thickness of the poly-Si. Here, changes in poly-Si thickness led to alterations in the thickness of the waveguide, which in turn impacted the central position of the optical field. Similar to the influence of the etching depth, this effect can be attributed to the degree of overlap between the center of the optical field and the region of the dense carrier accumulation. We conducted a performance scan on the modulator using a range of poly-Si thicknesses to elicit clear and intuitive conclusions. Since the initial poly-Si thickness was 150 nm, we set the scanning range from 120 to 200 nm. The outcomes of this scan are presented in Figure 9a,b.

Increasing the poly-Si thickness impacts modulation efficiency while concurrently decreasing the efficiency–loss product. As the poly-Si thickness increases, the normalized optical field strength on both sides of the dielectric layer also rises, thus, boosting the modulation efficiency. However, this increase in thickness has its constraints. Maintaining the overall polysilicon thickness below 220 nm is crucial to meet the single-mode optical transmission condition. Notably, and irrespective of the applied voltage, the trend toward a product with reduced efficiency–loss and increased polysilicon thickness remains consistent, providing a valuable guideline for our optimization design process.

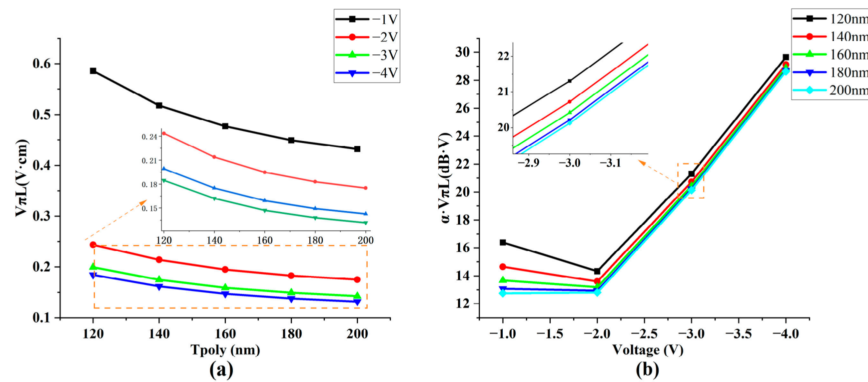

Figure 9. Schematic of performance with different poly-Si thicknesses (T poly). (**a**) Schematic diagram of modulation efficiency changing with poly-Si thickness (**b**) Efficiency–loss product changing with voltage and poly-Si thickness.

To more intuitively demonstrate the influence of geometric factors on modulation efficiency, we have developed optical field intensity diagrams under varied geometric scenarios, presented in Figure 10a,b. Indeed, Figure 10a illustrates the optical field intensity distribution for an etching depth of 155 nm and a polysilicon thickness of 150 nm. In this configuration, the central position of the optical field intensity is predominantly concentrated in the center of the monocrystalline silicon layer, considerably distant from the sides of the dielectric layer. Conversely, Figure 10b shows a noticeable upward shift in the central position of the optical field when the etching depth and the polysilicon thickness were increased to 370 nm and 200 nm, respectively. This shift increased the overlap with the dielectric layer's position, resulting in significantly higher modulation efficiency. These observations confirm our proposed hypothesis and underscore the crucial role of geometric modifications and the complex relationship between physical structure and functional efficacy in photonic devices.

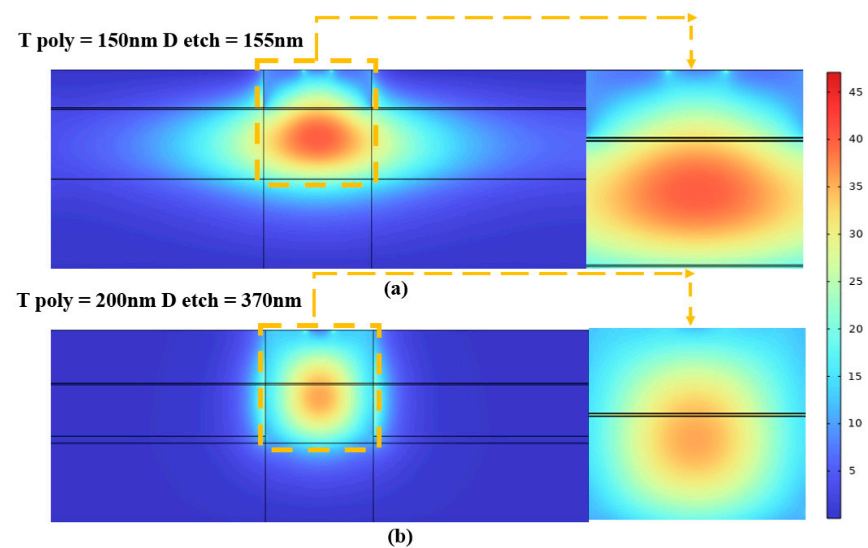

Figure 10. Schematic of optical field distribution under different geometric conditions (**a**) T poly = 150 nm, D etch = 155 nm and (**b**) T poly = 200 nm, D etch = 370 nm.

Building upon insights from our previous research, we redesigned and optimized the structure of our modulator. The outcomes of this re-simulation are depicted in Figure 11. After optimization, the modulator achieves its peak efficiency–loss product at a voltage of −1.2 V—registering a remarkable 6.1 dB·V. This peak corresponds to a modulation efficiency of 0.26 V·cm. It is important to note that these results specifically pertain to the efficiency–loss product. However, increasing the applied voltage is a viable strategy should

a higher modulation efficiency be the priority. For example, at −4 V, the modulator can surpass a modulation efficiency of 0.1 V·cm, attaining an impressive 0.096 V·cm.

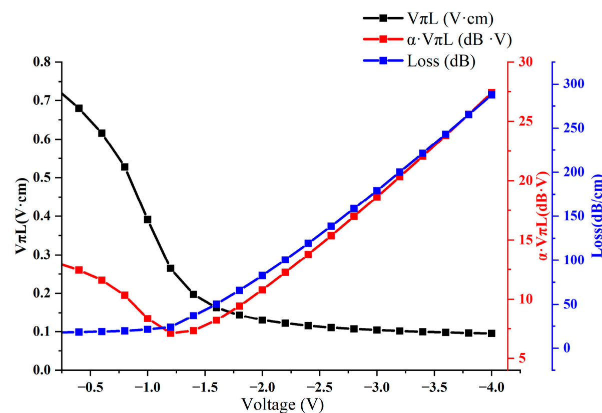

Figure 11. Schematic of modulator performance after optimization.

Nevertheless, a working voltage of −1.6 V appears optimal following a comprehensive evaluation. At this voltage, the modulator exhibits a modulation efficiency of 0.16 V·cm and a corresponding efficiency–loss product of 8.24 dB·V. This optimization process showcases the modulator's efficiency across different electrical conditions and underscores the critical need to balance the modulation efficiency and efficiency–loss product for optimal performance in practical applications.

Upon the foundation of our optimized structure, we conducted a comparative analysis of the simulation results for non-optimized structures using SiO_2 and ZrO_2 dielectric layers, as shown in Figure 12. The collected data distinctly highlights the advantages of using high-k (HK) materials in modulators. Whether considering modulation capability or efficiency–loss metrics, modulators employing ZrO_2, an HK material, consistently surpass those with traditional dielectric materials. Furthermore, the optimized structure demonstrates significant performance enhancements compared to the initial design. This improvement confirms the effectiveness of the structural optimization. In a side-by-side comparison using the same framework, our optimized structure, when contrasted with traditional SiO_2 dielectric layers, shows a clear and substantial increase in the simulation results. Both the efficiency–loss product and modulation efficiency increased by over 200%.

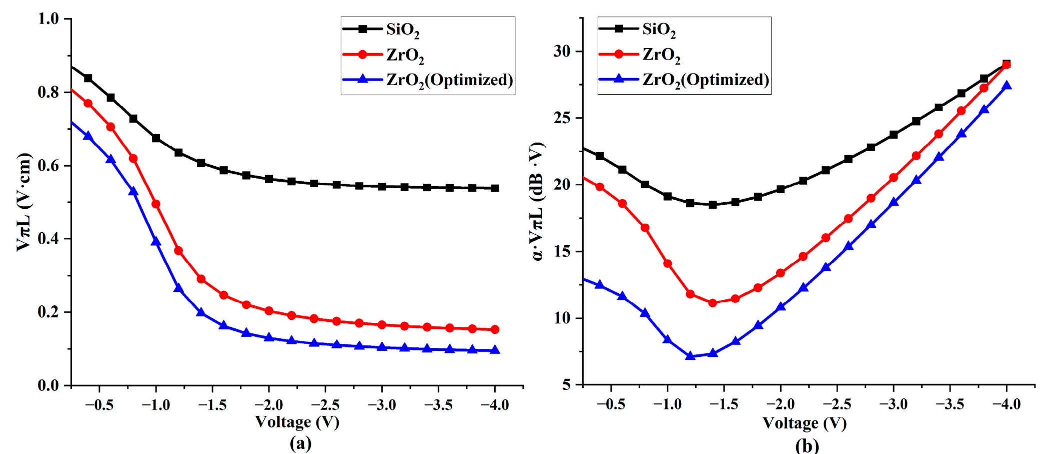

Figure 12. Comparison chart of modulator performances after optimization (**a**) Comparison chart of modulation efficiencies of different materials. (**b**) Comparison chart of efficiency–loss products using different materials.

One of the primary metrics for evaluating the efficiency of optical modulators is the phase shift length. Our study compared the phase shift lengths of optical modulators employing traditional SiO_2 dielectric layers, high-k (HK) material ZrO_2 dielectric layers, and optimized ZrO_2 dielectric layers through simulations. As depicted in Figure 13, the optical modulators with ZrO_2 dielectric layers demonstrate an approximate 200% improvement in phase shift length compared to those with traditional layers. Following the optimization of the device's geometric structure and doping, the phase shift length was further reduced based on these findings. Specifically, at a voltage of −1.4 V, the phase shift length was 1.14 mm, and at voltages below −1.6 V, it was less than 1 mm. This reduction in phase shift length contributes to greater integration, underscoring the benefits of using HK material ZrO_2 dielectric layers in optical modulators.

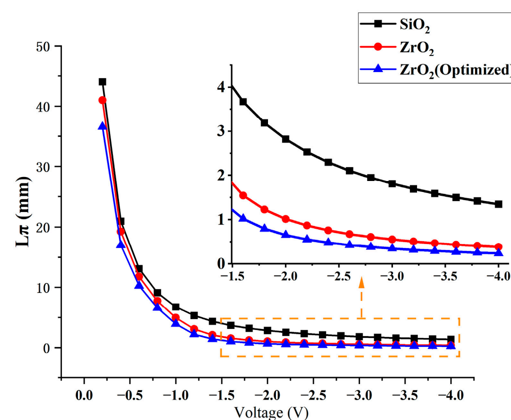

Figure 13. Schematic illustration of phase shift length variation with voltage.

In our final simulation, we assessed the leakage current and bandwidth of the optical modulators with optimized ZrO_2 dielectric layers. Figure 14a illustrates that the leakage current consistently stays below 7.6×10^{-5} A/cm^2 at voltages above −3.2 V. However, at voltages below −3.2 V, there is a marked increase in leakage current, culminating in a peak of 0.039 A/cm^2 at −4.0 V.

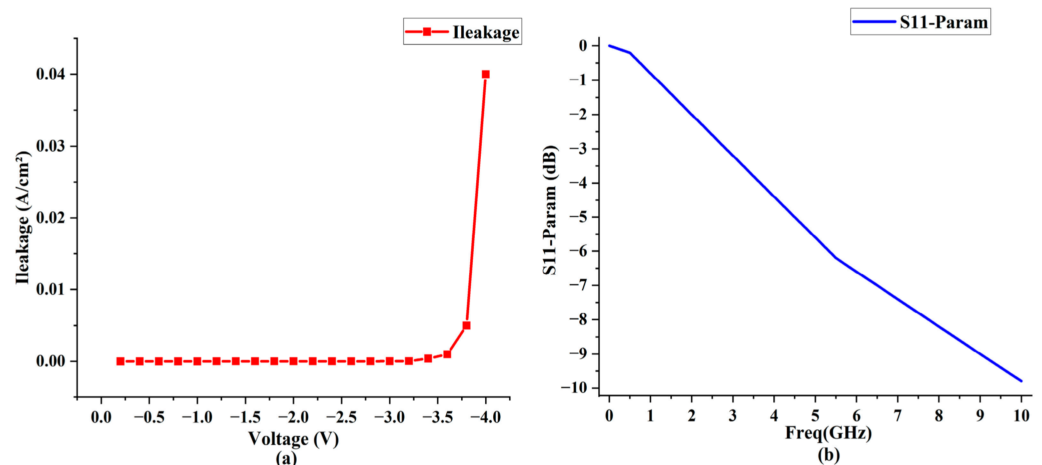

Figure 14. Simulation graphs of leakage current and bandwidth. (**a**) Schematic illustration of leakage current variation with voltage. (**b**) Schematic illustration of bandwidth based on -S11 parameter.

An analysis of the device's S11 parameter indicates a −3 dB bandwidth of 2.94 GHz, as depicted in Figure 14b. The utilization of high-k (HK) materials increases overall capacitance compared to traditional SiO_2 dielectric layers. Although the bandwidth of optical modulators using HK material dielectric layers still necessitates further optimization—especially when contrasted with traditional SiO_2 layer modulators, which can achieve

bandwidths exceeding 10 GHz—this aspect will be a primary focus in our future research endeavors.

4. Discussion

High-efficiency modulators often incorporate accumulation capacitors in their design. The capacity of the oxide layer to accumulate carriers is crucial in determining modulation efficiency. This efficiency is also influenced by the doping concentration, the modulator's geometry, and the applied voltage. Geometric factors are instrumental in dictating carrier accumulation and its interaction with the optical field distribution, which, in turn, impacts both modulation efficiency and losses. An increased overlap between these elements results in higher modulation efficiency, leading to more significant losses. On the other hand, a thicker oxide layer diminishes capacitance and carrier accumulation capability, which reduces modulation efficiency.

Regarding the effects of doping, modulation capability is closely linked to carrier concentration. However, N/P doping scenarios exhibit distinct behaviors. Hence, increasing doping concentrations in the N and P-type regions can enhance modulation efficiency, yet the resulting losses vary significantly. At equivalent doping concentrations, holes demonstrate more pronounced modulation efficiencies, leading to reduced losses and a lower efficiency–loss product. Thus, strategically employing holes as the primary modulation carriers is a crucial method for improving the efficiency–loss product.

This study suggests using a vertical structure capacitor modulator constructed with an innovative oxide layer material to achieve enhanced modulation efficiency and reduced efficiency–loss products, while also simplifying the manufacturing process. When focusing on a single performance goal, we can attain an ultra-low efficiency–loss product of 6.1 dB·V and an exceptional modulation efficiency of 0.096 V·cm. Nevertheless, this involves a trade-off with losses. The realized modulation efficiency is 0.16 V·cm, corresponding to an efficiency–loss product of 8.24 dB·V. A comparison with other silicon-based accumulation modulators is provided in Table 1.

Table 1. Performance parameters of accumulation modulators with different gate materials.

Gate Material	Oxide	$V\pi L$ (V·cm)	Loss (dB/cm)	$\alpha \cdot V\pi L$ (dB·V)	Result Type
ITO [23]	Al_2O_3	0.052	>1500	>80	Experimental
ITO [24]	Al_2O_3	0.095	16,000	152	Experimental
InGaAsP [25]	Al_2O_3	0.047	4.6	<1	Experimental
InP [26]	SiO_2/Al_2O_3	0.54	2.3	1.24	Experimental
Poly-Si [7]	SiO_2	1.8	>30	>48	Experimental
Poly-Si [29]	SiO_2	0.886	>18	>16	Numerical
Poly-Si [9]	SiO_2	0.2	65	13	Experimental
(This work) Poly-si	ZrO_2	0.16	50	8.24	Numerical

Compared to traditional SiO_2 dielectric layer capacitor structures, our modulator demonstrated significant advancements in modulation capabilities. Our approach has resulted in a 20% increase in modulation capacity and a notable 40% decrease in the efficiency–loss product, ultimately, outperforming the most advanced high-efficiency modulators currently available.

Our modulator also shows substantial improvements over alternative approaches, such as those using ITO gate materials. Specifically, we have achieved a significant reduction in modulation losses. Moreover, compared to III–V material modulators, our design eliminates the need for additional bonding processes, thereby simplifying the overall complexity of the manufacturing procedure. This advancement creates new possibilities for

future research and offers innovative solutions for achieving high-density, high-efficiency, and high-precision modulations.

5. Conclusions

This paper presents a high-density modulator based on a vertical structure incorporating CMOS-compatible high-k (HK) material dielectric layers, featuring an innovative accumulation structure using ZrO_2 oxide layers. Our simulations indicate that the modulator achieves a modulation efficiency of 0.16 V·cm in the vertical direction, with a corresponding loss-efficiency product of 8.24 dB·V. Further optimization of the voltage settings could lead to even more impressive modulation efficiency, potentially lowering the efficiency–loss product to 6.1 dB·V and fulfilling the requirements for high-precision, dense, and efficient modulations.

In summary, our research underscores the advantages of HK materials in constructing high-efficiency optical modulators. The significant benefits of utilizing high-k materials, such as ZrO_2, and structural optimization have opened new avenues for enhancing device performances. This breakthrough emphasizes the critical role of material selection and structural design in optimizing the optical modulator efficiency. It establishes a new standard in the field, fostering further research and innovation in photonic technology. This advancement heralds exciting prospects for developing more efficient, powerful, and versatile optical communication systems. However, further research is essential to evaluate its performance and explore its practical applications fully. Nevertheless, the outcomes of this research mark a significant step forward in devising innovative designs for high-efficiency optical modulators.

Author Contributions: Methodology, Y.C., X.Z., L.L., Y.L., Y.S., P.J. and Y.N.; Software, Z.L. and Y.W.; Validation, Y.X. and Y.Q.; Resources, Y.Z.; Writing—original draft, Z.Z.; Writing—review & editing, C.Q.; Supervision, L.Q.; Funding acquisition, L.W. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Key R & D Program of China [2022YFB2803500]; The National Natural Science Foundation of China [62090050, 62121005, 61934003, 62227819, 62090051]; The Science and Technology Development Project of Jilin Province [20210301016GX, 20230508097RC]; The National Key Scientific Instrument and Equipment Development Projects of China under grant No. 2021YFF0700500.

Data Availability Statement: The data presented in this study are available on the request from the corresponding author.

Conflicts of Interest: Author Yongyi Chen was employed by the company Jlight Semiconductor Technology Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

References

1. Luo, W.; Cao, L.; Shi, Y.; Wan, L.; Zhang, H.; Li, S.; Chen, G.; Li, Y.; Li, S.; Wang, Y. Recent progress in quantum photonic chips for quantum communication and internet. *Light Sci. Appl.* **2023**, *12*, 175. [CrossRef] [PubMed]
2. Chen, Z.; Segev, M. Highlighting photonics: Looking into the next decade. *ELight* **2021**, *1*, 2. [CrossRef]
3. Zhou, H.; Dong, J.; Cheng, J.; Dong, W.; Huang, C.; Shen, Y.; Zhang, Q.; Gu, M.; Qian, C.; Chen, H. Photonic matrix multiplication lights up photonic accelerator and beyond. *Light Sci. Appl.* **2022**, *11*, 30. [CrossRef] [PubMed]
4. Noguchi, K.; Mitomi, O.; Kawano, K.; Yanagibashi, M. Highly efficient 40-GHz bandwidth Ti: LiNbO/sub 3/optical modulator employing ridge structure. *IEEE Photonics Technol. Lett.* **1993**, *5*, 52–54. [CrossRef]
5. Amin, R.; Maiti, R.; George, J.K.; Ma, X.; Ma, Z.; Dalir, H.; Miscuglio, M.; Sorger, V.J. A lateral MOS-capacitor-enabled ITO Mach–Zehnder modulator for beam steering. *J. Light. Technol.* **2020**, *38*, 282–290. [CrossRef]
6. Zangeneh Kamali, K.; Xu, L.; Gagrani, N.; Tan, H.H.; Jagadish, C.; Miroshnichenko, A.; Neshev, D.; Rahmani, M. Electrically programmable solid-state metasurfaces via flash localised heating. *Light Sci. Appl.* **2023**, *12*, 40. [CrossRef] [PubMed]
7. Zhang, W.; Debnath, K.; Chen, B.; Li, K.; Liu, S.; Ebert, M.; Reynolds, J.D.; Khokhar, A.Z.; Littlejohns, C.; Byers, J. High bandwidth capacitance efficient silicon MOS modulator. *J. Light. Technol.* **2021**, *39*, 201–207. [CrossRef]
8. Hanim, A.; Mardiana, B.; Hazura, H.; Saari, S. On the modulation phase efficiency of a silicon pin diode optical modulator. In Proceedings of the International Conference On Photonics 2010, Langkawi, Malaysia, 5–7 July 2010; pp. 1–3. [CrossRef]

9. Webster, M.; Gothoskar, P.; Patel, V.; Piede, D.; Anderson, S.; Tummidi, R.; Adams, D.; Appel, C.; Metz, P.; Sunder, S. An efficient MOS-capacitor based silicon modulator and CMOS drivers for optical transmitters. In Proceedings of the 11th International Conference on Group IV Photonics (GFP), Paris, France, 27–29 August 2014; pp. 1–2.
10. Yang, Y.; Fang, Q.; Yu, M.; Tu, X.; Rusli, R.; Lo, G.-Q. High-efficiency Si optical modulator using Cu travelling-wave electrode. *Optics Express* **2014**, *22*, 29978–29985. [CrossRef]
11. Fujikata, J.; Ushida, J.; Ming-Bin, Y.; ShiYang, Z.; Liang, D.; Guo-Qiang, P.L.; Kwong, D.-L.; Nakamura, T. 25 GHz operation of silicon optical modulator with projection MOS structure. In Proceedings of the Optical Fiber Communication Conference, San Diego, CA, USA, 21–25 March 2010. p. OMI3.
12. Liu, A.; Jones, R.; Liao, L.; Samara-Rubio, D.; Rubin, D.; Cohen, O.; Nicolaescu, R.; Paniccia, M. A high-speed silicon optical modulator based on a metal–oxide–semiconductor capacitor. *Nature* **2004**, *427*, 615–618. [CrossRef]
13. Debnath, K.; Thomson, D.J.; Zhang, W.; Khokhar, A.Z.; Littlejohns, C.; Byers, J.; Mastronardi, L.; Husain, M.K.; Ibukuro, K.; Gardes, F.Y. All-silicon carrier accumulation modulator based on a lateral metal-oxide-semiconductor capacitor. *Photonics Res.* **2018**, *6*, 373–379. [CrossRef]
14. Liu, J.; Li, J.; Wu, J.; Sun, J. Structure and dielectric property of high-k ZrO_2 films grown by atomic layer deposition using tetrakis (dimethylamido) zirconium and ozone. *Nanoscale Res. Lett.* **2019**, *14*, 1–12. [CrossRef] [PubMed]
15. Li, Y.; Tang, X.; Xu, G.; Li, H.; He, S.; Hu, X.; Su, X.; Bai, W.; Lu, D.; Long, S. The Effects of Postdeposition Anneal and Postmetallization Anneal on Electrical Properties of $TiN/ZrO_2/TiN$ Capacitors. *IEEE Trans. Electron Devices* **2022**, *70*, 59–64. [CrossRef]
16. Deshmane, V.G.; Adewuyi, Y.G. Synthesis of thermally stable, high surface area, nanocrystalline mesoporous tetragonal zirconium dioxide (ZrO_2): Effects of different process parameters. *Microporous Mesoporous Mater.* **2012**, *148*, 88–100. [CrossRef]
17. Robertson, J.; Wallace, R.M. High-K materials and metal gates for CMOS applications. *Mater. Sci. Eng. R Rep.* **2015**, *88*, 1–41. [CrossRef]
18. Manipatruni, S.; Xu, Q.; Schmidt, B.; Shakya, J.; Lipson, M. High speed carrier injection 18 Gb/s silicon micro-ring electro-optic modulator. In Proceedings of the LEOS 2007-IEEE Lasers and Electro-Optics Society Annual Meeting Conference Proceedings, Lake Buena Vista, FL, USA, 21–25 October 2007; pp. 537–538. [CrossRef]
19. Wang, J.; Qiu, C.; Li, H.; Ling, W.; Li, L.; Pang, A.; Sheng, Z.; Wu, A.; Wang, X.; Zou, S. Optimization and demonstration of a large-bandwidth carrier-depletion silicon optical modulator. *J. Light. Technol.* **2013**, *31*, 4119–4125. [CrossRef]
20. Félix Rosa, M.; Rathgeber, L.; Elster, R.; Hoppe, N.; Föhn, T.; Schmidt, M.; Vogel, W.; Berroth, M. Design of a carrier-depletion Mach-Zehnder modulator in 250 nm silicon-on-insulator technology. *Adv. Radio Sci.* **2017**, *15*, 269–281. [CrossRef]
21. Marpaung, D.; Yao, J.; Capmany, J. Integrated microwave photonics. *Nat. Photonics* **2019**, *13*, 80–90. [CrossRef]
22. Soref, R.; Bennett, B. Electrooptical effects in silicon. *IEEE J. Quantum Electron.* **1987**, *23*, 123–129. [CrossRef]
23. Amin, R.; Maiti, R.; Carfano, C.; Ma, Z.; Tahersima, M.H.; Lilach, Y.; Ratnayake, D.; Dalir, H.; Sorger, V.J. 0.52 V mm ITO-based Mach-Zehnder modulator in silicon photonics. *APL Photonics* **2018**, *3*, 126104. [CrossRef]
24. Amin, R.; Maiti, R.; Gui, Y.; Suer, C.; Miscuglio, M.; Heidari, E.; Chen, R.T.; Dalir, H.; Sorger, V.J. Sub-wavelength GHz-fast broadband ITO Mach–Zehnder modulator on silicon photonics. *Optica* **2020**, *7*, 333–335. [CrossRef]
25. Han, J.-H.; Boeuf, F.; Fujikata, J.; Takahashi, S.; Takagi, S.; Takenaka, M. Efficient low-loss InGaAsP/Si hybrid MOS optical modulator. *Nat. Photonics* **2017**, *11*, 486–490. [CrossRef]
26. Ohno, S.; Li, Q.; Sekine, N.; Fujikata, J.; Noguchi, M.; Takahashi, S.; Toprasertpong, K.; Takagi, S.; Takenaka, M. Taperless Si hybrid optical phase shifter based on a metal-oxide-semiconductor capacitor using an ultrathin InP membrane. *Optics Express* **2020**, *28*, 35663–35673. [CrossRef] [PubMed]
27. Kononchuk, O.; Nguyen, B.-Y. *Silicon-on-Insulator (Soi) Technology: Manufacture and Applications*; Elsevier: Amsterdam, The Netherlands, 2014.
28. Witzens, J. High-speed silicon photonics modulators. *Proc. IEEE* **2018**, *106*, 2158–2182. [CrossRef]
29. Passaro, V.M.; Dell'Olio, F. Scaling and optimization of MOS optical modulators in nanometer SOI waveguides. *IEEE Trans. Nanotechnol.* **2008**, *7*, 401–408. [CrossRef]

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