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Low Conducted-EMI Single-Phase Boost PFC with Sliding Frequency Modulation

Zhansen Akhmetov,
Electrical & Computer Engineering, Department North Carolina State University, Raleigh, USA

Muhammad Abdelraziq,
Electrical & Computer Engineering, Department North Carolina State University, Raleigh, USA

Zeljko Pantic
Electrical & Computer Engineering, Department North Carolina State University, Raleigh, USA

Abstract

A boost Power Factor Correction (PFC) circuit is connected between the AC grid and converters to meet Electromagnetic Interference (EMI) and Total Harmonic Distortion (THD) standards. An EMI filter should be utilized at the input of the PFC to attenuate high-frequency noise injected into the grid. This article discusses the low-conducted EM emission boost PFC with Sliding Frequency Modulation (SFM) proposed by *Power Integrations*. The proposed boost PFC is compared with a conventional boost PFC operated using Constant Frequency Modulation (CFM) at 120 kHz. Both PFCs are rated for the same nominal power (i.e., 300 W) and output voltage (i.e., 383 V). An analytical loss model is also developed to compare the performance of the SFM and CFM PFCs. The analytical findings are verified by means of simulations and experiments.

Keywords

Boost Power Factor Correction Circuit; Electromagnetic Interference; Conducted EMI; Sliding Frequency Modulation; Power Loss; Efficiency; Total Harmonic Distortion

I. Introduction

Power electronics systems connected to the grid must meet the CISPR 22, and the IEEE 519 standards to keep current harmonics below the specified levels [1, 2]. The CISPR 22 standard determines the EMI noise levels produced by electronics, while the IEEE 519 standard establishes the maximum Total Harmonic Distortion (THD) levels. Both EMI and THD are caused by the harmonic content of the converters' input current. Boost Power Factor Correction (PFC) converters and input EMI filters are employed to ensure the Power Factor (PF) is close to unity, and the harmonic content meets the standards. A typical single-phase boost PFC circuit is shown in Fig. 1 and discussed comprehensively in [3]-[7]. There are different EMI filter designs to reduce high-frequency noise; however, all of them are the result of a tradeoff between size and filtering ability. The authors in [7]

zakhmet@ncsu.edu .

propose an optimized EMI filter design procedure for the boost PFC circuit. However, since conventional boost PFCs operate with a Constant Frequency Modulation (CFM) of up to 150 kHz, their efficiency is considerably reduced at light loads due to switching losses. Changing the frequency modulation of the boost PFC from CFM to Sliding Frequency Modulation (SFM) can increase efficiency without redesigning the circuit. The proposed boost PFC circuit with SFM mentioned in [8] improves the efficiency and meets the CISPR 22 and IEEE 519 standards without additional hardware changes.

In this paper, an SFM boost PFC circuit is analyzed, experimentally tested, and compared with the CFM boost PFC. Section II discusses the basic circuit and key parameters of the boost PFC and introduces the SFM technique. In Section III, analytical power loss analysis is performed to compare the power losses in CFM and SFM PFCs with the same hardware components. Additionally, the CFM and SFM PFCs are experimentally compared in terms of their EMI, THD, and efficiency measurements in Section IV. Finally, future work and conclusions are presented in Section V.

II. Description of the PFC Converter Circuit

This section describes the basic circuit parameters of the CFM and SFM boost PFC converters. Both PFC converters have the same main power stage and input EMI filters. However, the two PFCs differ in terms of their control techniques and switching frequencies. While the CFM PFC operates at a constant 120 kHz, the SFM PFC operates in a spanning range of 22~123 kHz.

A. Main Power Stage of a Boost PFC converter

The main power stage of a boost PFC comprises an input filter, a rectifier, and a boost converter, as shown in Fig. 1. The overall design was adopted from the UCC28189EVM-573 PFC prototype with CFM designed by Texas Instruments (TI). However, minor changes in the boost inductor value L and EMI filter components are introduced and discussed below. The final circuit parameters are shown in Table 1.

To decrease the current ripple and improve efficiency, the new inductor was designed with an increased self-inductance of 410 μH instead of the previous 327 μH on TI PFC. Assuming that the core loss is proportional to $\sim I^2$, the overall power loss in the inductor can be described by its resistance. The frequency sweep of the inductor resistance is performed using the Hioki IM3536 LCR meter. The measured resistance vs. frequency characteristic of the inductor can be expressed by:

$$r_{LHF}(f) = 2.796 \cdot 10^{-11} f^2 - 5.069 \cdot 10^{-8} f + 0.2297 \quad (1)$$

where f is the frequency of the inductor's excitation current. (1) is valid for frequency within the 10–145 kHz range. Further, the inductor resistance at 60 Hz r_{L60} is 29.8 mΩ.

The input EMI filter used in this converter is a one-stage filter that consists of a Common Mode (CM) filter and a Differential Mode (DM) filter. The CM filter components are the choke inductor L_1 and capacitors C_3 and C_4. On the other hand, the leakage inductance L_{leak} of the choke inductor and capacitors C_1 and C_2 make up the DM filter. To reduce the CM noise, the choke inductor L_1 value in the TI PFC is increased. Instead of the original choke inductor 8113-RC Bourns with 5mH, the 8112-RC Bourns with 8mH is used. With the change of the choke inductor, there is a change in L_{leak} from 25 μH to 38 μH that affects the DM filter performance. However, to keep the DM mode filter cut-off frequency the same, the C_1 and C_2 capacitance values are decreased from the original 0.47 μF used in the TI PFC to 0.33 μF. Thus, the DM filter cut-off frequency changed slightly from 46.43 kHz to 44.94 kHz.

B. Sliding Frequency Modulation

In SFM PFCs, the switching frequency varies over the line frequency (i.e., 60 Hz) half-cycle, typically spanning a range of 22~123 kHz when operating in CCM [8]. Fig. 2 illustrates the spread frequency modulation at 300 W load for the HiperPFS-4 PFC family mentioned in [8]. This type of frequency variation decreases switching losses at low currents by decreasing the switching frequency. Moreover, the peak frequency of the SFM decreases with the decrease in the load [8]. Thus, SFM modulation varies not only over the line frequency but also over the load. However, to be used in further analysis, the SFM line from the datasheet at 300 W load is approximated by:

$$f_s = 25000 + 90000\left|\sin(2\pi f_{grid} t)\right| \tag{2}$$

where f_{grid} is the 60-Hz frequency of the grid. The approximated SFM is given by the dashed line in Fig. 2.

III. Analytical Study of the Efficiency

An analytical study of the power dissipated in the boost inductor L, boost diode D_1, and switch Q_1 is performed in this section. These are the main elements whose power losses are affected by the PFC switching frequency. High-frequency ripples do not affect the power losses in elements like the rectifier, output capacitor C_{DC}, and EMI filter. Thus, for the same power, they are considered the same for the CFM and SFM PFCs.

All the calculations are performed for the rated power (i.e, 300 W) where the PFCs operate in the Continuous Conduction Mode (CCM). Critical waveforms of the boost PFC operating in CCM are given in Fig. 3. The overall hardware parts for both PFCs are the same. However, the model of the switch installed in the SFM PFC module cannot be identified. Thus, to provide a valid comparison, analytical analysis is performed for the SPP20N60C3 switch used by the CFM PFC board for both boards.

A. Conduction Losses

All three elements L, D_1, and Q_1 dissipate power in the form of conduction losses. However, due to the change in resistance with frequency, the inductor losses consist of lowfrequency and high-frequency conduction losses. The inductor loss in the switching period T_s can be written as:

$$P_{L,T_s} = I_{L,avg}^2 r_{L60} + I_{LHF,rms}^2 r_{LHF} \tag{3}$$

where $I_{L,avg}$ is the instantaneous value of the line AC current, $I_{LHF,rms}$ is the RMS value of the first harmonic of the current ripple, r_{L60} is the resistance of L at 60 Hz, and r_{LHF} is the resistance of L at higher frequencies given by (1). The input current through the inductor is calculated as:

$$I_{L,avg}\left(t\right) = \frac{\sqrt{2}P_{out}}{\eta V_{in,rms} PF}\left|\sin(2\pi f_{grid} t)\right| \tag{4}$$

where PF is a power factor taken as 1, and η is the efficiency taken as 0.95 based on experimental measurements. For the boost inductor current ripple, the RMS of the first harmonic is considered, while higher harmonic currents are neglected. The RMS of the first harmonic from the asymmetric triangular waveform can be found as follows [9]:

$$I_{LHF,rms} = \frac{\sqrt{2}\sin\left[\left(1-D\right)\pi\right]}{\left(D-D^2\right)\pi^2}\Delta i \tag{5}$$

where D is the duty cycle that changes with time, and Δi is the current ripple amplitude. The duty cycle formula for the boost converter is [10]:

$$D = \frac{V_{out} - V_{in}\left|\sin(2\pi f_{grid} t)\right|}{V_{out}} \tag{6}$$

From Fig. 3, the current ripple amplitude is [10]:

$$\Delta i = \frac{V_{in}\left|\sin(2\pi f_{grid} t)\right|}{2L} D T_s \tag{7}$$

Substituting (5), (6), and (7), the following is obtained:

$$I_{LHF,rms} = \frac{V_{out}\sin\left(\frac{V_{in}\left|\sin(2\pi f_{grid}t)\right|}{V_{out}}\pi\right)}{\sqrt{2}Lf_s\pi^2} \tag{8}$$

It should be noted that the high-frequency current value is inversely proportional to switching frequency f_s, while the low-frequency part is not affected by f_s. Further, to find the average conduction loss of the inductor, (3) is integrated over a quarter of the period T_{grid} as:

$$P_L = \frac{4}{T_{grid}}\int_0^{T_{grid}/4}\left(I_{L,avg}^2 r_{L60} + I_{LHF,rms}^2 r_{LHF}\right)dt \tag{9}$$

Eq. (9) is numerically solved for CFM with constant f_s and SFM with variable f_s described by (2). The results in Table 2 show that the PFC module with SFM creates 9.3% more inductor losses compared to the CFM.

Further, the conduction losses of the boost diode D_1 are considered. The diode used in both PFC boards is SiC Schottky Diode C3D04060A, with negligible reverse recovery and switching loss. The formula of the diode conduction losses over a period T_s is:

$$P_{D,T_s} = I_{D,avg}V_D + I_{D,rms}^2 R_D \tag{10}$$

where $V_D = 0.83$ V, $R_D = 111.6$ mΩ at a junction temperature of 75◦C from the datasheet. It should be noted that the average current through the diode is the same in both cases; however, the current RMS values are different. Considering the waveform in Fig. 3, the RMS current through the diode is given by (11), and the average current is given by (12) [10].

$$I_{D,rms} = I_{L,avg}\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I_{L,avg}}\right)^2} \tag{11}$$

$$I_{D,avg} = (1-D)I_{L,avg} \tag{12}$$

Further, to find the conduction losses in the diode, (10) is integrated over a quarter of the period as shown:

$$P_D = \frac{4}{T_{grid}} \int_0^{T_{grid}/4} \left(I_{D,avg} V_D + I_{D,rms}^2 R_D \right) dt \tag{13}$$

Since all the parameters change with time, integral (13) cannot be solved analytically. Thus, all the results are generated by solving (13) numerically, and they are given in Table 2. The results show that the PFC module with SFM creates 0.4% more diode conduction losses compared to the CFM PFC.

The conduction loss of the switch Q_1 is determined by $r_{ds,on}$. The SPP20N60C3 switch with $r_{ds,on} = 0.24\Omega$ at a junction temperature of 75°C is assumed to be used in both PFC boards. The conduction losses in a period T_s are calculated as follows:

$$P_{QC,T_s} = I_{Q,rms}^2 r_{ds,on} \tag{14}$$

where $I_{Q,rms}$ is the RMS value of the current through the switch. Considering the waveform in Fig. 3, the RMS current through the switch is given as [10]:

$$I_{Q,rms} = I_{L,avg} \sqrt{D} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i}{I_{L,avg}} \right)^2} \tag{15}$$

Further, to find the conduction loss in the switch, (14) should be integrated over a quarter of the period as shown:

$$P_{QC} = \frac{4}{T_{grid}} \int_0^{T_{grid}/4} I_{Q,rms}^2 r_{ds,on} dt \tag{16}$$

All the results are generated by numerically solving (16) and are given in Table 2. The results show that the PFC module with SFM creates 2.66% more conduction loss in the switch compared to the CFM PFC. In total, the SFM PFC has 62.5 mW or 2.64% more conduction loss than the CFM PFC due to the increased current ripples. This change in the conduction loss has a negligible effect on the overall system efficiency.

B. Switching Losses

The reverse recovery losses are eliminated by employing a Schottky diode, while the gate losses are neglected. The dominating switching loss components of Q_1 are the output capacitance C_{oss} charging-discharging losses P_{QCoss}, and turn-on-off losses $P_{Qon\text{-}off}$. Also, there is a diode capacitor charging and discharging losses P_{DCO}.

P_{QCoss} is the loss during the charging and discharging of the C_{oss} capacitor of the MOSFET. Due to the non-linear nature of C_{oss}, the capacitor charging and discharging power loss in a period T_s is calculated as follows:

$$P_{QCoss,T_s} = f_s W_{Coss,T_s} = f_s V_{out} \int_0^{V_{out}} C_{oss}(V_{ds}) dV_{ds} \tag{17}$$

where $C_{oss}(V_{ds})$ is the small-signal C_{oss} versus drain to source voltage V_{ds}. The equation of $C_{oss}(V_{ds})$ is found by curve fitting the datasheet values and given as:

$$C_{oss}(V_{ds}) = 65.72 + 5781 \cdot e^{-0.07341 V_{ds}} \text{pF} \tag{18}$$

Further, to calculate the average loss, (17) is integrated over a quarter of the period as shown:

$$P_{QCoss} = \frac{4}{T_{grid}} \int_0^{T_{grid}/4} f_s W_{Coss,T_s} dt \tag{19}$$

The integral in (19) is numerically solved for CFM and SFM PFCs, and the results are shown in Table 2. The Boost PFC with SFM demonstrates 1.5 W or 31.41% improvement in P_{QCoss} compared to CFM.

The turn-on and turn-off losses of the MOSFET in a period T_s are calculated as:

$$P_{Qon-off,T_s} = f_s(E_{onQ} + E_{offQ}) \tag{20}$$

where turn-on energy is given by [11]:

$$E_{onQ} = V_{out}(I_{L,avg} - \Delta i)\frac{t_{r,I} + t_{f,V}}{2} \tag{21}$$

The current rise time $t_{r,I}$ is given in the datasheet as 5 ns, while the voltage fall time $t_{f,V}$ is calculated as [11]:

$$t_{f,V} = (V_{out} - (I_{L,avg} - \Delta i) r_{ds,\,\text{on}}) R_G \frac{(C_{GD1} + C_{GD2})}{2(V_{Dr} - V_{plateau})} \tag{22}$$

where $R_G = 3.3\Omega$ is the gate resistance, $V_{Dr} = 15.2$ V is the driver voltage, and $V_{plateau} = 5.5$ V is the gate plateau voltage. The gate-drain capacitances C_{GD1} and C_{GD2} are given by (23) and (24):

$$C_{GD1} = C_{rss}(V_{out}) \tag{23}$$

$$C_{GD2} = C_{rss}((I_{L,avg} - \Delta i) r_{ds,on}) \tag{24}$$

where C_{rss} from the datasheet can be expressed by:

$$C_{rss}(V_{DS}) = 14.47 + 1010e^{-0.2039 \cdot V_{DS}}\text{pF} \tag{25}$$

The turn-off energy is given by [11]:

$$E_{ofQ} = V_{out} \cdot (I_{L,avg} + \Delta i) \cdot \frac{t_{r,V} + t_{f,I}}{2} \tag{26}$$

where the current fall time $t_{f,I}$ is given in the datasheet as 4.5 ns, while voltage rise time $t_{r,V}$ is given by [11]:

$$t_{r,V} = (V_{out} - (I_{L,avg} + \Delta i) r_{ds,on}) R_G \frac{(C_{GD1} + C_{GD2,r})}{2(V_{Dr} - V_{plateau})} \tag{27}$$

The gate-drain capacitance $C_{GD2,r}$ sees the different voltage and is given by:

$$C_{GD2,r} = C_{rss}((I_{L,avg} + \Delta i) r_{ds,on}) \tag{28}$$

Finally, to find $P_{Qon-off,}$, (20) should be integrated over a quarter of the period as shown:

$$P_{Qon-off,s} = \frac{4}{T_{grid}} \int_0^{T_{grid}/4} \frac{E_{onQ} + E_{ofQ}}{T_s} dt \tag{29}$$

Expression (29) is numerically solved for CFM and SFM PFCs, and the results are given in Table 2. The Boost PFC with SFM shows 1.693 W or 21.47% improvement in the

turn-on and turn-off losses. Lastly, the diode junction capacitance losses due to charging and discharging are calculated. Due to the non-linear nature of diode capacitor C_o, the power loss P_{DCo} in a period T_s is calculated as follows:

$$P_{DCo,T_s} = f_s W_{DCo,T_s} = f_s V_{out} \int_0^{V_{out}} C_o(V_R) dV_R \tag{30}$$

where $C_o(V_R)$ is the small-signal C_o versus diode reverse voltage V_R. The equation of $C_o(V_R)$ is found by curve fitting the datasheet values and given as:

$$C_o(V_R) = \frac{253.5}{(1 + V_R/0.7)^{0.4332}} \text{pF} \tag{31}$$

Further, to calculate the average loss, (30) is integrated over a quarter of the period as shown:

$$P_{DCo} = \frac{4}{T_{grid}} \int_0^{T_{grid}/4} f_s W_{DCo,T_s} dt \tag{32}$$

The integral in (32) is numerically solved for CFM and SFM PFCs, and the results are shown in Table 2. The Boost PFC with SFM demonstrates 1.5 W or 31.41% improvement in P_{QCoss} compared to CFM. The Boost PFC with SFM shows 0.157 W or 31.41% improvement in P_{DCo}.

Thus, there is a 3.35 W switching loss improvement due to SFM. This represents a 1.12% overall efficiency improvement. Moreover, with the decrease in the load, the effect of the switching losses on efficiency becomes considerable. Thus, at lower loads, there can be up to a 5% improvement in efficiency due to SFM.

IV. Experimental Results on EMI, THD, and Efficiency of the Converters

This section provides the experimental results to compare the CFM and SFM boost PFC converters. The main parameters that are compared are EMI, THD, and the efficiency of the converters at different loads. It should be noted that all hardware parts for both PFCs are the same except the switch Q_1. The comparison of the main parameters of the two switches is given in Table 3. However, most of the important parameters are not found in the datasheet of the PFS7628H module.

A. EMI measurement

The experimental setup to measure the EMI noise according to CISPR 25 standard is given in Fig. 4. The Equipment Under Test (EUT) is placed on the table with a Line Impedance Stabilization Network (LISN) at a certain distance from other electronics. The Rohde Schwarz FSL spectrum analyzer is used with a measurement range from 9 kHz to 3 GHz. The analyzer measures the quasi-peak value of the noise, and it is compared to the limit set by CISPR 22 for Class B devices.

The conducted EMI of both boost PFC converters was measured without an EMI filter and with an EMI filter. Fig. 5 shows the conducted EMI of boost PFC converters without an EMI filter. The boost PFC with CFM fails to meet the CISPR 22 limit in the range from 240 kHz to 440 kHz, which is the second and third harmonics of the switching frequency of 120 kHz. However, the SFM PFC meets the CISPR 22 limit even without an input EMI filter. Moreover, it should be noted that the SFM PFC has a significantly lower EMI at higher frequencies above 3 MHz compared to CFM PFC. With the addition of the EMI filter, both CFM and SFM boost PFC converters meet the CISPR 22 standard with a considerable safety margin.

B. Efficiency and THD measurement

The efficiency and THD measurements are performed using a Yokogawa WT3000 power analyzer. The power analyzer is connected to the input of the boost PFC to measure the input power and THD, while the output power is adjusted by the electronic load at the output. Fig. 7 shows the efficiency with respect to the output power of both boost PFC converters. The boost PFC shows an improved efficiency for all output power ranges. It should be noted that the improvement in efficiency at 300 W power is 1.13%, which is very close to the analytically calculated improvement of 1.12%.

On the other hand, the THD for boost PFC converter with SFM is worse at low power compared to conventional boost PFC, as shown in Fig. 8. However, at higher power, it becomes better and reaches 3.73%, which is lower than the limit noted in IEEE 519 standard of 5%.

V. Conclusion

The proposed SFM boost PFC was analyzed in terms of efficiency, EMI noise, and THD. It is proven analytically and experimentally that the efficiency of the proposed converter improves by 1–5% in all loading conditions compared to the conventional CFM PFC with the same hardware parts. Moreover, the proposed SFM PFC meets EMI noise and THD standards. In the future, the proposed SFM technique can be optimized for better efficiency and noise performance.

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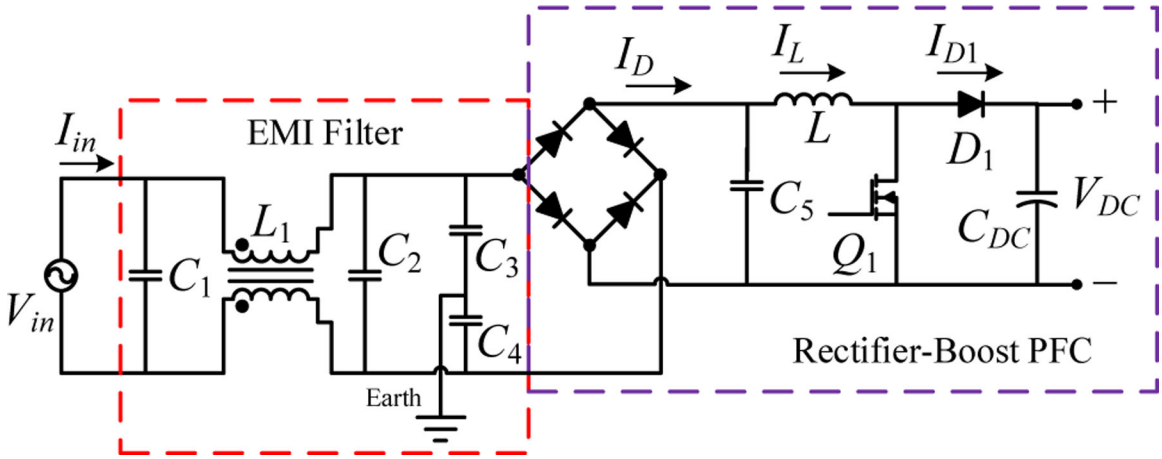

Fig. 1.
Boost PFC converter with an input EMI filter.

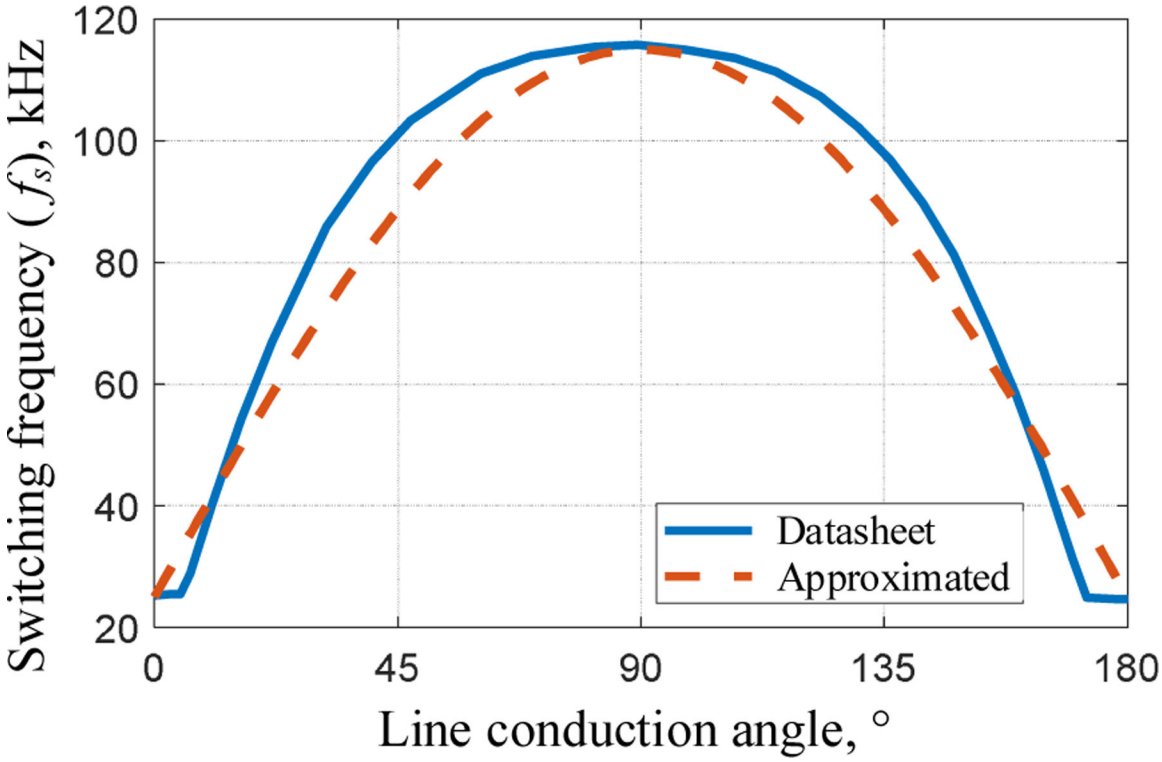

Fig. 2.
Sliding frequency modulation at 300 W of the proposed boost PFC circuit used by *Power Integrations* [8].

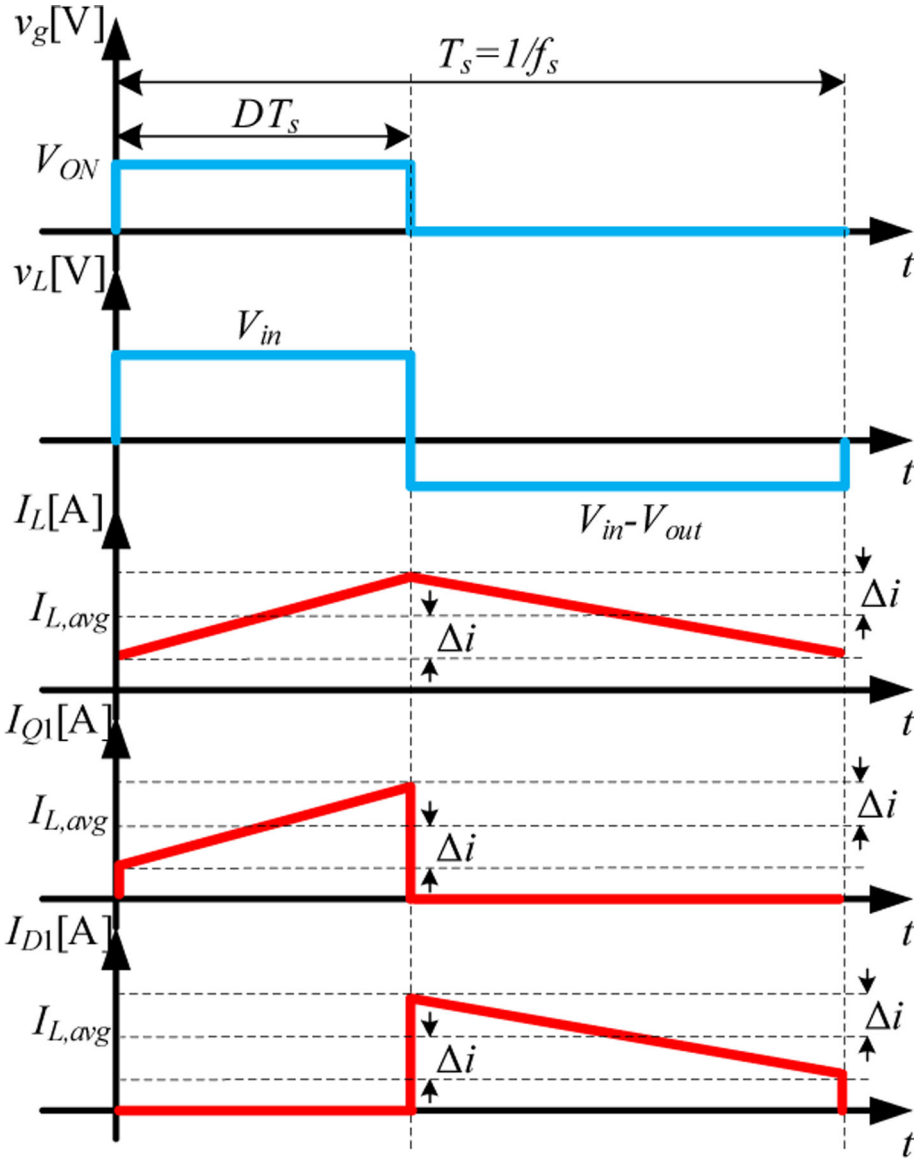

Fig. 3.
Waveforms of the boost PFC for CCM operation.

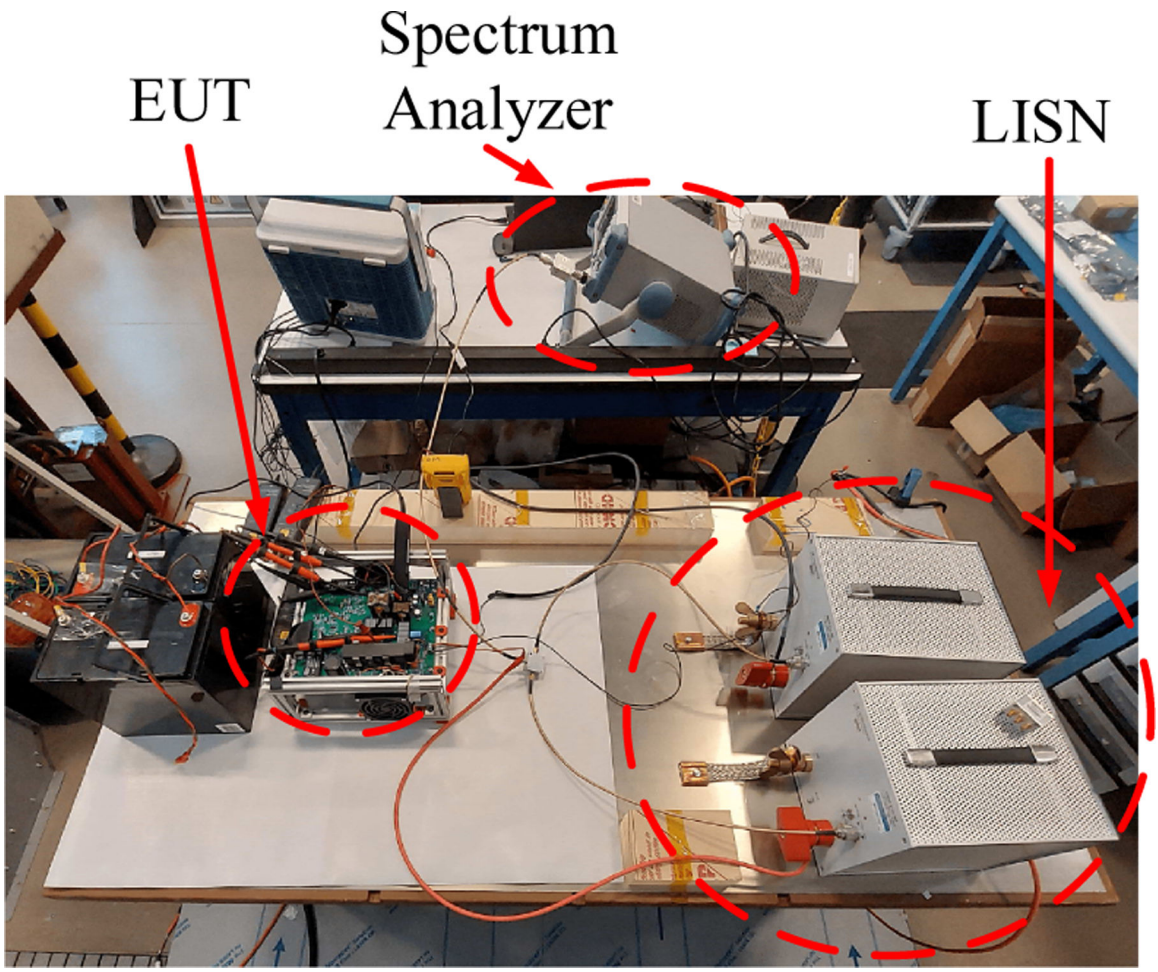

Fig. 4.
Experimental setup for measuring the EMI noise according to CISPR 25 standard.

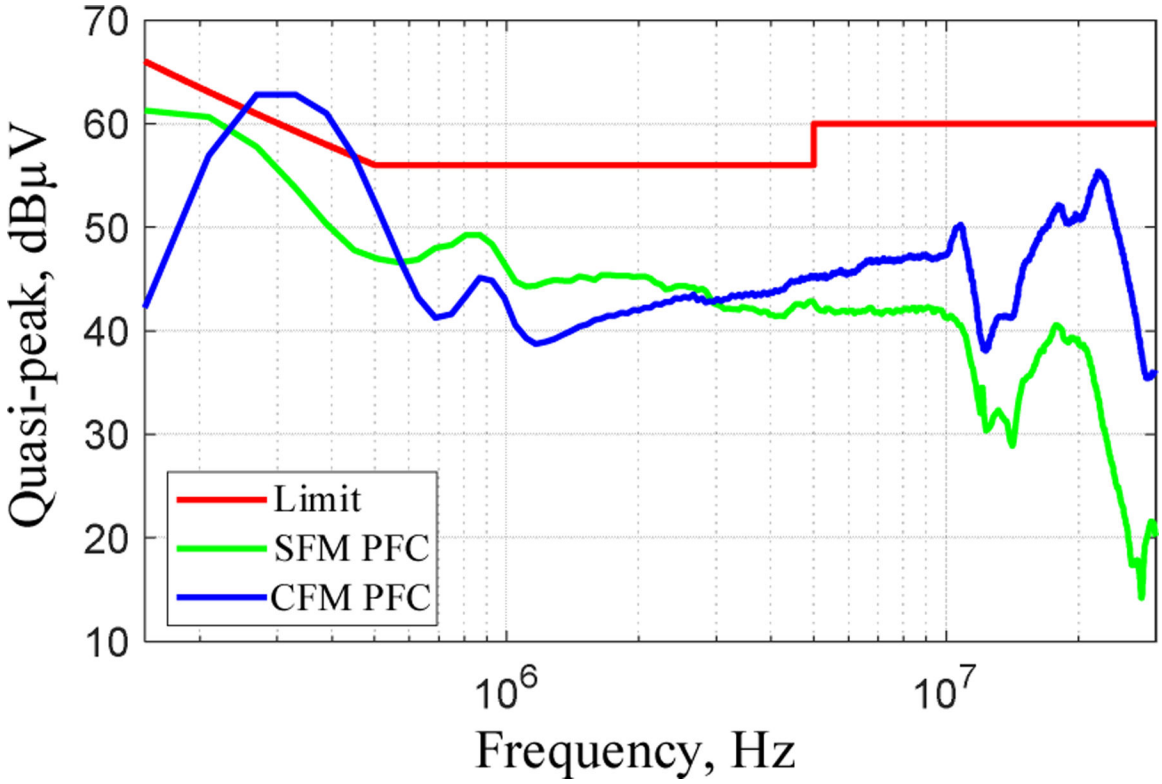

Fig. 5.
Measured conducted-EMI noise of the boost PFC with CFM and SFM at 250 W power without an EMI filter.

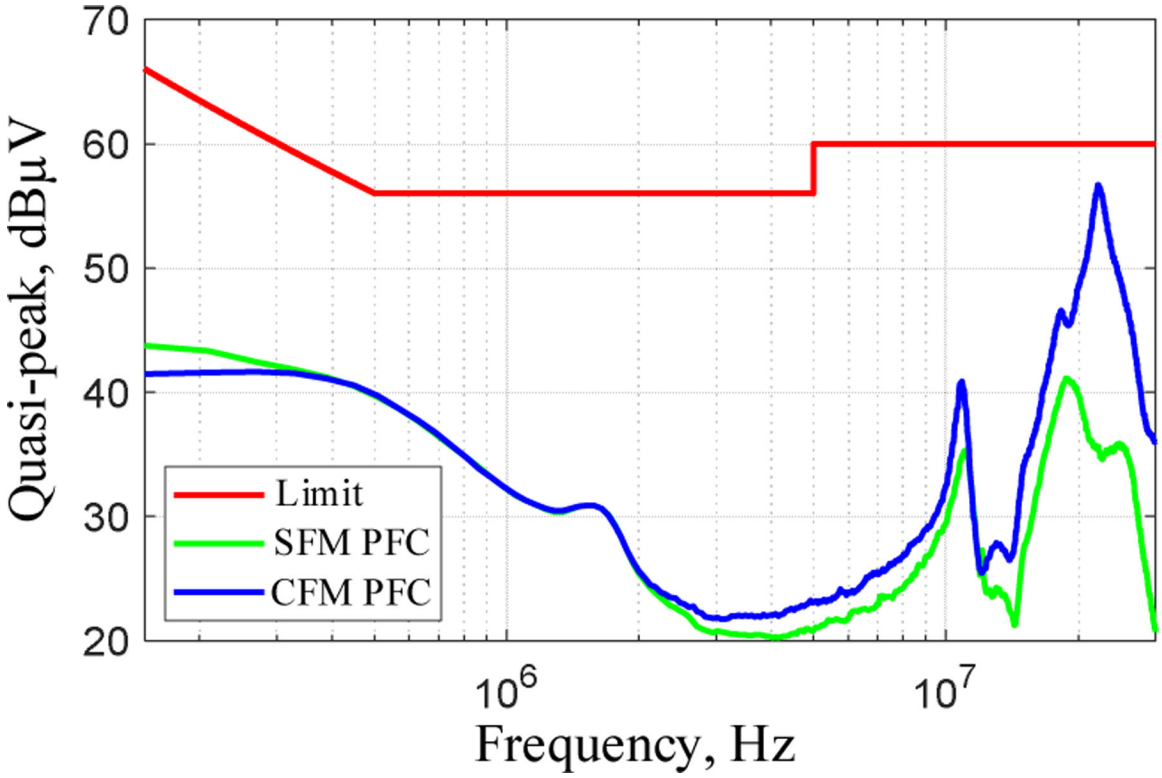

Fig. 6.
Measured conducted EMI noise of the boost PFC with CFM and SFM at 250 W power with an EMI filter.

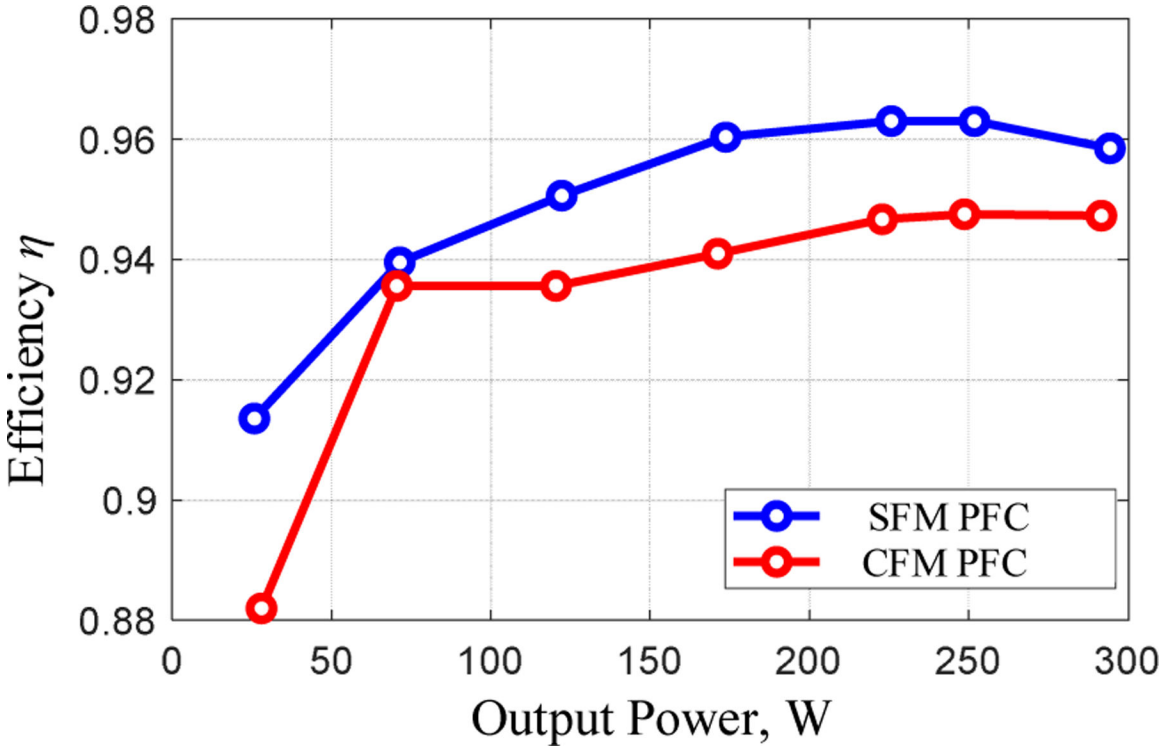

Fig. 7.
Measured efficiency of the boost PFCs with CFM and SFM applied.

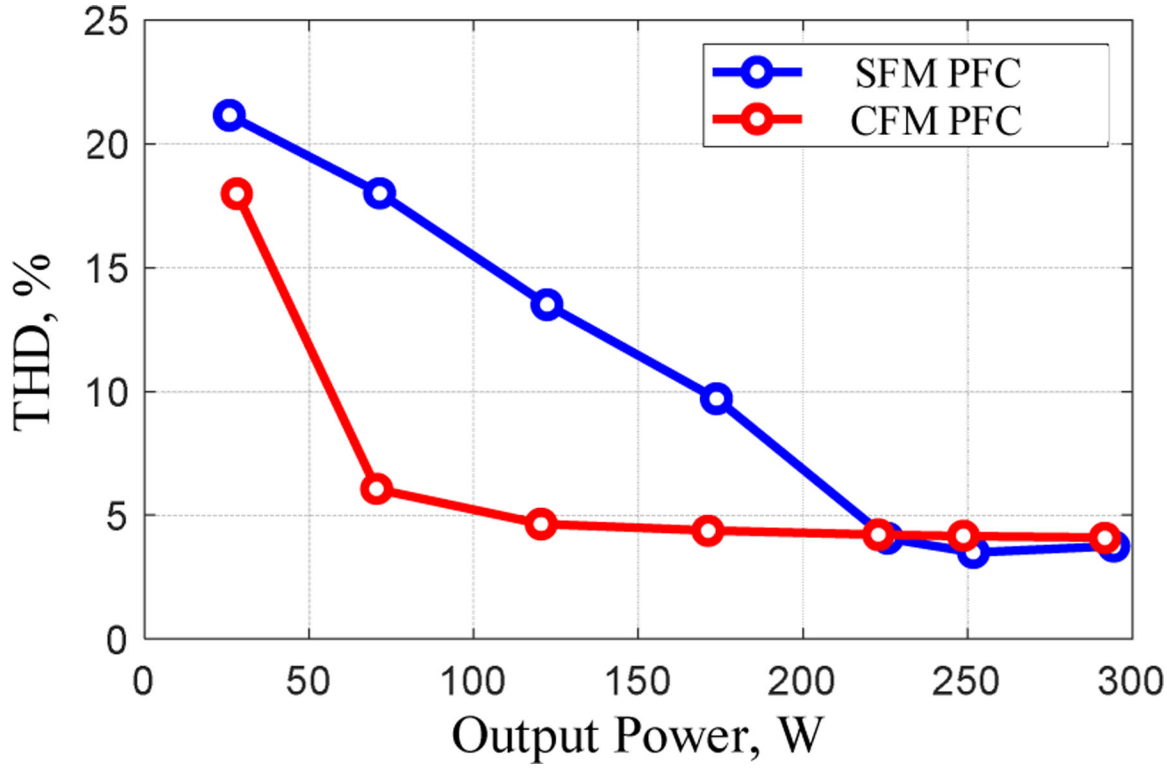

Fig. 8.
Measured THD of the boost PFCs with CFM and SFM applied.

TABLE I.

Boost PFC circuit parameters

Parameters	Value
Nominal input voltage (V_{in})	169.7 V
Nominal grid frequency (f_{grid})	60 Hz
Rated power (P_{out})	300 W
Output voltage (V_{DC})	383 V
Boost inductor (L)	410 μH
Choke inductor (L_1)	8 mH
Choke leakage inductance (L_{leak})	38 μH
CM filter capacitors (C_3, C_4)	2200 pF
DM filter capacitors (C_1, C_2)	0.33 μF

TABLE II.

Analytically calculated losses in boost PFC converters with different modulations

Parameters	Boost PFC with CFM	Boost PFC with SFM
Boost inductor conduction loss P_L	0.321 W	0.351 W
Boost diode conduction loss P_D	0.983 W	0.987 W
Switch conduction loss P_{QC}	1.067 W	1.096 W
Switch C_{oss} losses P_{Qcoss}	4.776 W	3.276 W
Switch on-off losses $P_{Qon\text{-}off}$	7.885 W	6.192 W
Diode junction capacitance loss P_{DCo}	0.499 W	0.342 W

TABLE III.

Comparison of the PFC switch parameters

Parameters	MOSFET used on CFM Boost PFC board (SPP20N60C3)	MOSFET used on SFM Boost PFC board inside PFS7628H
Breakdown Voltage V_{BR}	600 V	600 V
Drain Current I_D	20.7 A @25°C	18 A @25°C
Drain-source on-state resistance $r_{ds,on}$	0.16 Ω @25°C 0.29 Ω @100°C	0.26 Ω @25°C 0.46 Ω @100°C
Effective output capacitance C_o, V_{DS}=0V to 480 V V_{GS} = 0V	83 pF	320 pF