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Discrete-Time Adaptive Control for Three-Phase PWM Rectifier

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Abstract: This paper proposes a dual-loop discrete-time adaptive control (DDAC) method for three-phase PWM rectifiers, which considers inductance-parameter-mismatched and DC load disturbances. A discrete-time model of the three-phase PWM rectifier is established using the forward Euler discretization method, and a dual-loop discrete-time feedback linearization control (DDFLC) is given. Based on the DDFLC, the DDAC is designed. Firstly, an adaptive inductance disturbance observer (AIDO) based on the gradient descent method is proposed in the current control loop. The AIDO is used to estimate lump disturbances caused by mismatched inductance parameters and then compensate for these disturbances in the current controller, ensuring its strong robustness to inductance parameters. Secondly, a load parameter adaptive law (LPAL) based on the discrete-time Lyapunov theory is proposed for the voltage control loop. The LPAL estimates the DC load parameter in real time and subsequently adjusts it in the voltage controller, achieving DC load adaptability. Finally, simulation and experimental results show that the DDAC exhibits better steady and dynamic performances, less current harmonic content than the DDFLC and the dual-loop discrete-time PI control (DDPIC), and a stronger robustness to inductance parameters and DC load disturbances.

Keywords: three-phase PWM rectifier; discrete-time adaptive control; inductance parameter mismatches; load disturbance; discrete-time feedback linearization control

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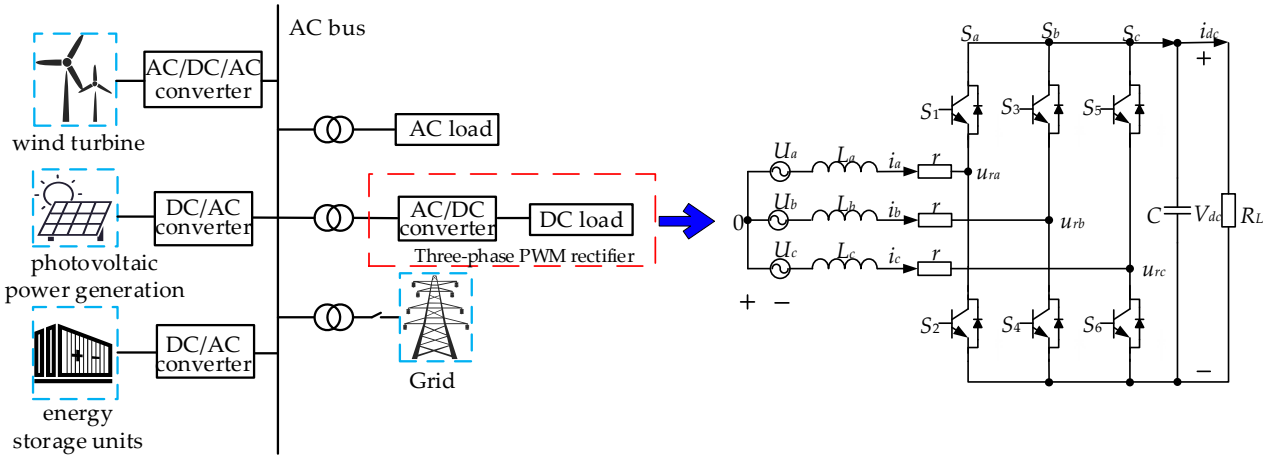
1. Introduction

Microgrids (MG) are essential components of modern power systems, offering various benefits including environmental friendliness, economic viability, flexibility, controllability, and high-power electronics [1]. As illustrated in Figure 1, rectifiers establish connections between AC buses and DC loads. In this context, the primary control objectives of rectifiers are to maintain a stable DC bus voltage for the DC load, operate at a unity power factor, and draw grid current with minimal harmonic distortion. However, PWM rectifiers are inherently nonlinear, multivariable, and coupled systems [2], and their control performances are susceptible to practical disturbances such as DC load disturbances and mismatched parameters (parameter disturbances). Therefore, anti-disturbance control strategies for rectifiers have garnered significant attention in recent years [3–5].

Currently, three-phase PWM rectifiers typically use a dual-loop control structure consisting of a voltage outer loop and a current inner loop [2]. Linear proportional–integral (PI) controllers are commonly used in this structure because of their simple structure and ease of engineering implementation. However, PI controllers have a relatively slow dynamic response. Moreover, since PI controllers are designed with a bounded operating range, their anti-disturbance performance degrades when the system encounters a large disturbance. Consequently, scholars have proposed various control methods to enhance the rectifier's resilience to disturbances. These methods mainly include backstepping control (BSC) [6], passivity-based control (PBC) [7,8], sliding mode control (SMC) [9,10], and adaptive control [11–14].

Of these control methods for rectifiers, adaptive control is a powerful control method, playing a leading role in addressing the global stability problems of nonlinear systems subject

to parameter uncertainty and disturbance. Reference [11] introduces an adaptive BSC to compensate for the inherent nonlinearities and uncertainties in the rectifier. On this basis, reference [12] presents an improved adaptive backstepping sliding mode control, which enhances the global stability of the adaptive BSC by incorporating error compensation and SMC. Reference [13] proposes a robust adaptive control for a three-phase PFC converter. This method utilizes a model reference adaptive control for the voltage outer loop to adapt to loads and capacitor variations. Simultaneously, SMC is used to strengthen the robustness of the current controller. In [14], an efficient adaptive controller is established in the voltage outer loop to improve the controller's ability to regulate DC bus voltage in the presence of external disturbances, and H∞ controllers are applied in the current loop. References [11–14] employ adaptive control to substantially enhance rectifier performance from multiple perspectives. However, the methods in [11–14] are designed in the continuous-time domain and are not directly applicable to a microprocessor using a digital controller. In recent years, with the increasing speed and decreasing cost of microprocessors, controller design utilizing discrete-time control has become a research hotspot in power electronics [15]. Additionally, it is well known that discrete-time systems, rather than continuous-time systems, are widely regarded as being closer to describing a real controlled system [16].



(a) AC microgrid (b)Three-phase PWM rectifier

Figure 1. Rectifier system in an AC microgrid.

Currently, discrete-time adaptive control is widely used in power electronic systems [17–20]. Reference [17] introduces a discrete-time model reference adaptive control method to reduce the number of sensors and improve robustness against unmodeled dynamics and sinusoidal disturbances in an LCL grid-connected inverter. Reference [18] proposes a discrete-time model reference adaptive controller based on adaptive super-twisting sliding mode control, effectively suppressing the 5th, 7th, 11th, and 13th current harmonic components. Reference [19] introduces a new discrete-time direct robust adaptive PI controller featuring fast current tracking, robustness to disturbances and grid inductance variations, and global stability. References [17–19] demonstrate the feasibility and effectiveness of employing discrete-time adaptive control in power electronic systems. However, to the best of our knowledge, most dual-loop adaptive controller methods for three-phase PWM rectifiers are formulated in the continuous-time domain [21,22]; there are no reports on dual-loop discrete-time adaptive controller methods for rectifiers.

This paper proposes a dual-loop discrete-time adaptive control (DDAC) method for three-phase PWM rectifiers, addressing inductance-parameter-mismatched and DC load disturbances. The main contributions of this work include the following:

1. An adaptive inductance disturbance observer (AIDO) is developed in the current control loop using the gradient descent method, ensuring its strong robustness and adaptability to mismatched inductance parameters.

2. A load parameter adaptive law (LPAL) is developed in the DC bus voltage control loop using the discrete-time Lyapunov stability theory, improving the DC load disturbances rejection ability of the DC bus voltage regulator.
3. Comparison experiments are conducted between the DDAC, dual-loop discrete-time feedback linearization control (DDFLC), and dual-loop discrete-time PI control (DDPIC) in a real three-phase PWM rectifier, thereby verifying the superiority of the DDAC.

The remainder of this paper is organized as follows: Firstly, Section 2 briefly introduces a discrete-time model of three-phase PWM rectifiers. Secondly, the shortcomings of the DDFLC are discussed and analyzed in Section 3. After that, in Section 4, the design and analysis of the DDAC are presented in detail. Then, Section 5 presents the simulation and experimental results of the proposed DDAC, which are compared with those of the DDFLC and the DDPIC to verify its effectiveness and advantages. Finally, some conclusions are given in Section 6.

2. Discrete-Time Model of Three-Phase PWM Rectifiers

The AC MG is depicted in Figure 1a. Since the energy storage unit can stabilize the AC bus, the AC bus is considered an ideal AC source in this paper. The circuit of a three-phase PWM rectifier is shown in Figure 1b. U_a, U_b, and U_c are the three-phase grid voltages; V_{dc} is the DC bus voltage; i_a, i_b, and i_c are the three-phase grid currents; L is the inductance; r is the equivalent resistance of the inductance; C is the filter capacitance; and R_L is the DC load. From Figure 1b, the three-phase PWM rectifier dq model is modeled as follows [23].

$$\begin{cases} L\frac{di_d}{dt} = U_d - ri_d + \omega Li_q - u_{rd} \\ L\frac{di_q}{dt} = U_q - ri_q - \omega Li_d - u_{rq} \\ C\frac{dV_{dc}}{dt} = \frac{3}{2}(S_d i_d + S_q i_q) - \frac{V_{dc}}{R_L} \end{cases} \tag{1}$$

where ω represents the voltage angular frequency, U_d and U_q are the active and reactive voltage, i_d and i_q are the active and reactive current, S_d and S_q are the d-axis and q-axis switching components, and $u_{rd} = S_d V_{dc}$ and $u_{rq} = S_q V_{dc}$ represent the control inputs.

Considering the fact that L and r change in a certain range during rectifier operation [24,25], the dq model can be rewritten as follows:

$$\begin{cases} L_0\frac{di_d}{dt} = U_d - r_0 i_d + \omega L_0 i_q - u_{rd} - f_d \\ L_0\frac{di_q}{dt} = U_q - r_0 i_q - \omega L_0 i_d - u_{rq} - f_q \\ C\frac{dV_{dc}}{dt} = \frac{3}{2}(S_d i_d + S_q i_q) - \frac{V_{dc}}{R_L} \end{cases} \tag{2}$$

where f_d and f_q denote the inductance parameter disturbances induced by L and r.

$$\begin{cases} f_d = \Delta r i_d + \Delta L\frac{di_d}{dt} - \Delta L\omega i_q \\ f_q = \Delta r i_q + \Delta L\frac{di_q}{dt} + \Delta L\omega i_d \end{cases} \tag{3}$$

where $L = L_0 + \Delta L$. $r = r_0 + \Delta r$. The forward Euler discretization method is used to discretize Equation (2), which yields

$$\begin{cases} L_0\frac{i_d(k+1)-i_d(k)}{T_s} = U_d(k) - r_0 i_d(k) + \omega L_0 i_q(k) - u_{rd}(k) - f_d(k) \\ L_0\frac{i_q(k+1)-i_q(k)}{T_s} = U_q(k) - r_0 i_q(k) - \omega L_0 i_d(k) - u_{rq}(k) - f_q(k) \\ C\frac{V_{dc}(k+1)-V_{dc}(k)}{T_s} = \frac{3}{2}\left(S_d(k) i_d(k) + S_q(k) i_q(k)\right) - \frac{V_{dc}(k)}{R_L} \end{cases} \tag{4}$$

where T_s denotes the sampling time and $\begin{cases} f_d(k) = \Delta r i_d(k) + \Delta L\frac{i_d(k+1)-i_d(k)}{T_s} - \Delta L\omega i_q(k) \\ f_q(k) = \Delta r i_q(k) + \Delta L\frac{i_q(k+1)-i_q(k)}{T_s} + \Delta L\omega i_d(k) \end{cases}$.

Since the bandwidth of the current loop is considerably larger than that of the voltage loop, it can be assumed that $i_d(k) = i_d^*(k)$ and $i_q(k) = i_q^*(k)$ in a steady state. $i_d^*(k)$ and $i_q^*(k)$

are the d-axis and q-axis reference currents, respectively. Considering that the three-phase PWM rectifier normally operates at a unity power factor, $i_q{}^*(k) = 0$. Consequently, the discrete-time model of the rectifier can be obtained from Equation (4).

$$\begin{cases} L_0\frac{i_d(k+1)-i_d(k)}{T_s} = U_d(k) - r_0 i_d(k) + \omega L_0 i_q(k) - u_{rd}(k) - f_d(k) \\ L_0\frac{i_q(k+1)-i_q(k)}{T_s} = U_q(k) - r_0 i_q(k) - \omega L_0 i_d(k) - u_{rq}(k) - f_q(k) \\ C\frac{V_{dc}(k+1)-V_{dc}(k)}{T_s} = u_{rdc}(k) - \xi(k)V_{dc}(k) \end{cases} \tag{5}$$

where $u_{rdc}(k) = \frac{3}{2}S_d(k)i_d{}^*(k)$, $\xi(k) = \frac{1}{R_L}$.

3. Design of the DDFLC

For the purpose of designing the controller efficiently and conveniently, the control objectives of these controllers are listed as follows:

1. In the current control loop, tracking the respective references of the active current i_d and reactive current i_q is required. In this control module, the reference of the active current $i_d{}^*$ is calculated based on the DC bus voltage control loop, and the reference of the reactive current $i_q{}^*$ is set to 0.
2. In the DC bus voltage control loop, the DC bus voltage V_{dc} must be controlled according to reference $V_{dc}{}^*$ when the system achieves a stable state.

Based on the above control objectives, current tracking errors and the voltage tracking error are defined as follows:

$$\begin{cases} e_{id}(k) = i_d(k) - i_d{}^*(k) \\ e_{iq}(k) = i_q(k) - i_q{}^*(k) \\ e_u(k) = V_{dc}(k) - V_{dc}{}^*(k) \end{cases} \tag{6}$$

where $V_{dc}{}^*$ is the reference DC bus voltage. Combining Equation (6) and the DFLC theory [15], we can obtain the current and voltage controllers, shown as follows:

$$\begin{cases} u_{rd}(k) = U_d(k) + \omega L_0 i_q(k) - r_0 i_d(k) - L_0\left[\frac{i_d{}^*(k+1)-i_d{}^*(k)}{T_s} - k_d e_{id}(k)\right] \\ u_{rq}(k) = U_q(k) - \omega L_0 i_d(k) - r_0 i_q(k) - L_0\left[\frac{i_q{}^*(k+1)-i_q{}^*(k)}{T_s} - k_q e_{iq}(k)\right] \\ u_{rdc}(k) = C\left[\frac{V_{dc}{}^*(k+1)-V_{dc}{}^*(k)}{T_s} - k_{vdc}e_u(k)\right] \end{cases} \tag{7}$$

where k_d and k_q are the control parameters for the current loop and k_{vdc} is a control parameter for the voltage loop, $k_d > 0$, $k_q > 0$, $k_{Vdc} > 0$. By substituting Equation (7) into Equation (5), it can be found that

$$\begin{cases} e_{id}(k+1) = e_{id}(k) - T_s k_d e_{id}(k) - \frac{T_s}{L_0} f_d(k) \\ e_{iq}(k+1) = e_{iq}(k) - T_s k_q e_{iq}(k) - \frac{T_s}{L_0} f_q(k) \\ e_u(k+1) = e_u(k) - T_s k_{vdc} e_u(k) - \frac{T_s}{C}\frac{V_{dc}(k)}{R_L} \end{cases} \tag{8}$$

Lemma 1 [26]. *For the system $z(k+1) = z(k) - lz(k) + g(k)$, if $|l| < 1$ and $|g(k)| < \gamma, \gamma > 0$, then it follows that z(k) is always bounded. There exists a finite number $K^* > 0$ such that $|z(k)| < \frac{\gamma}{|l|}, \forall k > K^*$.*

Assumption 1. *The disturbances $f_d(k)$, $f_q(k)$, and $\xi(k)$ are bounded, and they satisfy $|f_d(k)| < M$, $|f_q(k)| < N$, $|\xi(k)| < G$, $M > 0$, $N > 0$, $G > 0$.*

In accordance with the stipulations of Lemma 1, it can be demonstrated that the control parameters must satisfy the following conditions:

$$0 < k_d < \frac{1}{T_s}, 0 < k_q < \frac{1}{T_s}, 0 < k_{vdc} < \frac{1}{T_s} \tag{9}$$

then the steady state errors are bounded and satisfy

$$|e_{id}(k)| \leq \frac{M}{L_0 k_d}, |e_{iq}(k)| \leq \frac{N}{L_0 k_q}, |e_u(k)| \leq \frac{G}{C k_{vdc}} \tag{10}$$

From Equation (10), it can be seen that $e_{id}(k)$, $e_{iq}(k)$, and $e_u(k)$ will increase with the increments of M, N, and G, and that increasing k_d, k_q, and k_{vdc} aids in decreasing tracking errors. However, k_d, k_q, and k_{vdc} cannot be too large due to the fact that excessive gain will lead to system instability [15]. Therefore, with the DDFLC, it is challenging to achieve no tracking error in the presence of mismatched parameters or load conditions. To address this issue, this paper proposes the DDAC method for three-phase PWM rectifiers.

4. Design of the DDAC

Based on the DDFLC, this section proposes an AIDO for the current inner loop and an LPAL for the voltage outer loop. The AIDO, designed using the gradient descent method, estimates mismatched inductance parameter disturbances and compensates for them in the current controller, ensuring a strong robustness to inductance parameters. The LPAL, designed based on the discrete-time Lyapunov stability theory, estimates the DC load and adjusts it within the voltage controller, thereby achieving DC load adaptability. The design process is as follows, and a flow diagram of the DDAC's design is shown in Figure 2.

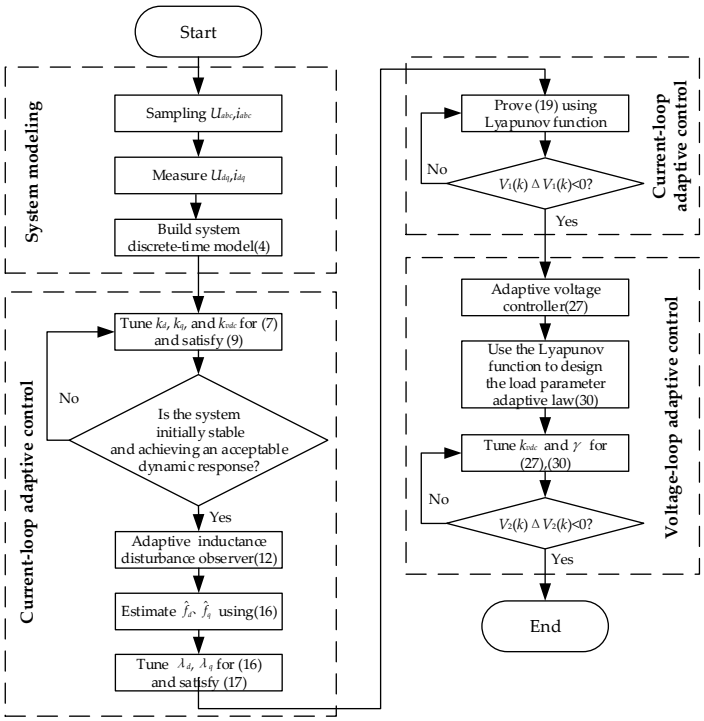


Figure 2. Flow diagram of the controller design.

4.1. Adaptive Controller for the Current Loop

According to Equation (5), the current discrete-time model can be expressed as

$$i_s(k+1) = Ai_s(k) + B[v_s(k) - u_{rs}(k) - f_s(k)] \tag{11}$$

where $i_s(k) = \begin{pmatrix} i_d(k) \\ i_q(k) \end{pmatrix}$, $v_s(k) = \begin{pmatrix} U_d(k) + \omega L_0 i_q(k) \\ U_q(k) - \omega L_0 i_d(k) \end{pmatrix}$, $u_{rs}(k) = \begin{pmatrix} u_{rd}(k) \\ u_{rq}(k) \end{pmatrix}$, $f_s(k) = \begin{pmatrix} f_d(k) \\ f_q(k) \end{pmatrix}$, $A = 1 - \frac{r_0 T_s}{L_0}$, $B = \frac{T_s}{L_0}$.

To estimate $f_s(k)$, a current adaptive observer with an input–output relationship is designed, as shown in Equation (12).

$$\hat{i}_s(k+1) = Ai_s(k) + B[v_s(k) - u_{rs}(k) - \hat{f}_s(k)] \tag{12}$$

where $\hat{i}_s(k)$ is the estimated value of $i_s(k)$ and $\hat{f}_s(k)$ is the estimated value of $f_s(k)$.

The disturbance estimation error $e_s(k)$ and $\widetilde{f}_s(k)$ are defined as

$$\begin{aligned} e_s(k) &= \begin{pmatrix} e_d(k) \\ e_q(k) \end{pmatrix} = \begin{pmatrix} i_d(k) - \hat{i}_d(k) \\ i_q(k) - \hat{i}_q(k) \end{pmatrix} \\ \widetilde{f}_s(k) &= \begin{pmatrix} f_d(k) \\ f_q(k) \end{pmatrix} = \begin{pmatrix} f_d(k) - \hat{f}_d(k) \\ f_q(k) - \hat{f}_q(k) \end{pmatrix} \end{aligned} \tag{13}$$

The gradient descent method is employed to design the AIDO. The gradient descent method is a local parameter optimization approach that assumes that parameters should be updated in a way that minimizes estimation errors [20]. Therefore, the following estimation error functions are considered as candidates:

$$E_s(k) = \begin{pmatrix} E_d(k) \\ E_q(k) \end{pmatrix} = \begin{pmatrix} \frac{1}{2}{e_d}^2(k) \\ \frac{1}{2}{e_q}^2(k) \end{pmatrix} \tag{14}$$

Combining Equations (11)–(14), the following Jacobian matrix J can be obtained.

$$J = \frac{\partial E_s(k)}{\partial \hat{f}_s(k)} = Be_s(k) \tag{15}$$

In accordance with the gradient descent idea [20], $\hat{f}_s(k)$ should change in the direction of the negative gradient. Combining this with Equation (15), this paper proposes an AIDO as follows:

$$\hat{f}_s(k+1) = \hat{f}_s(k) + \Delta\hat{f}_s(k) = \hat{f}_s(k) - \lambda Be_s(k) \tag{16}$$

where λ_d, λ_q are adaptive gain, and they satisfy

$$0 < \lambda_d < \frac{2}{B^2}, 0 < \lambda_q < \frac{2}{B^2} \tag{17}$$

Based on the concept of feed-forward compensation, we develop current controllers as follows:

$$u_{rs}(k) = \begin{pmatrix} u_{rd}(k) \\ u_{rd}(k) \end{pmatrix} = \begin{pmatrix} U_d(k) + \omega L_0 i_q(k) - \hat{f}_d(k) - r_0 i_d(k) - L_0\left[\frac{{i_d}^*(k+1) - {i_d}^*(k)}{T_s} - k_d e_{id}(k)\right] \\ U_q(k) - \omega L_0 i_d(k) - \hat{f}_q(k) - r_0 i_q(k) - L_0\left[\frac{{i_q}^*(k+1) - {i_q}^*(k)}{T_s} - k_q e_{iq}(k)\right] \end{pmatrix} \tag{18}$$

To prove the stability of the current adaptive observer, we define the Lyapunov function as

$$V_1(k) = \frac{1}{2}{e_s}^2(k) \tag{19}$$

Assumption 2. *The disturbance $f_s(k)$ is slow time-varying, it satisfies $f_s(k) = f_s(k+1)$.*

Combining Equations (11), (12), and (16), and Assumption 2, it obtains

$$\Delta e_s(k) = e_s(k+1) - e_s(k) = -\lambda B^2 e_s(k) \tag{20}$$

From Equations (19) and (20), we obtain

$$\begin{aligned} \Delta V_1(k) &= V_1(k+1) - V_1(k) = \tfrac{1}{2}\left[{e_s}^2(k+1) - {e_s}^2(k)\right] \\ &= \left(-\lambda B^2 {e_s}^2(k) + \tfrac{1}{2}\lambda^2 B^4 {e_s}^2(k)\right) \end{aligned} \tag{21}$$

From Equation (17), this can be obtained as

$$-\lambda B^2 {e_s}^2(k) + \frac{1}{2}\lambda^2 B^4 {e_s}^2(k) < 0 \tag{22}$$

Therefore $\Delta V_1 < 0$. According to the discrete Lyapunov stability condition [27]

$$V_1(k)\Delta V_1(k) < 0 \tag{23}$$

From Equation (23), it is evident that $e_s(k)$ will converge to zero. There is $e_s(k) = -B\widetilde{f}_s(k)$, thus $\widetilde{f}_s(k)$ will converge to zero. Consequently, it is reasonable to assume that there exists a finite number $K^*_1 > 0$ such that

$$\left|\widetilde{f}_d(k)\right| \le M_1, \left|\widetilde{f}_q(k)\right| \le N_1, \forall k \ge K_1^* \tag{24}$$

where $0 < M_1 << M$, $0 < N_1 << N$. Substituting Equation (18) into Equation (5), it can be found that

$$\begin{cases} e_{id}(k+1) = e_{id}(k) - T_s k_d e_{id}(k) - \frac{T_s}{L_0}\widetilde{f}_d(k) \\ e_{iq}(k+1) = e_{iq}(k) - T_s k_q e_{iq}(k) - \frac{T_s}{L_0}\widetilde{f}_q(k) \end{cases} \tag{25}$$

From Equations (24) and (25), and Lemma 1, we obtain

$$|e_{id}(k)| \le \frac{M_1}{L_0 k_d} << \frac{M}{L_0 k_d}, \left|e_{iq}(k)\right| \le \frac{N_1}{L_0 k_q} << \frac{N}{L_0 k_q}, \forall k \ge K_1^* \tag{26}$$

It can be seen that, with the same control parameters k_d and k_q, the proposed DDAC can significantly reduce the current tracking error compared to DDFLC.

4.2. Adaptive Controller for the Voltage Loop

DC loads in the AC MG are frequently unknown and time-varying, which places higher requirements on the performance of the voltage controller. This section employs the discrete-time Lyapunov stability theory to design the LPAL for estimation of DC loads in real-time, thereby ensuring the voltage controller's adaptability to DC loads. The design process is as follows.

Firstly, the proposed discrete-time adaptive voltage controller is as follows:

$$u_{rdc}(k) = \hat{\xi}(k)V_{dc}(k) + C\left[\frac{{V_{dc}}^*(k+1) - {V_{dc}}^*(k)}{T_s} - k_{vdc}e_u(k)\right] \tag{27}$$

where $\hat{\xi}(k)$ is the estimated value of $\xi(k)$.

Secondly, we employ discrete-time Lyapunov theory to design the LPAL. The specific process is as follows.

Define the following Lyapunov function:

$$V_2(k) = \frac{1}{2}[Ce_u(k)^2 + \frac{1}{\gamma}\widetilde{\xi}^2(k)] \tag{28}$$

where $\widetilde{\xi}(k)$ is the load parameter estimation error, $\widetilde{\xi}(k) = \hat{\xi}(k) - \xi(k)$. γ is the adaptive gain, $\gamma > 0$.

Assumption 3. *$\xi(k)$ is slow time-varying, it satisfies $\xi(k+1) = \xi(k)$. $\widetilde{\xi}(k)$ is bounded and satisfies $\widetilde{\xi}(k) \le M_2$, and M_2 is the upper bound of $\widetilde{\xi}(k)$.*

Combining Equations (5) and (27), and Assumption 3, we obtain

$$\begin{aligned}\Delta V_2(k) &= V_2(k+1) - V_2(k)\\ &= \tfrac{1}{2}\left[Ce_u{}^2(k+1) - Ce_u{}^2(k)\right] + \tfrac{1}{2}\left[\tfrac{1}{\gamma}\widetilde{\xi}^2(k+1) - \tfrac{1}{\gamma}\widetilde{\xi}^2(k)\right]\\ &= \tfrac{1}{2}[e_u(k+1) + e_u(k)][Ce_u(k+1) - Ce_u(k)] + \tfrac{1}{2}\left[\widetilde{\xi}(k+1) + \widetilde{\xi}(k)\right]\left[\tfrac{1}{\gamma}\widetilde{\xi}(k+1) - \tfrac{1}{\gamma}\widetilde{\xi}(k)\right]\\ &= -CT_s k_{vdc} e_u{}^2(k) + \left([\tfrac{\sqrt{C}T_s k_{vdc}}{\sqrt{2}} e_u(k)] - [\tfrac{T_s}{\sqrt{2C}}\widetilde{\xi}(k)V_{dc}(k)]\right)^2 + \tfrac{T_s}{2} e_u(k)V_{dc}(k)[\widetilde{\xi}(k) - \widetilde{\xi}(k+1)]\end{aligned} \tag{29}$$

This paper designs the LPAL as follows.

$$\frac{\hat{\xi}(k+1) - \hat{\xi}(k)}{T_s} = -\gamma e_u(k)V_{dc}(k) \tag{30}$$

Substituting Equation (30) into Equation (29) yields

$$\Delta V_2(k) = -CT_s k_{vdc} e_u{}^2(k) + \left([\frac{\sqrt{C}T_s k_{vdc}}{\sqrt{2}} e_u(k)] - [\frac{T_s}{\sqrt{2C}}\widetilde{\xi}(k)V_{dc}(k)]\right)^2 + \frac{T_s{}^2}{2}\gamma e_u{}^2(k)V_{dc}{}^2(k) \tag{31}$$

According to the Cauchy–Buniakowsky–Schwarz Inequality [28], we obtain

$$\frac{\Delta V_2(k)}{k_{vdc}{}^2} \le \frac{-CT_s e_u{}^2(k)}{k_{vdc}} + CT_s{}^2 e_u{}^2(k) + \frac{T_s{}^2 V_{dc}{}^2(k)\gamma}{2k_{vdc}{}^2} e_u{}^2(k) + \frac{T_s{}^2 V_{dc}{}^2(k)\widetilde{\xi}^2(k)}{Ck_{vdc}{}^2} \tag{32}$$

Combing this with Assumption 3, if the selected k_{vdc} satisfies

$$k_{vdc} >> \frac{T_s V_{dc}(k)M}{\sqrt{C}} > \frac{T_s V_{dc}(k)\widetilde{\xi}(k)}{\sqrt{C}} \tag{33}$$

then form Equations (32) and (33); we obtain

$$\Delta V_2(k) \le -CT_s k_{vdc} e_u{}^2(k) + CT_s{}^2 k_{vdc}{}^2 e_u{}^2(k) + \frac{T_s{}^2 V_{dc}{}^2(k)\gamma}{2} e_u{}^2(k) \tag{34}$$

Further, if

$$0 < \gamma < \frac{2\left(Ck_{vdc} - CT_s k_{vdc}{}^2\right)}{T_s V_{dc}{}^2} \tag{35}$$

then $\Delta V_2 < 0$. Combining Equations (9) and (33), k_{vdc} satisfies

$$\frac{T_s V_{dc}(k)M}{\sqrt{C}} << k_{vdc} < \frac{1}{T_s} \tag{36}$$

From the above analysis, it can be concluded that $e_u(k)$ and $\widetilde{\xi}(k)$ can converge to zero. Further, M_2 can be chosen as a smaller value close to zero. The parameter design procedure for the DDAC is summarized as follows:

Step 1: Use Equations (9) and (36) to select k_d, k_q, and k_{vdc}. They should be initially set to large values to avoid a slow dynamic response, and then gradually decreased until the system stabilizes and an acceptable dynamic response is achieved.

Step 2: Set the adaptive parameters λ_d, λ_q, and γ to large values based on Equations (17) and (35). Adjust these values until the system achieves an optimal steady state and dynamic performance.

Based on the above analysis, a block diagram of the DDAC is illustrated in Figure 3.

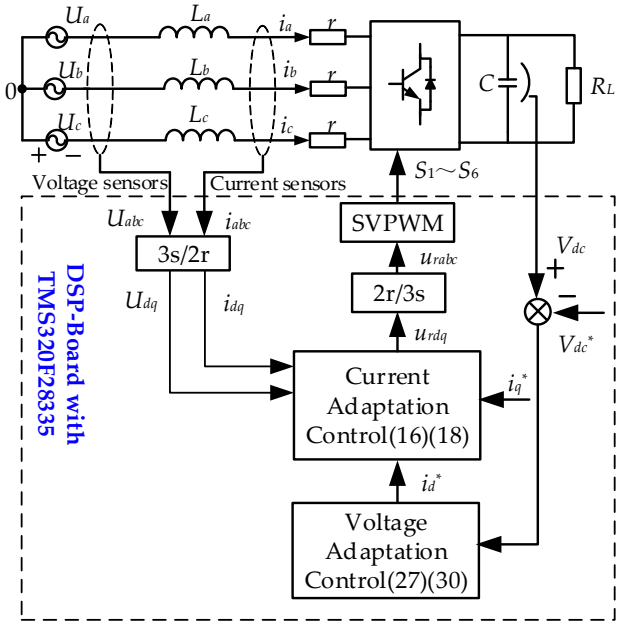


Figure 3. Block diagram of the proposed DDAC.

Remark 1. *Considering the physical properties of inductors and current protection, it is obvious that* ΔL, Δr, $i_d(k)$, *and* $i_q(k)$ *must be limited. For rectifiers, the sampling frequency is usually high. Related to the sampling system,* $f_s(k)$ *and* $\xi(k)$ *can be considered slow time variables,* $f_s(k)$ *and* $\xi(k)$ *are approximated as constants in a sampling period, namely* $f_s(k) = f_s(k+1)$, $\xi(k+1) = \xi(k)$.

5. Simulation and Experimental Verification

This paper uses MATLAB/Simulink (2018) for simulations, with the experimental platform shown in Figure 4. In Figure 4, an autotransformer is connected to a 311 V grid to generate 38 V. The voltage and current sensors are LV-25P and LA-55P (LEM Company, Geneva, Switzerland), respectively. The power switching device is IRFP460 (INFINEON Company, Neubiberg, Gemany), and the control algorithm is implemented via TMS320F28335 (TI Company, Dallas, TX, USA). The experimental data are acquired using TPS2024B (Tektronix Inc., Beaverton, OR, USA), TDS1012B-SC (Tektronix Inc.), and DS1204B (RIGOL Company, Suzhou, China). The estimated inductance disturbances and the DC load are obtained from a four-channel DAC7724 (TI Company). A six-channel AD7656 (Analog Devices Company, Wilmington, MA, USA) is selected to collect voltage and current signals. To verify the superiority of the DDAC, experimental and simulation comparisons are conducted with the DDFLC and the DDPIC. The main circuit parameters are listed in Table 1, and the control parameters are listed in Table 2.

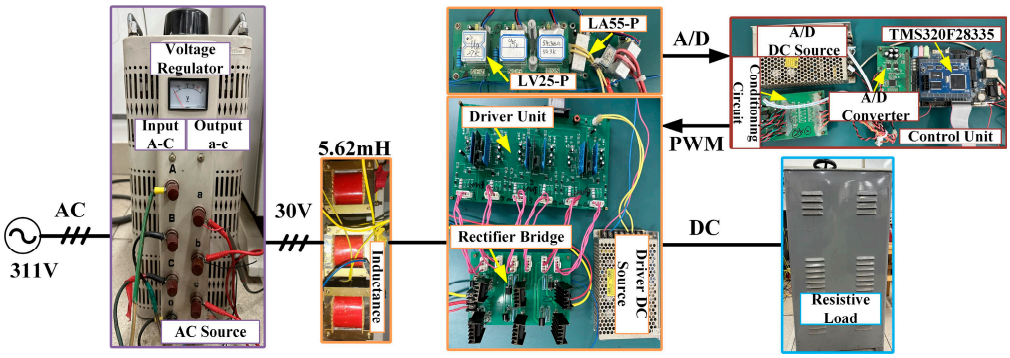


Figure 4. Three-phase PWM rectifier experimental platform.

Table 1. System parameters.

Meaning	Parameters	Value	Units
Grid voltage (peak voltage)	V_m	30	V
Grid frequency	f	50	Hz
Filter inductance	L	5.62	mH
Equivalent resistance	r	1.2	Ω
DC bus reference voltage	V_{dcref}	100	V
DC filtering capacitor	C	1000	μF
Sampling frequency	f_s	9000	Hz

Table 2. Parameters of control systems in the experiment.

Controllers	Parameters	Value
DDAC	k_d	50
	k_q	50
	λ_d	10
	λ_q	10
	k_{vdc}	180
	γ	0.00005
DDFLC	k_d	50
	k_q	50
	k_{vdc}	180
DDPIC	k_{p_d}	50
	k_{i_d}	150
	k_{p_q}	50
	k_{i_q}	150
	k_{p_vdc}	180
	k_{i_vdc}	370

5.1. Dynamic and Steady-State Performance at Nominal Parameters

In this case, the DC load steps up from no load to a load composed of a 50 Ω resistor. Figures 5 and 6 show the transient response of the DC bus voltage. In Figures 5 and 6e, DDPIC exhibits an excellent steady-state performance. However, the PI controller based on the deviation control principle makes it difficult to overcome the control time lag caused by the capacitive element [4], resulting in a low response. From Figures 5 and 6c, it is evident that the DDFLC exhibits a significant steady-state error. This is because increasing the k_{vdc} can reduce the error, as illustrated in Equation (10). However, a large k_{vdc} will lead to V_{dc} instability [15]. Therefore, a compromise k_{vdc} is selected in this paper. It can be further observed from Figures 5 and 6a,c that, under the same k_{vdc} condition, the steady state error of DDAC is significantly smaller than that of DDFLC, confirming the correctness of Equations (10) and (26). Figure 7 illustrates the response of the LPAL when L_0 is equal to L. It can be seen that $\hat{\xi}(k)$ can quickly and smoothly converge to the steady state value (≈0.025). The theoretically calculated value is about 0.02. This slight discrepancy is attributed to practical factors such as measurement errors, measurement noise, and line impedance. However, this discrepancy does not impact the DC bus voltage tracking effect, as demonstrated in Figures 5 and 6a.

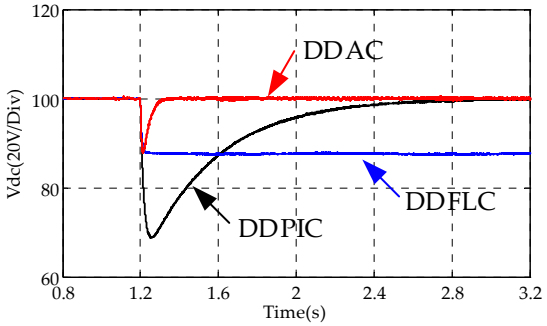
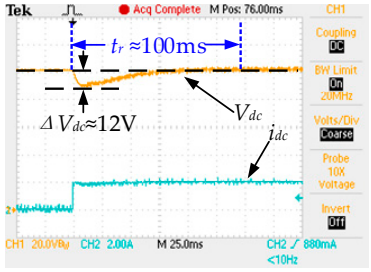
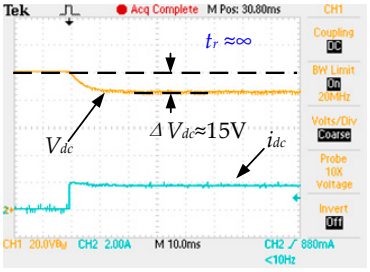


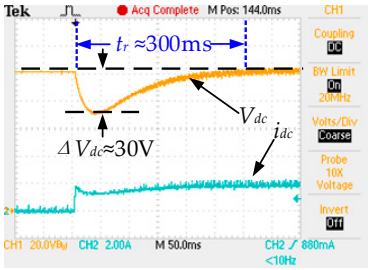
Figure 5. Simulation waveforms when the load steps from 0 Ω to 50 Ω.



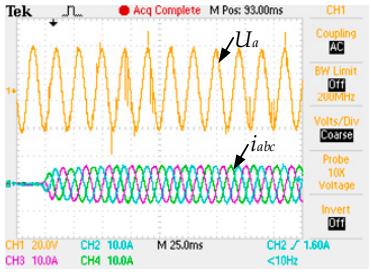
(a) DC bus voltage and current(DDAC)



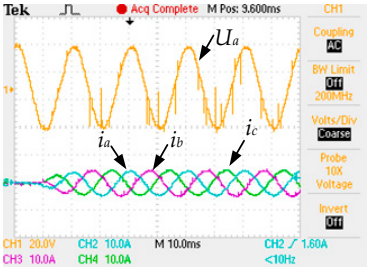
(c) DC bus voltage and current(DDFLC)



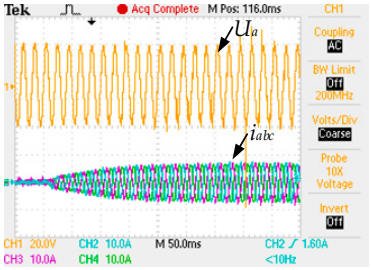
(e) DC bus voltage and current(DDPIC)



(b) Grid-side voltage and current(DDAC)



(d) Grid-side voltage and current(DDFLC)



(f) Grid-side voltage and current(DDPIC)

Figure 6. Experimental waveforms when the DC load steps from 0 Ω to 50 Ω.

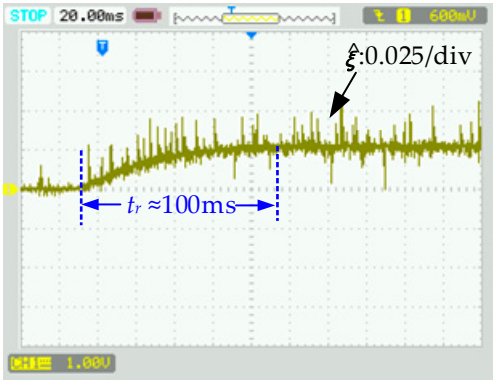
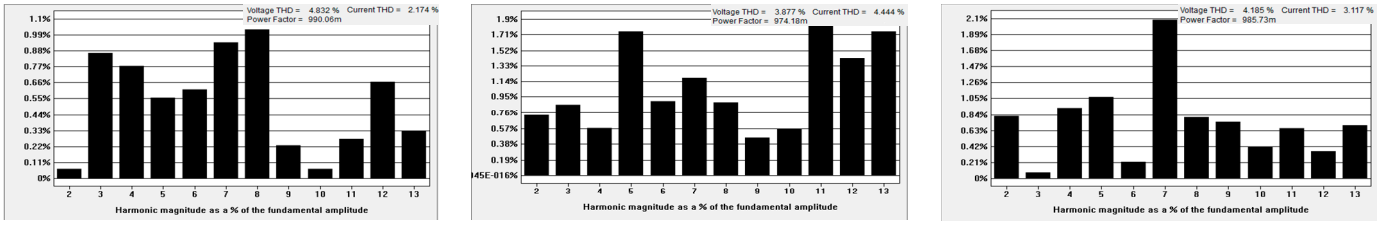


Figure 7. The response of the LPAL when L_0 is equal to L.

Figure 6b,d,f display the steady-state current waveforms of three control methods. Harmonic analyses with an a-phase current are shown in Figure 8. The current THD values for DDFLC are 4.444% (i_a), 4.383% (i_b), and 4.609% (i_c). The current THD values for DDPIC are 3.117% (i_a), 3.008% (i_b), and 3.396% (i_c), while the current THD values for DDAC are 2.174% (i_a), 2.543% (i_b), and 2.668% (i_c). These results indicate that all methods meet the IEEE 519-2014 standards [29] of a THD below 5%; however, the DDAC exhibits the smallest current THD. As illustrated in Figure 8, the 5th and 7th harmonics under DDAC are smaller than those of DDFLC and DDPIC. Moreover, the 9th, 11th, and 13th harmonics are reduced compared to the DDFLC and the DDPIC. These findings suggest that the DDAC has the best steady-state performance. Additionally, from Figure 8, it is observed that even when the grid voltage THD is high, the DDAC still maintains the minimum current THD. This is because grid voltage harmonics can be considered as a part of $f_s(k)$ in Equation (11), and grid voltage harmonics are estimated by the AIDO and compensated for in the DDAC, thereby reducing the influence of grid voltage harmonics on the grid-side current.



(a) DDAC (b) DDFIC (c) DDPIC

Figure 8. Harmonic analyses under steady-state conditions.

5.2. Parameter Robustness

In this section, the robustness of both the DDFLC and the DDAC are investigated under different combinations of L_0 and r_0. It should be noted that the parameters in the control system are mainly changed to evaluate the robustness of the control, because this method can avoid the degradation of filter performance due to the physical changes in its L filter and r [30]. Figures 9 and 10 show the simulation and experimental results with different combinations of L_0 and r_0. In Figures 9 and 10a, it is observed that the voltage drops and transition times do not change significantly, regardless of how L_0 and r_0 change. These results indicate that the DDAC has a strong robustness to L and r due to the AIDO compensating for $f_d(k)$ and $f_q(k)$. Figure 10c shows the transient response of the LPAL and the AIDO when L_0 is equal to 1.5 L. It can be seen that $\hat{\xi}(k)$ and $\hat{f}_q(k)$ can quickly and smoothly transition to steady-state values ($\hat{\xi}(k) \approx 0.025$, $\hat{f}_q(k) \approx 5.3$). This indicates that the proposed the LPAL and the AIDO are effective under inductance parameter variations.

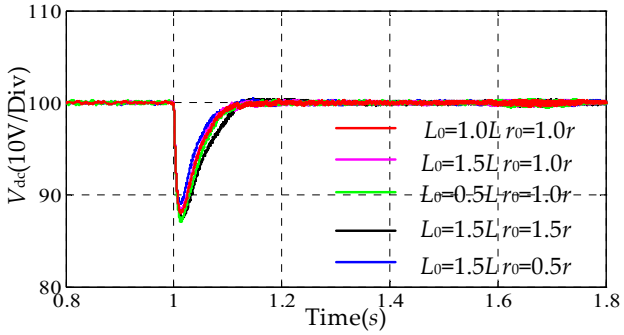
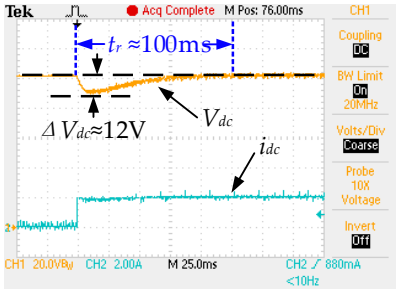
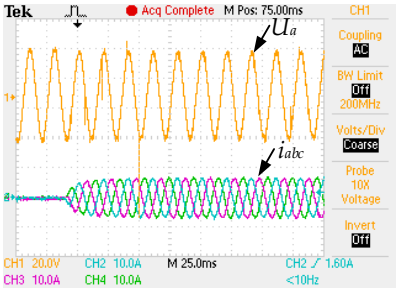


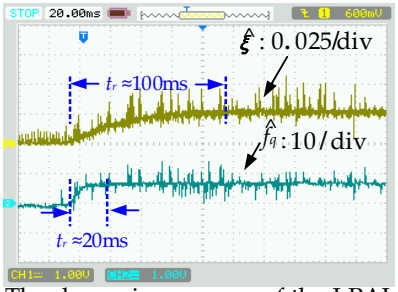
Figure 9. Simulation waveforms under different mismatched inductance parameters.



(a) DC bus voltage and current



(b) Grid-side voltage and current



(c) The dynamic response of the LPAL and the AIDO

Figure 10. Dynamic responses under mismatched inductance parameters (L_0 = 1.5 L, r_0 = 1.0 r, load steps from 0 Ω to 50 Ω).

Figure 11 shows the current tracking errors of the DDFLC and the DDAC. It can be observed that the current tracking errors with the DDFLC are 0.2 A (d-axis current) and 1 A (q-axis current), while those with the DDAC consistently remain near zero. This indicates

that the AIDO significantly enhances the current tracking accuracy of the DDAC, while simultaneously enhancing the DDAC's robustness to inductance parameters.

(a)DDFLC (b)DDAC

Figure 11. Current tracking errors when $L_0 = 1.5\,L$.

6. Conclusions

Based on the DDFLC, this paper proposes a DDAC for a three-phase PWM rectifier, which considers inductance-parameter-mismatched and DC load disturbances. An AIDO is designed in the current loop using the gradient descent method to enhance its robustness against inductance-parameter-mismatched disturbances. Additionally, an LPAL is designed in the voltage loop to enable the rectifier system to adapt to load disturbances. The proposed DDAC can be directly employed in digital control systems. Compared with the DDFLC and the DDPIC, in simulation and experiment, the proposed DDAC exhibits the fastest response, the smallest DC bus voltage drop, the smallest current tracking error, and a strong robustness to inductance parameter and load disturbances, while also minimizing its current harmonics contents. The DDAC has the potential to be applied to other converters, such as three-phase three-level Neutral Point Clamped (NPC) rectifiers, thus possessing significant theoretical and engineering value.

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