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On the Design and Manufacturing of Miniaturized Microstripline Power Splitters for Driving Multi-Coil Transmit Arrays with Arbitrary Ratios at 7 Tesla

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Abstract

Purpose: To implement unequal microstrip power splitters for parallel transmission at 7 Tesla which are optimized for size and loss and can be configured for a wide range of power ratios. The splitters will enable the use of more transmit coils without a corresponding increase in the number of transmit channels or amplifiers to control SAR, shorten RF pulses, and shim inhomogeneous RF fields.

Methods: Wilkinson unequal power splitters based on a novel microstrip network design were optimized to minimize their size under 8 cm in length and 9 cm in width, enabling them to be included in a coil housing or cascaded in multiple stages. Splitters were designed and constructed for a wide range of output power ratios at 298 MHz. Simulations and bench tests were performed for each ratio, and a methodology was established to adapt the designs to other ratios and frequencies. The designs and code are open-source and can be reproduced as-is or reconfigured.

Results: The single-stage designs achieved good matches and isolations between output ports (worst isolation -15.9 dB, worst match -15.1 dB). A two-stage cascaded (1 input to 4 outputs) power splitter with 1:2.5, 1:10, 1:3, and 1:6 ratio outputs was constructed. The worst isolation between output ports was -19.7 dB in simulation and the worst match of the 3 ports was -17.8 dB. The measured ratios for one and two-stage boards were within 10% of the theoretical ratios. The power handling capability of the smallest trace was approximately 70 watts. Power loss for the one and two-stage boards ranged from 1-3% in simulation compared with 5.1-7.2% on the bench.

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Conflicts of Interest

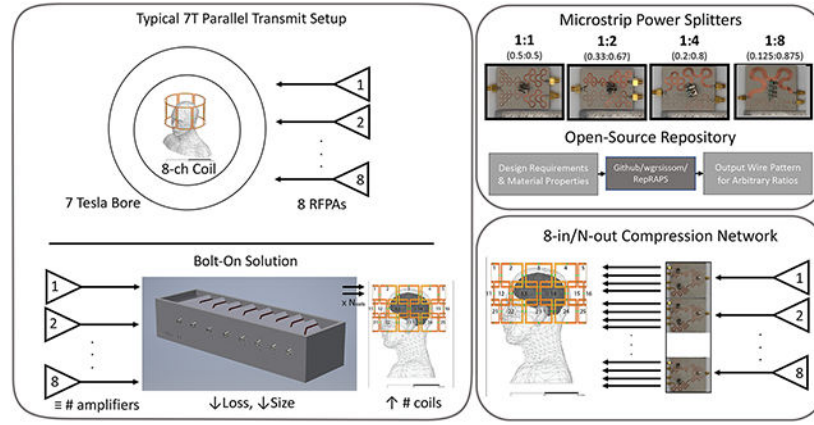
The authors declare no conflicts of interest.

Code availability

To facilitate reproducing and adapting the circuits to other ratios and applications, a complete package of code, design files for the circuits in this study as well as a video tutorial has been made available at <https://github.com/wgrissom/RepRAPS>.

Conclusion: Wilkinson unequal microstrip power splitters can be implemented with a small board size (low height) and low loss, and across a wide range of output power ratios. The splitters can be cascaded in multiple stages while maintaining the expected ratios and low loss. This will enable the construction of large fixed transmit array compression matrices with low loss.

Graphical Abstract



This work describes a universal method for creating microstripline Wilkinson power splitters that have been optimized for size and loss. As the design can be configured for a wide range of power ratios, the framework is useful for ultra-high field MRI parallel transmission coils and overcoming existing transmit amplifier limitations with the use of array compressed parallel transmission.

Keywords

RF coils; MR Engineering; Ultra-high Field MRI (UHF MRI); Parallel Transmission (pTx); Optimization; Miniaturization; Planar Transmission Line; Array Compression

Introduction

For parallel transmission (pTx) at ultra-high field strengths of 7 Tesla or above, a large number of coils can be highly beneficial. A large number of coils allows for fine control over specific absorption rate (SAR) [1-3], the excitation of complex patterns with short-duration pulses [4], and spatially uniform excitation via B_1^+ shimming [5-8]. However, state-of-the-art ultra-high field scanners today have only 8 or 16 transmit channels versus up to 128 receive channels, and increasing the number of channels is difficult for many reasons, including the high cost of transmit amplifiers, cabling requirements, and space limitations inside the bore. There have been several technical developments made to facilitate many-coil parallel transmit. These include many-channel transmitters [9], improvements in amplifier performance via real-time amplifier feedback control [10], decoupling coils [11], mode compression, decoupling using Butler matrices [12,13], on-coil and current-mode amplifiers [14,15], and coil element and array designs that may reduce or eliminate the need for decoupling [16-18].

Another solution that addresses many of the drawbacks of many-coil pTx is the use of a bolt-on network that is designed to optimally drive a many-coil array with a smaller

number of channels. The original concept, termed array-compressed parallel transmission (acpTx), was first proposed by Cao et al. [19], with a first hardware implementation by Yan et al. [20]. In acpTx a set of compression weights (amplitudes and phase shifts) are optimized jointly with pTx pulses, and the weights are implemented in a splitting, (relative) attenuating, and phase-shifting network that connects the small number of amplifiers to the larger number of coils. Unequal splitters are needed to realize the compression weights needed for the network. The control of amplitude and phase, through unequal splitters, can be used to achieve better transmit performance and increased signal homogeneity, otherwise enabled by using additional RF amplifiers. Ideally, the weights could be adjusted in real-time on a subject-to-subject, scan-to-scan, or even pulse-to-pulse basis. To this end, the use of PIN diodes and MEMS to dynamically switch between weights during a scan has been explored, which comes with the tradeoff of added complexity and power loss [21,22]. At the same time, it has been shown that a fixed set of weights can be used between different subjects and scans with a large improvement in the excitation accuracy B_1^+ homogeneity versus SAR tradeoff [23,24], compared to conventional systems with the same number of channels and coils.

This suggests that for most applications, acpTx networks may not need to be adjusted once manufactured. For such fixed networks, matching the target and realized compression weights while minimizing power loss, size, and complexity is paramount. While fixed phase shifts can be implemented using transmission lines, relative attenuations are more challenging due to large differences in impedance needed, and ratio-adjustable power splitter (RAPS) circuits have been developed using lumped elements and coaxial cables [25] and commercial hybrid couplers [26] for this application. However, each of these solutions has some drawbacks including large numbers of lumped elements and screw connections which lead to large sizes and/or power losses, or mechanical connections that may affect reliability. In the present work we prioritized low loss, small size, a small number of elements, and circuit simplicity while maintaining high isolation and manufacturability.

Common power splitting solutions include: 1. the Wilkinson power splitter; 2. the reactive power splitter; 3. the Lange coupler; 4. the branchline coupler; 5. the rat-race coupler; 6. the hybrid 3 dB coupler; and 7. the Gysel coupler [27]. In this work, the Wilkinson unequal power splitter [27,28] was chosen for its low insertion loss, its high isolation, and its ability to easily split the output power with arbitrary ratios. To address the need for compact low-loss fixed unequal power splitters, we designed and evaluated microstrip unequal Wilkinson power splitters. This was done using an iterative design process starting with theoretical design equations, followed by circuit layout and electromagnetic simulations to tune the trace length before manufacturing. Once the simulations were within tolerance, boards were milled, connectorized, bench tested, and fine-tuned. The splitters comprise only planar transmission lines, microstrip lines, and a single resistor. Imaging experiments were performed to evaluate the achieved power ratios. The splitters are based on a high dielectric constant-substrate [29], which improves manufacturability and size and enables output power ratios up to 1:8, where this limit was established based on manufacturability of the very-high impedance traces required at higher ratios: Larger power ratios are more difficult to manufacture. Defected ground structure (DGS) was used to realize the larger power ratios. Splitters were designed and constructed with 1:1, 1:2, 1:4 and 1:8 ratios,

to demonstrate feasibility across a large ratio range to cover a variety of applications. As there are various new emerging pTx coil developments, this framework is intended to be compatible with a wide variety of coil designs and can either be constructed in separate housing or integrated into the coil housing. A 1-channel-to-4-coil two-stage network was constructed from three of these splitter circuits. A detailed methodology for the board design and construction was established for reproducibility.

Methods

The design equations used for construction follow Figure 1 which shows schematics of microstrip Wilkinson splitters for equal and unequal output ratios. The RF signal V_{in} is divided into two ports (V_1 and V_2) with the power ratio between the two ports determined by the impedances of the traces. Given a desired voltage ratio $\gamma = V_1 / V_2$, each trace's characteristic impedance and the resistor value can be calculated using the following equations (Ref. [27] §7.3):

$$\begin{aligned} Z_1 &= Z_0 \sqrt{\gamma^{-1.5} + \gamma^{-0.5}}, \\ Z_2 &= Z_0 \gamma^{0.25} \sqrt{1 + \gamma}, \\ Z_3 &= Z_0 \gamma^{-0.25}, \\ Z_4 &= Z_0 \gamma^{0.25}, \\ R_{isolation} &= Z_0 (\gamma^{0.5} + \gamma^{-0.5}). \end{aligned}$$

Given a trace's characteristic impedance Z , thickness t [mil], relative permittivity (dielectric constant) ϵ_r , and copper weight c [mil], its width [mil] is given by [27,30-33]:

$$W = \frac{7.48 \times t}{e^{\frac{1}{87}} Z_0 \sqrt{\epsilon_r + 1.41}} - 1.25 \times c$$

This Wilkinson splitter design can be expanded such that the number of output ports is increased to drive a larger number of coils either in a single stage or cascaded in multiple stages. In this work, we consider 1 input-to-2 output (single-stage) unequal splitters both individually and as building blocks of a 1 input-to-4 (two-stage) output unequal splitter. For ease of manufacturing we: 1. Chose a suitable dielectric material to reduce the trace size of the microstrip Wilkinson circuit; and 2. used a meandering method to reduce overall board size.

A microstrip Wilkinson circuit is typically large due to the use of quarter wavelength-long traces of about 14.43 cm at 298 MHz for FR4 $\epsilon_r = 4$, a typical RF substrate. The wavelength decreases as ϵ_r increases, and materials with $\epsilon_r > 4$ are available which yield shorter quarter-wave traces. However, trace width also decreases for a given desired characteristic impedance as ϵ_r increases, which can lead to unreliable manufacturing. To address this problem, we previously considered materials [34] with ϵ_r between 4 and 7 to minimize size while ensuring reliable milling. We chose Rogers RO3006 laminate (Rogers Corporation, Chandler, AZ) for this work, since it has a dielectric constant $\epsilon_r = 6.5$, a copper weight of 1 ounce (approx. 35 μm thick), and a substrate thickness of 50 mil. This material also has

low loss and a high degree of manufacturability at 7 Tesla which has been a significant consideration in other compact RF circuit designs [12,13].

To further reduce board size, a meandering method [35] was applied to spread the traces over more of the board surface. The optimized designs comprise matrices of rings, each split into four equal length segments. The radius of the rings was calculated using the trace widths and the length of the microstrip segment. Given the wavelength λ and the desired trace width W , the wire pattern was calculated using the following equations for a desired electrical length and the diagram shown in Figure 2 [35]:

$$\Gamma = \frac{\pi r}{2\lambda},$$

$$r_1 = \sqrt{\frac{\Gamma\lambda^2}{\pi} + \frac{W^2}{2}} + \frac{\Gamma\lambda}{\pi} - \frac{W}{2},$$

$$r_2 = W + r_1,$$

$$r = 2\frac{r_2 \times r_1}{r_2 + r_1}.$$

These curves were concatenated to achieve the required total trace length. Figure 3 shows manually meandered and ring-meandered 1:1 splitter board designs. Applying ring-meandering reduced the board area by 37%. In addition, the ring-meandered layout allows for better spacing between the connectors for each connection or cascading while minimizing trace coupling effects. As the traces are larger in size, the coupling effects will increase.

CAD Layout, EM Simulation, and Manufacturing

Splitters with power ratios (V_1^2 / V_2^2) of 1:1, 1:2, 1:4, and 1:8 were designed in Autodesk Eagle (San Francisco, CA, USA) using the above equations and assuming the use of the RO3006 laminate substrate and ideal resistance. The Larmor frequency (298 MHz) determined the length of the quarter-wave traces to be 11.79 cm, shorter than using FR4, and with the additional benefit of lower loss.

To form the ring-meandered trace patterns, a single ring was laid out for each trace and duplicated to form the full trace [35]. Each of the 4 segments was placed in a separate net and the individual segment lengths were calculated from there. All segment editing was done in Eagle to ensure that the simulated CAD model matched the constructed PCBs. The final wire pattern was full wave-simulated in Ansys HFSS (Canonsburg, PA, USA) for approximate circuit resonance frequency. This was iterated several times to center the resonance frequency at 298 MHz by adjusting the trace lengths.

For the 1:8 board, the defected ground structure (DGS) technique was applied wherein slots were milled in the ground plane underneath the traces [36]. This increased trace inductance and enabled a wider, more manufacturable trace width to be used; without DGS, the circuit's narrowest trace was thinner than could be reliably milled (< 0.4 mm). Additionally, as the traces become thinner with higher power ratios, the less power handling capability they have. The traces with the smallest width have a power handling capacity of about 70 Watts

shown in Appendix A. Six different DGS geometries were evaluated in terms of the resulting match, isolation, and ratio in simulation. The six different geometries were tested in the HFSS simulation before the final DGS pattern was applied to the board on the bench.

We further developed a workflow for designing a multi-stage splitter. The four 1 input-to-2 output circuits were designed for both single and two-stage (both 3 and 4 output ports) use, where the layouts for two-stage designs had modified port positions to ensure that the stages lined up properly and could be milled on a single board without connectors between the stages. Alignment of ports was especially important to develop this multi-stage workflow. Though exponential tapers between traces of different widths are encouraged at high frequencies for better impedance matching [37] they were found to be unnecessary in simulation for these devices.

The boards were milled using an LPKF S103 (LPKF Laser & Electronics, Garbsen, Germany). The RO3006 substrate was used for all circuits. Each 1 input-to-2 output board (1:1, 1:2, 1:4, 1:8) was milled along with a two-stage 1 input to 4 output splitter to demonstrate port placements and ease of cascading the circuits. The two-stage board was built of 1:1 (stage 1), 1:2 (stage 2), and 1:4 (stage 2) boards, which had nominal output ratios of 1:2.5 (0.4), 1:10 (0.10), 1:3 (0.335), and 1:6 (0.165). Nonmagnetic high-power resistors rated for 60 W were used (American Technical Ceramics, Huntington Station, NY, USA). The resistor values were 100 Ω , 100 Ω , 125 Ω , and 200 Ω 5% for the 1:1, 1:2, 1:4, and 1:8 splitters, respectively. SMA connectors were used at the ports for their small size and compatibility.

To facilitate reproducing and adapting the circuits to other ratios and applications, a complete package of code, design files for the circuits in this study as well as video tutorials has been made available at <https://github.com/wgrissom/RepRAPS>. This includes MATLAB (Mathworks, Natick, MA, USA) code that takes as input the desired number of output ports and ratios, the operating frequency, and properties of the laminate and cladding, and outputs a wire pattern that can be saved as a bitmap, imported into an image editor and filled to complete the output wire pattern. Then the filled wire pattern (a 256-color bitmap) can be imported to a circuit design software such as Eagle, where it can be edited and exported as a DXF file for the EM simulator. The video tutorial walks the user through the process. The inputs and outputs of the MATLAB code are illustrated in Figure 4. Scripts are provided for multiple port configurations, including a 1 input-to-2 output, single stage circuit, a two-stage 1 input-to-3 output circuit, and a 1 input-to-4 output two-stage circuit. The port configurations determine the location of the ports so that the traces align and the number of stages and outputs can vary for implementation. We have previously published code to determine individual splitter ratios for multistage networks with a set of desired output voltage ratios [25].

Experimental Validation: Bench Measurements

A 4-port Keysight E5080A ENA Vector Network Analyzer (Santa Rosa, CA, USA) was used for reflection and transmission measurements. All cables were calibrated to the board connection to account for adapters. S11, S22, and S33 were measured to validate the resonance and match of the input port (port 1) and the two output ports (ports 2 and 3).

S23 was measured to verify the effective isolation of the output ports. S12 and S13 were measured to verify the desired ratios were being achieved.

These bench measurements were compared to the simulations and minor adjustments were made to the design as needed.

Experimental Validation: Phantom Imaging

To verify the splitter ratios in imaging, a 14 cm-diameter mineral oil bottle phantom was imaged in a Nova Medical Inc (Wilmington, MA, USA) birdcage coil with a 32-channel receive array insert on a Philips Achieva 7T scanner (Best, Netherlands). A single port of the birdcage coil was used for transmission to measure the power ratio between the output ports of the circuit. The coil's 90° port was connected to port 1 of the divider and port 2 was terminated using a 50 Ω non-magnetic load. The 0° port of the interface box was terminated using a high-power load inside the scanner room and the 0° port on the coil was terminated using a 50 Ω non-magnetic low-power load. After scans with port 1 of the divider were completed, the port connections were swapped for a second set of scans. This produced images for each of port to determine the splitter output ratios. The dividers' input ports were connected to the 90° port of the interface box to use one of the 4 kW RF amplifiers. Low-flip-angle gradient-recalled echo images were collected for each port configuration (TR = 500 ms, flip angle = 15°, 3 mm slice thickness, 336 x 336 matrix size), where transmit gain was held fixed when scanning with the other port. 20 averages were used the 1:8 splitter produced very little excitation from its smaller output port. Power optimization for each scan was turned off so that the scanner didn't change the transmit gain in between scans when changing the port. For the reference image, the 0° port was terminated and the same cables used to connect the divider were used along with an adapter to enable measuring the splitters' loss inside the scanner. Special attention was paid to ensuring that the power not being delivered to the coil was properly terminated with a high-power load.

Results

Simulations

Figure 5 shows the final circuit boards used in HFSS simulations with full ground planes, along with simulated ratios versus frequency. The simulation results for the power ratios are shown (S12 and S13). The tuning, port match, and the output port isolation was maximized relative to each other before finalizing the design for each of the ratios. On average, the initial imported wire patterns were approximately 9 MHz off resonance based on simulations. The length was adjusted to tune the circuit to the Larmor frequency. The worst isolation in simulations between the output ports was -12.3 dB, -10.7 dB, -8.69 dB and -5.92 dB, respectively, and the worst match in simulations was -13.59 dB, -13.48 dB, -11.63 dB and -11.06 dB, respectively. The circuit is reciprocal; the s-parameters are independent from the direction of propagation. The calculated ratios from the simulations are shown for comparison to theoretical values. The calculated ratios from the simulations at 298 MHz were 1:1.00, 1:1.76, 1:2.13, and 1:8.69 (with DGS for the 1:8 board). The 1:1 and 1:2 splitters are closest to their desired ratios while the 1:4 and 1:8 are further off. For the 1:4 board the ratio is harder to achieve while the 1:8 simulation shows that DGS is required

to achieve that ratio. Overall, the simulations are most useful for adjusting the trace lengths for tuning the circuit instead of ratio adjustment, while the widths of the traces are better determined by the analytical equations.

Six DGS geometry designs were tested in simulations for the 1:8 splitter, as shown in Figure 6. These included a large block design, a three-barbell design, a large-barbell design, a rectangular snake, a circle pattern, and a larger three-barbell design. The resonance frequency of the circuit was found to be approximately 30 MHz higher than the Larmor frequency which was acceptable for the DGS comparison. The best matches for the ports (S11, S22, S33) and the best isolation of the output ports (S23) were achieved using the large block cutout. Additionally, the large block cutout made it easiest to achieve the desired output ratio. Based these results, the large block cutout was used in the manufactured board, with minor adjustments to optimize the power ratio.

Experimental Validation: Bench Measurements

Figure 7 shows the manufactured boards with the resistors that were configured in series or a combination of series and parallel. We note that while the 1:1, 1:2, and 1:4 constructed boards had full copper backing, the 1:8 boards used the block cutout DGS (Figure 6) to maintain manufacturable trace sizes. The DGS cutout was 3 cm x 1.5 cm. Milling each board took approximately one hour (including calibration and setup time). The milling time for the 1:8 board was longer since the bottom layer also had to be milled for DGS. The final board sizes for the four boards were 7 cm x 5.25 cm x 0.65 cm (1:1), 7 cm x 5.25 cm x 0.65 cm (1:2), 7 cm x 6.35 cm x 0.75 cm (1:4), and 8 cm x 9 cm x 0.5 cm (1:8), respectively. The heights of the boards were minimized and determined by the resistor count, position and orientation. The bench power ratio measurements are plotted across frequency and are comparable to the simulation results for the 1:1 and 1:2 splitters. The ratio measurements for the 1:4 and 1:8 splitters do not match as well, though the resonance frequency is accurate. The worst isolation on the bench between the output ports was -22.6 dB, -17.5 dB, -20.0 dB and -15.9 dB for the 1:1, 1:2, 1:4, and 1:8 boards, respectively, and the worst match on the bench was -21.2 dB, -21.5 dB, -15.8 dB and -15.1 dB, respectively. Figure 8 shows the two-stage cascaded power splitter, with 1:2.5 (0.4), 1:10 (0.10), 1:2.985 (0.335), and 1:6.06 (0.165) ratio outputs. The worst isolation between output ports was -19.72 dB (S23) and the worst match was -17.79 dB (S22).

Bench-measured losses were between 5.1-7.2% for all boards after calibration. Due to resistor value mismatch and other imperfections during construction, there was some additional loss compared to simulation and more isolation between the output ports of a splitter with a larger ratio. Aside from manufacturing and practical limitations, most of the loss can be attributed to the adapters, the lumped components (the high-power resistors) and impedance mismatch at the connectors. The boards accounted for between 0.28 dB and 0.3dB power loss (about 7%).

Experimental Validation: Phantom Imaging

Figure 9 shows the phantom imaging results and compares imaging-measured ratios with bench-measured ratios. The signal levels were uniform across the phantom due to the

division of the two images to obtain the ratio and the use of a mineral oil phantom. The same region of interest in the middle of the phantom (not including the edges) was selected in the middle of the phantom for all cases to make the ratio measurements. The measured power ratios were 1:0.98, 1:1.85, 1:4.73, and 1:6.32, for the 1:1, 1:2, 1:4, and 1:8 splitters, respectively.

The overall results for the achieved versus targeted ratios and power losses are shown in Tables 1 and 2. The ratios for the 1:1 and 1:2 power splitters are closest to the theoretical ratios. As the ratios increased to 4 and 8 the ratio error also increased to 0.73 and 1.68, respectively and relative to the normalized ratio. The loss was most accurately measured on the bench. As expected, the simulated losses were lower than the bench measurements. The average loss of 6.22% on the bench is low given the previous iteration of RAPS circuits have reported 10% [25] and 7.31% [26]. The magnitude of loss and accuracy of the ratios held for the two-stage cascaded network as well, indicating that these circuits can be cascaded to drive many more coils from a single transmit channel.

Discussion

This work presented the design, simulation, and manufacturing of a set of compact microstrip unequal power splitters that allow a small number of RF transmit amplifiers to be connected to a larger number of coils at 7 Tesla. Manufactured boards were validated using bench measurements and further in phantom imaging experiments. 1 input-to-2 output power splitters were designed with output ratios of 1:1 (0.5:0.5), 1:2 (0.33:0.67), 1:4 (0.2:0.8), and 1:8 (0.125:0.875). The circuits are compact, they have low loss and accurate ratios, and they can be cascaded together to build one input-to-many output networks. As more stages are added, the board size does increase but the number of coils doubles. A challenge with the board comes from the difference in trace width from large power split ratios. The wire patterns change drastically when the trace width changes. The error associated with in-bore experiments can be attributed to interference and cable currents along with noise and calibration errors. Our wire pattern ensures that the inter-trace coupling is minimized by the elimination of long parallel traces in many conventional microstripline designs. The design also ensures that if more stages are added, the input and output ports will align. In this work has shown up to a 1:8 power split ratio but higher ratio power splitting can be achieved using this framework. The two-stage size board can easily fit inside the bore with the coil and the other cables/connectors. Additionally, an open-source code toolbox was developed to enable others to generate the wire patterns for other materials, power ratios, and field strengths.

Minimizing power loss was paramount in this work to minimize circuit heating and maximize the power reaching the coils. Additionally, any mismatch can lead to high power reflected back into the amplifiers, leading to potential hardware damage. The PCB loss on our boards was less than 7.2%. The loss from the boards themselves depends on the loss tangent of the substrate chosen which was very low for the RO3006 used in this work (0.0020). The limiting factors for loss in the constructed boards were the connectors, components, adapters, and cables as those are required but each add some non-negligible loss.

There are some limitations to the proposed splitter designs. For much thicker traces the curvature may take up too much space in comparison to thinner traces. On the other hand, with thinner traces, the curvature may not provide the most space-efficient wire pattern. Additionally, for large power output ratios and additional cascading, aligning the ports input to output will become more difficult. As the power ratio increased, the bench results became more necessary as the simulation didn't capture the complexities of manufacturing. The lengths of the wire pattern aren't a concern because large pTx arrays (> 16 coils) aren't common below 7 T. As the field strength increases, the length of the wire pattern will become shorter and the splitters will further decrease. There are various other meandering geometries that would produce similar ratio results. However, given our design criteria for small size and in-house production we found that the meandering method was most suitable. Without a size constraint, coupling could be optimized by changing the geometry of the traces.

Striplines or coplanar waveguides (CPWs) are alternatives to microstrip transmission lines. We chose microstrip transmission line for its ability to be constructed in-house, which allows design iterations and reduces cost. If the splitters were to be placed closer together within the network, striplines may be preferred to avoid coupling between the traces and to increase power handling capabilities. CPW manufacturing requires via stitching along the traces which would be time-consuming for in-house construction but could also be a potential future transmission line method. Additionally, Rogers Corporation has recently begun producing laminate boards with embedded fiberglass that could increase the rigidity of the splitters while maintaining their higher dielectric constant.

The ratio measurements taken from the VNA were highly reproducible, while the imaging results were noisier. The imaging experiments were helpful to pair with the bench tests because they allowed realistic power handling testing and testing of any unexpected issues like eddy currents. In the future, it may be advantageous to use an improved setup so that the power being delivered to the coil can be measured with confidence without extensive signal averaging. Additionally, for smaller ratio power splits the ratios were constant over wide frequency ranges, as was shown in Figure 7. As the target ratio increased, the circuit's frequency dependence increased over a 100 MHz span, which indicated that there is more possibility to tune with DGS but also that care needs to be taken to ensure that the ratio is correct at the Larmor frequency and that the increased trace width and coupling effects are accounted for. The largest error in the imaging-measured ratios was for the 1:8 board, which may have experienced a frequency shift in the bore due to its stronger frequency dependence compared to the other boards.

In the scanner, the high transmit power could create an issue for thin traces or components. We ensured that the traces could handle the power applied and the components could withstand power transmitted during imaging. The smallest trace width can handle about 70 Watts without a significant temperature increase that would change the dielectric properties. The resistors had heat sinks and could be replaced with resistors with higher power ratings if needed. Custom resistors would reduce loss by avoiding the use of series or parallel resistors and achieving more accurate values. If placing multiple boards in the bore increases coupling, the wire pattern could be altered to increase the turn radius and move the traces

further apart. Additionally, large eddy currents may be generated on the ground plane. To mitigate this disturbance, the ground plane can be segmented. This should lead to only minor deviations from the results presented here. Additionally, the power reflected from each channel is monitored via the scanner. Because the proposed circuits are effectively part of the fixed coil array, for the purposes of SAR monitoring each input channel can still be treated as a single coil. Further coil-resolved monitoring could be achieved using on-coil RF power monitoring similar to [38].

Forming networks of the proposed splitter circuits enables the use of a large number of coils driven by a small number of transmit channels. For example, 64 coils could be driven by 8 input channels. Transmit performance is higher over a larger region when the number of transmit loops increases. It has been shown in simulation that more than 32 elements are required to approach optimal transmit efficiency at 7 Tesla in the entire head [39]. The optimization considers the ratio of transmit sensitivity and RF power deposition. It has been found that the optimal number of coil elements isn't infinite given that coil geometries determine what current patterns can be generated by an array. Additionally, work by Cao et al [23] has shown that a 48-ch coil array outperforms smaller coil arrays in terms in excitation flip angle RMSE and head-averaged SAR. To determine the upper bound of the ideal coil number, work has been done by Hardy et al [40] to determine that 256 small elements perform best under realistic current constraints based on excitation homogeneity, local SAR, and global SAR. Much work remains to determine the ideal number of coils. This work supports various coil geometries and increased coil count without substantial system changes. Additionally, most of the work to determine the ideal number of coils for parallel transmission has been done in simulation and may change as more coil decoupling and building strategies emerge to realize these very dense arrays. Any coupling between coil elements should be captured in the $B1^+$ maps used in determining the network weights. The proposed circuits and the networks they can form will remain applicable as these coil geometries with various coil element counts are developed.

Conclusion

Wilkinson unequal microstrip power splitters using microstriplines were optimized for small board size and low loss, across a broad range of power ratios. Code and instructional materials were provided to reproduce the boards so they can be applied widely in ultra-high field MRI. The splitters can be cascaded, output to input, into two or more stages while maintaining the expected ratios and low loss. The measured ratios for one and two-stage boards were within 10% of the theoretical ratios and power loss for the one and two-stage boards ranged from 5.1-7.2%. Used in acpTx networks, these power splitters (when combined with phase shifters) are a building block that can improve the transmit performance of current UHF scanners without significant modifications. In future work this will enable the construction of a two-stage 8-channel-to-30-coil acpTx matrix with less than 7.2% power loss [41].

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Appendix A

The power calculation for the following substrate and trace width of 4mm [Pozar]

$$P_{max} = \frac{V_{max}^2}{2Z_0}$$

Peak power will have the circuit suffer from breakdown effects like arcing while average power will cause the circuit to breakdown from heating effects. To calculate the maximum current ANSI/IPC-2221/IPC-2221A design standards for PCB trace width are used. For external traces, current is

$$I_{max} = 0.024 * dT^{0.44} * A^{0.725}$$

For 0.4mm trace width, 1.2 Amps with a temperature rise of 10 degrees C is reasonable. Given that the smaller traces will inherently have less power as the divider splits the power, this is acceptable. The substrate used RO3006 has significant dielectric property change with temperature increase, so 10 degrees C is the desired maximum temperature rise. If the dielectric properties change then the ratio will not hold so keeping this heating limitation in mind determines how much amperage the traces can handle. The smallest trace can handle about 70 Watts of power at 50-ohm impedance [42,43].

Abbreviations

pTx	parallel transmission
SAR	Specific absorption rate
acpTx	Array-compressed parallel transmission
RMSE	Root mean square error

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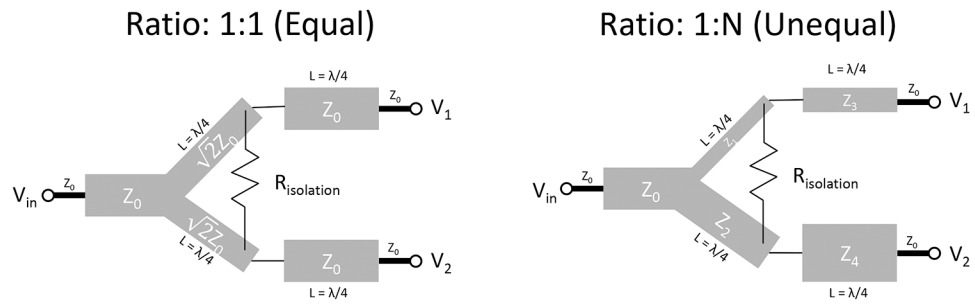


Figure 1:

Left: A 1:1 microstrip power splitter circuit using a Wilkinson topology. Right: An unequal Wilkinson microstrip power splitter, which has different trace widths on each branch.

Ring-meandered Layout

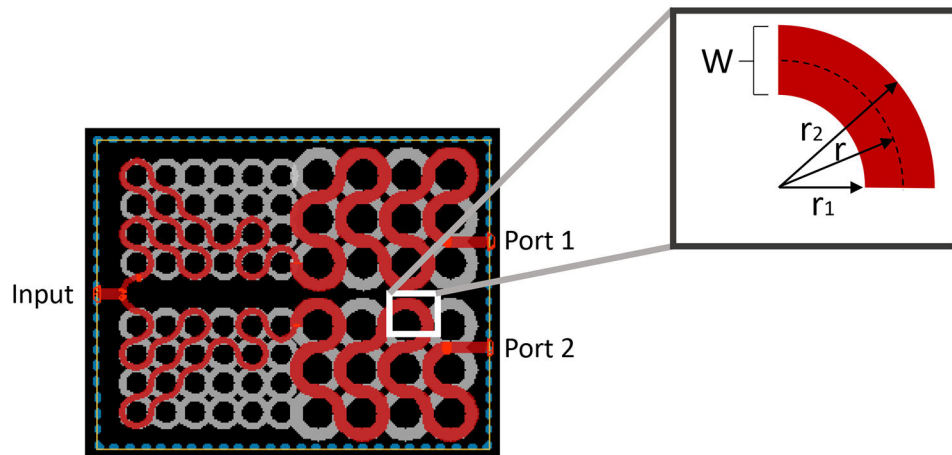


Figure 2: The geometry used in the calculation of the meandered trace curves. The beige traces are the potential trace positions, and the red traces are the actual chosen trace locations for this board. This is a two-layer board with a full copper ground plane on the bottom layer.

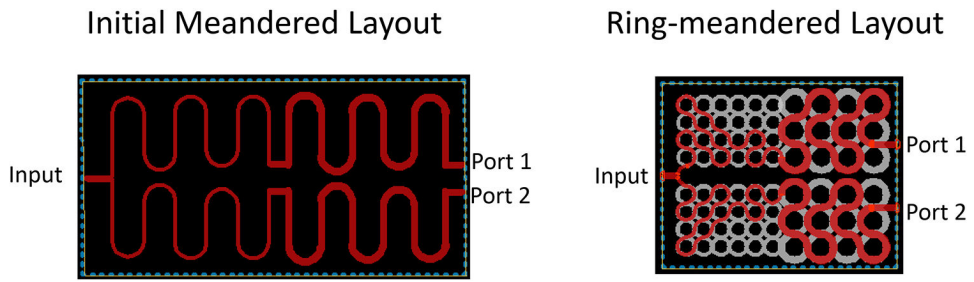


Figure 3: Left: An initial meandering circuit layout. Right: The same circuit with ring-meandering, which reduced the board size by 37%.

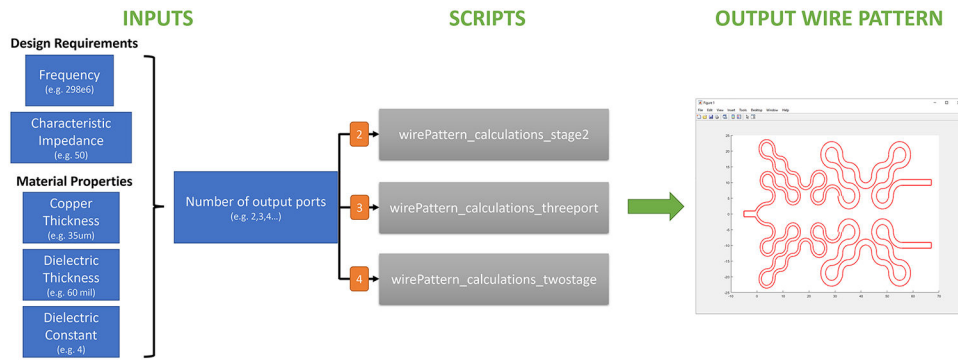


Figure 4: Illustration of the wire pattern generation code showing input parameters, functions, and an output wire pattern which is saved as a bitmap file for further processing.

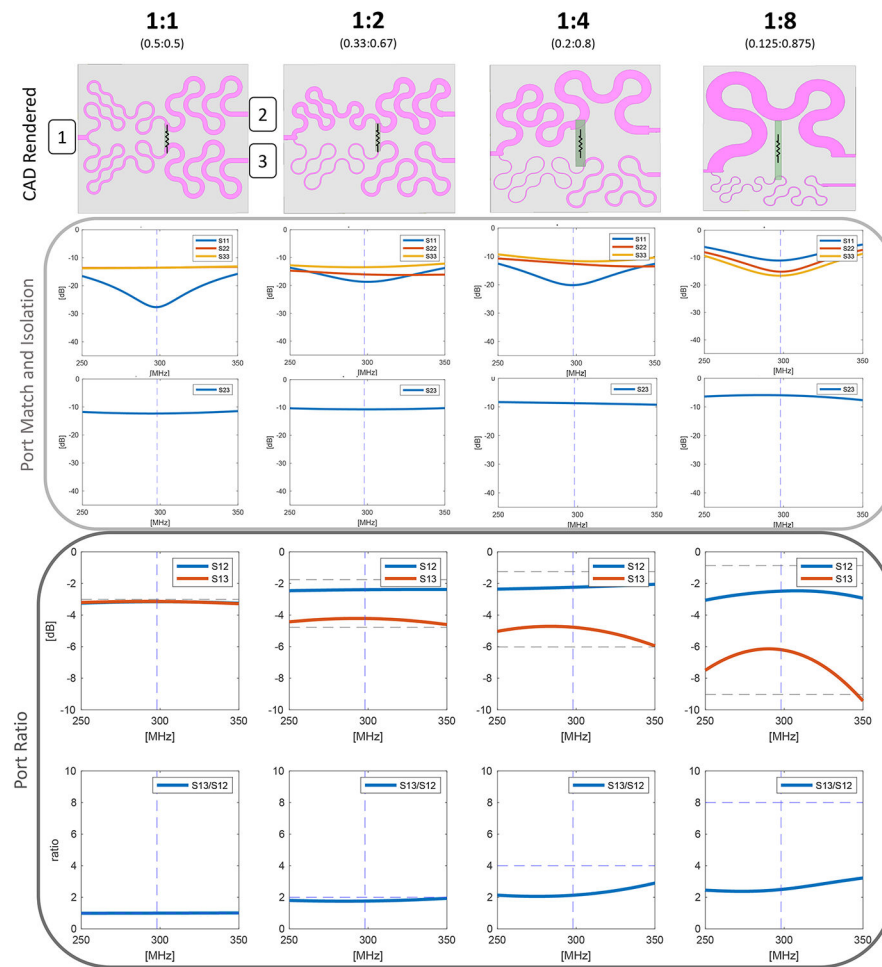


Figure 5: Simulation results for each splitting ratio. Top row: The simulated circuit boards; all boards had a full ground plane. The pink structures are the traces and the green structures are the resistors. The top plots show the simulated port matches (S11, S22, and S33) and output isolations (S23) versus frequency. Simulated power ratios (1:1, 1:2, 1:4, 1:8) are shown in the bottom plots; the power ratios were calculated from the ratio of the input port to each of the output ports (S12,S13). The nominal frequency and ratios are indicated by the vertical and horizontal dashed lines, respectively, while the simulated values are plotted with solid lines. All the bottom layers are full copper ground planes.

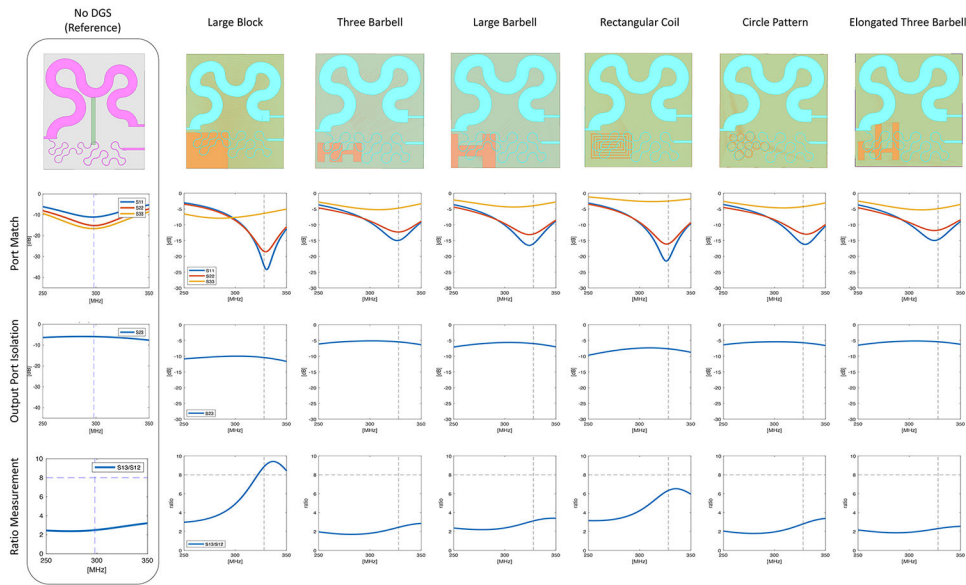


Figure 6: Comparison of defected ground structure (DGS) patterns for the 1:8 splitter. DGS is implemented by removing copper on the bottom of the PC board, and each pattern appears in orange underneath the thin 0.4 mm trace in the top row. From left to right: a large block design, a three barbell design, a large barbell design, a rectangular coil, a circle pattern, and an elongated three barbell design. The second row shows the port match, the third row shows the output port isolation, and the fourth row shows the ratio for each design. The simulation results are provided on the left without the use of DGS for easy comparison.

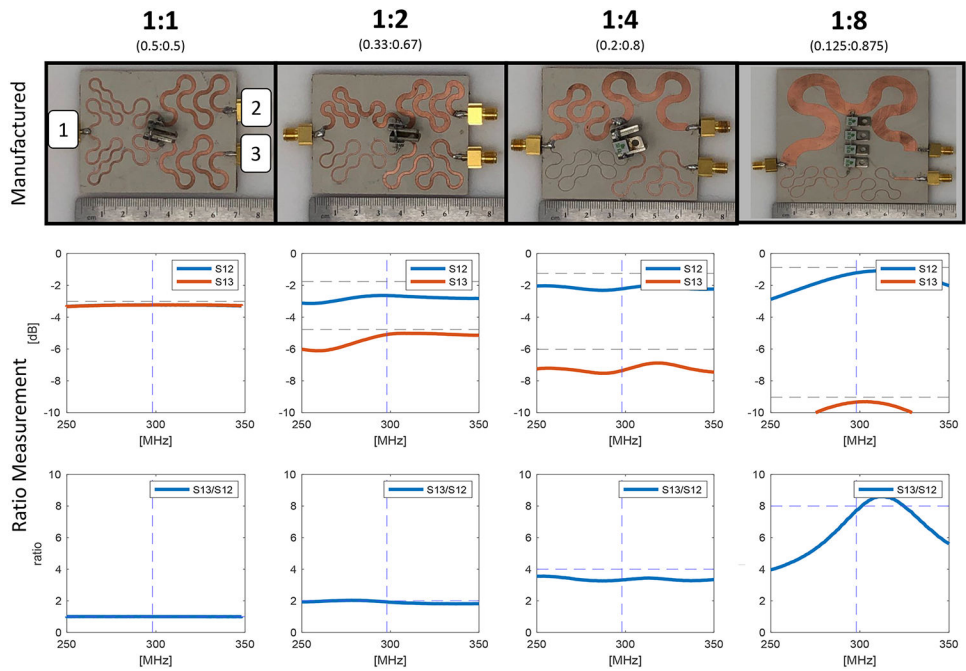


Figure 7: Manufactured splitters for each ratio and bench measurements versus frequency. The power ratios were calculated from the ratios of the transmission coefficients from the input port to each of the output ports (S12, S13).

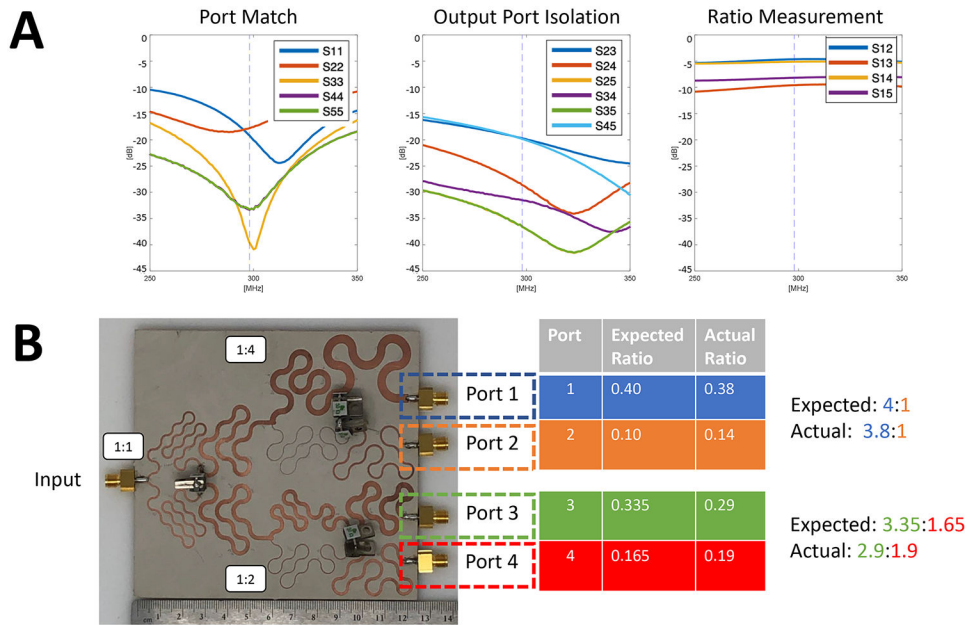


Figure 8: Bench measurements for the two-stage (1 input-to-4 output) board. (A) Bench-measured S-parameters. (B) A photo of the 2-stage board with a table of expected ratios compared to the measured ratios.

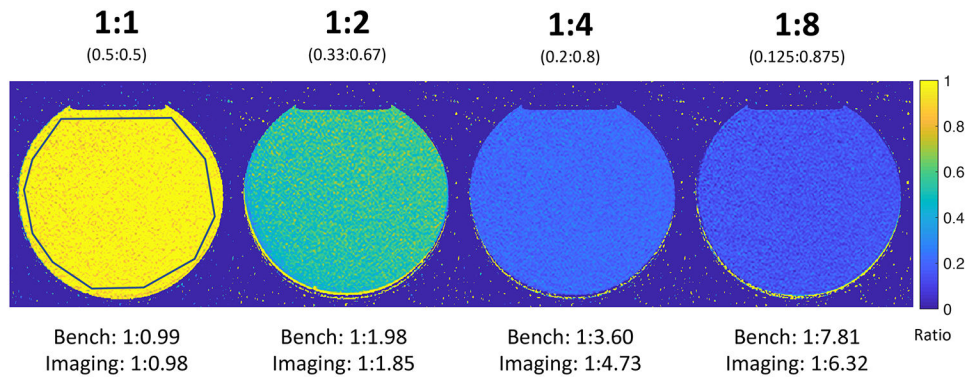


Figure 9: Ratios of small-flip-angle gradient-recalled images collected with each port of each 1 input to 2 output splitter. The ROI for these calculations is plotted in black on the 1:1 splitter's image. Additionally, under the normalized headings the ratio of the power split is included for clarity.

Table 1:

The ratios for each of the power splitters outputs from the simulations, bench tests, and imaging experiments.

Theoretical	Simulation	Bench	Imaging
1:1	1:1.00	1:0.99	1:0.98
1:2	1:1.76	1:1.98	1:1.85
1:4	1:2.13	1:3.60	1:4.73
1:8	1:8.69	1:7.81	1:6.32

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Table 2:

Simulated and bench-measured power losses.

	Simulation	Bench
1:1	1%	5.1%
1:2	2.7%	5.9%
1:4	2.2%	7.2%
1:8	3%	6.7%

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