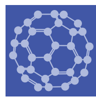 nanomaterials

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Enhancing the Stability and Mobility of TFTs via Indium–Tungsten Oxide and Zinc Oxide Engineered Heterojunction Channels Annealed in Oxygen Ambient

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Abstract: This study demonstrates a significant enhancement in the performance of thin-film transistors (TFTs) in terms of stability and mobility by combining indium–tungsten oxide (IWO) and zinc oxide (ZnO). IWO/ZnO heterojunction structures were fabricated with different channel thickness ratios and annealing environments. The IWO (5 nm)/ZnO (45 nm) TFT, annealed in O_2 ambient, exhibited a high mobility of 26.28 $cm^2/V \cdot s$ and a maximum drain current of 1.54 µA at a drain voltage of 10 V, outperforming the single-channel ZnO TFT, with values of 3.8 $cm^2/V \cdot s$ and 28.08 nA. This mobility enhancement is attributed to the formation of potential wells at the IWO/ZnO junction, resulting in charge accumulation and improved percolation conduction. The engineered heterojunction channel demonstrated superior stability under positive and negative gate bias stresses compared to the single ZnO channel. The analysis of O 1s spectra showed O_I, O_{II}, and O_{III} peaks, confirming the theoretical mechanism. A bias temperature stress test revealed superior charge-trapping time characteristics at temperatures of 25, 55, and 85 °C compared with the single ZnO channel. The proposed IWO/ZnO heterojunction channel overcomes the limitations of the single ZnO channel and presents an attractive approach for developing TFT-based devices having excellent stability and enhanced mobility.

Keywords: thin-film transistors; heterojunction; channel engineering; indium–tungsten oxide; zinc oxide; electron mobility; stability; charge trapping

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1. Introduction

Recently, amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) have attracted significant attention in various industries, including display, semiconductors, and sensors, owing to their excellent characteristics such as low processing temperature, large-area uniformity, and low leakage current [1–6]. Zinc oxide (ZnO) AOS is widely used in next-generation display technologies owing to its high optical transparency and the feasibility of forming smooth thin films on large-area substrates [7–9]. To enhance the properties of conventional ZnO, single AOSs incorporated with additional elements, such as indium, tungsten, and gallium, have been developed, resulting in materials such as zinc–indium oxide (ZIO), tungsten–indium–zinc oxide (WIZO), and indium–gallium–zinc oxide (IGZO) [10–13]. However, these materials have limited mobility, making it challenging to meet the requirements of specific applications [14,15]. High-mobility AOSs, such as indium–zinc oxide (IZO) and zinc oxynitride (ZnON), frequently suffer from insufficient bias stability, leading to a trade-off between mobility and stability in zinc-based AOSs [16–18].

To address these challenges, various approaches, such as optimizing annealing conditions and doping concentrations, forming metal capping layers, and developing heterojunction channel structures, are actively being studied [19–22]. Among these, heterojunction

channel engineering has garnered significant attention for its potential to overcome the limitations of conventional AOS development [23–25]. In this study, we focused on enhancing the characteristics of ZnO channels through heterojunction engineering. Extensive research has been conducted on various factors affecting heterojunction AOS TFTs, including material types, channel thickness and ratios, and annealing conditions [26–28].

In this study, we explored the heterojunctions of indium–tungsten oxide (IWO) and ZnO, given the high indium content and excellent conductivity of IWO. Channels with various thickness ratios were fabricated based on a total AOS channel thickness of 50 nm. The fabricated heterojunction channels were subjected to an annealing process under different ambient conditions (O_2 and air). We analyzed the electrical characteristics and mechanisms of heterojunction-channel TFTs based on the thickness ratios and ambient conditions. The mobility of IWO/ZnO heterojunction TFTs was found to increase, attributed to the potential well formed at the heterointerface. To validate this result, we conducted a series of systematic experiments. First, the optical bandgaps (E_g) of ZnO and IWO were derived using UV–visible spectroscopy and Tauc plots, followed by the extraction of $E_V - E_F$ (E_{FV}) through X-ray photoelectron spectroscopy (XPS) valence band (VB) spectra [29,30]. Based on this, we investigated the alignment of the Fermi energy levels to confirm the formation of the potential well [31]. Moreover, various parameters were calculated and specifically compared based on the transfer curves. The IWO (5 nm)/ZnO (45 nm) channel annealed in O_2 improved the on/off current ratio by more than 30 times to 7.50×10^9 and μ_{FE} by more than 6 times to 26.28 $cm^2/V{\cdot}s$ compared with the ZnO channel. Positive/negative gate bias stress tests were conducted on both the fabricated single and heterojunction channels to confirm the excellent stability of the IWO/ZnO heterojunction channel. An XPS O 1s analysis helped investigate the chemical bonding states of the IWO film depending on the annealing ambient conditions. This theoretical explanation elucidates the reasons behind the performance and stability improvements in the proposed heterojunction TFT. To ensure comprehensive reliability, additional stability evaluations were performed on both the optimal heterojunction channel and the single ZnO channel under various temperature conditions [32–34]. By analyzing the threshold voltage shifts in TFTs under bias and temperature stress, we confirmed the excellent charge-trapping characteristics and structural stability of IWO/ZnO. The IWO (5 nm)/ZnO (45 nm) heterojunction-channel TFT annealed in O_2 ambient demonstrated remarkable improvements in terms of both mobility and stability compared with the single-ZnO-channel TFT. This advancement signifies notable progress in the development of ZnO channels through heterojunction engineering using IWO materials, contributing to the broader development of oxide semiconductor technology.

2. Materials and Methods

2.1. Material Specifications

We employed the following materials in the fabrication of the TFTs: a p-type Si substrate (orientation (100); resistivity range: 1–10 Ω·cm; LG Siltron Inc., Gumi, Republic of Korea), an IWO sputter target (In_2O_3:WO_3 = 99:1 wt%, THIFINE Co., Ltd., Incheon, Republic of Korea), ZnO sputter targets (purity > 99.99%, THIFINE Co., Ltd.), and Al pellets (purity > 99.99%, THIFINE Co., Ltd.).

2.2. AOS Structure and Transistor Fabrication Process

Figure 1 shows the schematics of the fabricated ZnO and IWO/ZnO TFTs. The substrate used was a heavily doped p-type Si wafer with a 100 nm thick thermally grown SiO_2 layer. This was followed by the deposition of the AOS channel and source/drain on top of the substrate. ZnO and IWO were deposited using radio frequency (RF) magnetron sputtering. For the single-channel TFT, ZnO was deposited to a thickness of 50 nm. In the case of the heterojunction-channel TFTs, IWO with thicknesses of 5, 10, and 20 nm was used as the front channel, while ZnO with thicknesses of 45, 40, and 30 nm was deposited on the back, resulting in a total thickness of 50 nm. For heterojunction channels,

IWO and ZnO were deposited through a continuous sputtering process to minimize the influence of impurities at the different AOS junction interfaces. The channel width and length were 120 µm and 60 µm, respectively. All the devices underwent a conventional thermal annealing process at 300 °C for 30 min under varying ambient conditions of air and oxygen. Al electrodes, 150 nm thick, were deposited using electron beam evaporation for the source/drain (S/D), and patterning was performed using the lift-off method. The width and length of the S/D electrodes were 150 µm and 120 µm, respectively.

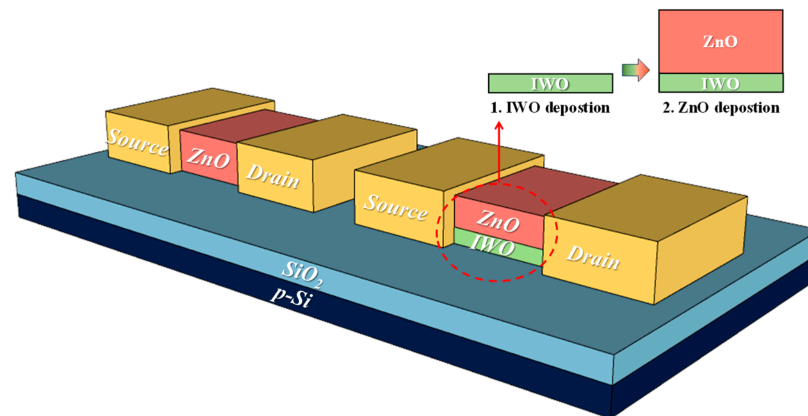

Figure 1. Schematic illustration of a TFT featuring a single ZnO channel and an IWO/ZnO heterojunction channel.

2.3. Characterization Method

The transfer and output characteristics of the single- and heterojunction-channel TFTs were evaluated using an Agilent 4156B precision semiconductor parameter analyzer (Hewlett-Packard Co., Palo Alto, CA, USA). All the electrical measurements were conducted inside an electromagnetically shielded dark box to minimize external interference, such as noise signals and optical noise, at room temperature with a relative humidity of approximately 25%. Thermal instability evaluations were performed using a Cascade Microtech M150 probe station with an ERS AC3 chuck for temperature control. The thicknesses of the IWO, ZnO, and Al films were measured using a Dektak XT Bruker stylus profiler (Bruker, Hamburg, Germany). The optical transmittances of the films were measured using an Agilent 8453 UV–visible spectrophotometer (Hewlett-Packard Co., USA) over a wavelength range of 300–800 nm. Moreover, the film composition and chemical bonding states were investigated using a K-Alpha + XPS system (Thermo Fisher Scientific, Sunnyvale, CA, USA) with a monochromated Al X-ray source (Al Kα line: 1486.6 eV).

3. Results and Discussion

3.1. Improvement in the Electron Mobility of Engineered Heterojunction AOS

To enhance the electron mobility in a single ZnO channel, heterojunction engineering was employed using an IWO front channel (known for its superior conductivity owing to a high indium content) and a ZnO back channel with comparatively lower conductivity. The junction between IWO and ZnO creates energy band bending that forms a potential well, facilitating electron accumulation and supporting enhanced mobility [35]. The thickness ratio of each AOS material in the heterojunction and the annealing ambient conditions play crucial roles in shaping the parameters observed in the TFT transfer curve [36]. The band diagram resulting from the IWO/ZnO junction was calculated to elucidate the mechanism behind mobility improvement through the heterojunction. The TFTs were fabricated with a single-ZnO-channel thickness of 50 nm, varying thickness ratios, and annealing ambient conditions for the IWO/ZnO heterojunction channel. A parameter analysis was conducted based on the transfer curve measurements, focusing on the conductivity characteristics extracted from threshold voltage values ranging from −1 to 1 V in the output characteristics.

Figure 2a,b show the optical transmittance and $(\alpha h\nu)^2$ versus the hν plots for IWO and ZnO. E_g was determined using the Tauc plot method with Equations (1) and (2) [37,38].

$$\alpha = \frac{1}{t}\ln\left(\frac{1}{T}\right) \tag{1}$$

$$\alpha h\nu = \left(h\nu - E_g\right)^{1/2} \tag{2}$$

where α is the absorption coefficient, T is the transmittance, and t is the film thickness. In the photon energy ($h\nu$), h is Planck's constant, and ν is the frequency of the incident photon. The E_g values extracted for IWO and ZnO were 3.20 eV and 3.36 eV, respectively, extrapolated from the linear region of $(\alpha h\nu)^2$ versus $h\nu$ where $\alpha = 0$. Further, XPS VB spectra measurements (Figure 2c) provided E_{FV} values of 2.68 eV for IWO and 2.89 eV for ZnO, obtained from the intersection of the linearly fitted leading edge with the X-axis (binding energy). The energy band diagram of the heterojunction AOS (Figure 2d) shows that when IWO and ZnO form a junction, electrons migrate from IWO to ZnO, aligning with the overall Fermi energy levels. This results in the upward bending of the energy bands of IWO and the downward bending of ZnO, creating a potential well at the IWO/ZnO interface [39–41]. The accumulation of electrons in this potential well enhances the field-effect mobility by mitigating conductivity-limiting effects caused by traps at the insulator and channel interface, thereby significantly improving the percolation conduction properties [42,43].

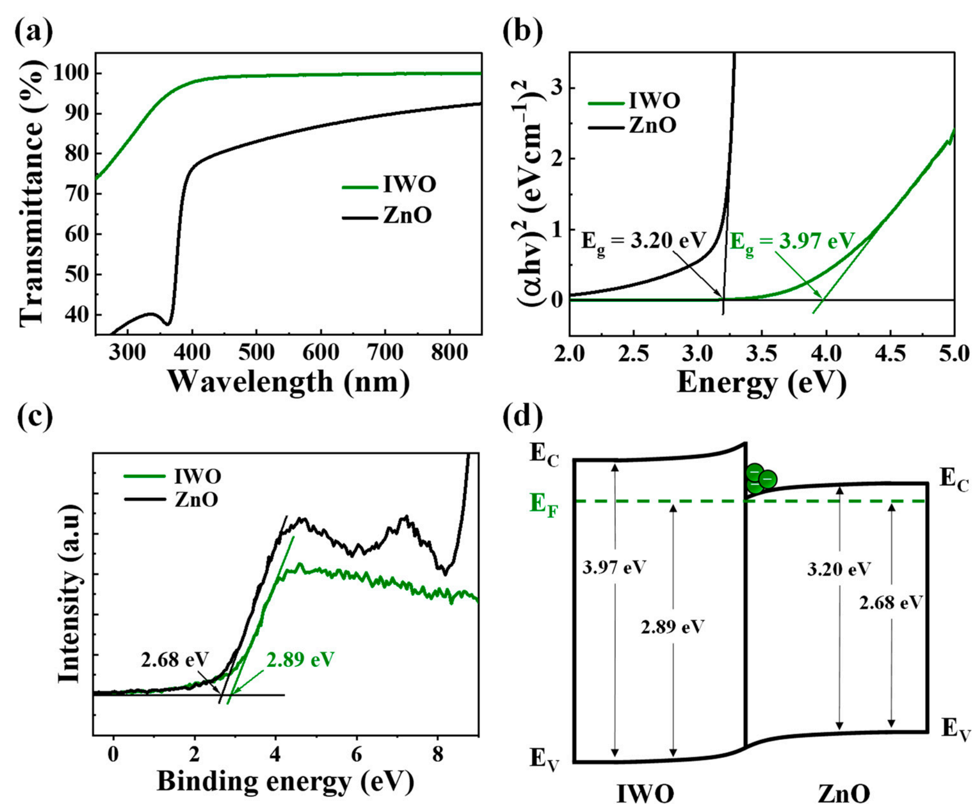

Figure 2. (**a**) Optical transmittance spectra; (**b**) plots of $(\alpha h\nu)^2$ versus $h\nu$; (**c**) XPS spectra showing the valence band edge; (**d**) energy band diagram for IWO and ZnO.

Figure 3a,b show the transfer curves of single-channel and IWO/ZnO heterojunction-channel TFTs, each with a total thickness of 50 nm, under varying annealing ambient conditions (air, O_2). The gate voltage (V_G) was swept from −20 to 40 V, while the drain voltage (V_D) was fixed at 10 V. Table 1 presents the key electrical performance parameters including the threshold voltage (V_{th}), field-effect mobility (μ_{FE}), subthreshold swing (SS),

and on/off current ratio ($I_{ON/OFF}$). Each extracted parameter represents the mean value, with the standard deviation falling within an acceptable range.

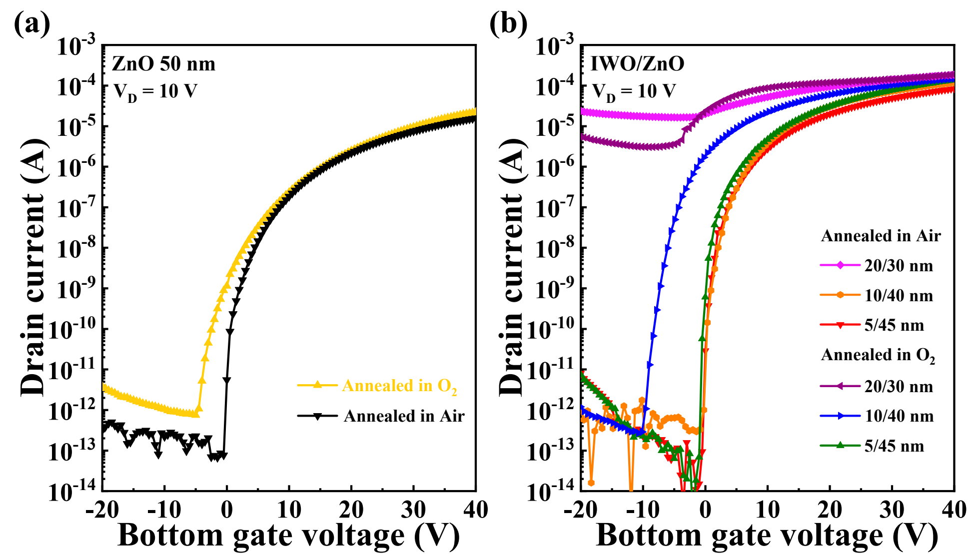

Figure 3. Transfer curves for (**a**) ZnO TFT and (**b**) IWO/ZnO TFT under different annealing ambient conditions.

Table 1. Variations in the threshold voltage, mobility, and on/off current ratio under different annealing ambient conditions and channel thicknesses.

Channel Type (Ambient)	V_{th} [V]	μ_{FE} [cm^2/V·s]	$S.S$ [V/dec]	$I_{ON/OFF}$ [A/A]
ZnO (O_2)	−2.65	7.14	0.72	1.61×10^7
[A] ZnO (Air)	0.48	3.80	0.27	2.04×10^8
10/40 (O_2)	−8.37	26.54	0.54	4.06×10^8
[B] 10/40 (Air)	0.25	28.89	0.27	5.03×10^8
[C] 5/45 (Air)	0.19	18.24	0.20	5.61×10^9
[D] 5/45 (O_2)	−0.44	26.28	0.17	7.50×10^9

V_{th} was determined using the constant-current method normalized by the channel width and length, while $I_{ON/OFF}$ was defined as the maximum on current divided by the minimum off current within the V_G sweep range. The field-effect mobility (μ_{FE}) was calculated as follows [44]:

$$\mu_{FE} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2 \quad (3)$$

where C_i is the capacitance per unit area, W is the channel width, and L is the channel length. The subthreshold swing (SS) was determined as follows [45]:

$$S.S = \frac{\partial V_G}{\partial log I_D} \quad (4)$$

When comparing the V_{th} values, the ZnO TFT exhibited a V_{th} of 0.48 V in air ambient, demonstrating superior characteristics compared with that observed under O_2 ambient (−2.65 V). Meanwhile, for the heterojunction channel in the front IWO thickness/back ZnO thickness (annealed ambient) configurations of 10/40 (O_2), 10/40 (air), 5/45 (O_2), and 5/45 (air), the V_{th} values were −8.37, 0.25, −0.44, and 0.19 V, respectively. In particular, the 20/30 channel configuration showed limited on/off operation due to the high conductivity of the 20 nm thick IWO layer, regardless of the post-annealing ambient in O_2 or air. Except

for the 20/30 (O_2), 20/30 (air), and 10/40 (O_2) configurations, all configurations exhibited V_{th} characteristics within the range of −1 to 1 V. In terms of μ_{FE}, ZnO (O_2), ZnO (air), 10/40 (O_2), 10/40 (air), 5/45 (O_2), and 5/45 (air) demonstrated values of 7.14, 3.8, 26.54, 28.89, 26.28, and 18.24 $cm^2/V\cdot s$, respectively. This highlights the significant enhancement in μ_{FE} for the IWO/ZnO heterojunction channel compared with the single ZnO channel. In particular, the 5/45 (O_2) configuration exhibited an $I_{ON/OFF}$ of 7.50 × 10^9 and an SS of 0.17 V/dec, indicating a superior electrical performance across all the extracted parameters.

Based on a comprehensive analysis of the parameters extracted from Figure 3, additional electrical characteristic analyses were conducted for ZnO (air), 10/40 (air), 5/45 (O_2), and 5/45 (air) TFTs. Figure 4a shows the schematic of the channel structures for the selected TFTs. For convenient classification, ZnO (air) is denoted by A, 10/40 (air) is denoted by B, 5/45 (air) is denoted by C, and 5/45 (O_2) is denoted by D. Figure 4b–e present the output curves of the selected channels (A–D). V_D was swept from 0 to 10 V, and $|V_G–V_{th}|$ was varied in 11 steps from 0 to 7 V. All four types of TFTs exhibited clear linear and saturation regions in the output curves, with the maximum saturation currents being 28.08 nA (A), 1.50 μA (B), 1.26 μA (C), and 1.54 μA (D), respectively. The I_D value of the heterojunction channels was more than 30 times higher than that of the single channel. The high I_D in the heterojunction TFTs indicates better driving capability compared with the single-channel TFT, consistent with the improved mobility inferred from the transfer curves.

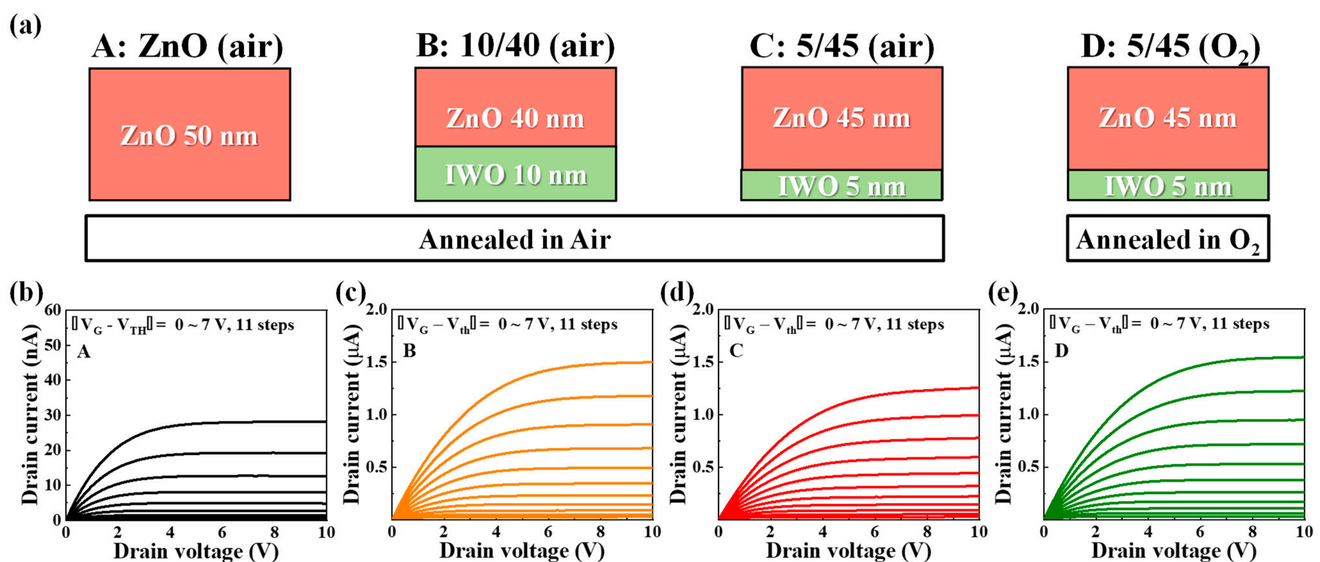

Figure 4. (**a**) Schematic representation of channel structures and annealing conditions for selected TFTs. Output curve characteristics for (**b**) ZnO (air) [A], (**c**) IWO/ZnO (10 nm/40 nm, air) [B], (**d**) IWO/ZnO (5 nm/45 nm, air) [C], and (**e**) IWO/ZnO (5 nm/45 nm, O_2) [D].

3.2. Stability of Heterojunction AOS under Gate Bias Stress

Evaluating the instability of TFT devices under gate bias stress is essential for understanding the potential degradation characteristics such as the threshold voltage shift (ΔV_{th}), mobility reduction, and increased leakage current in the proposed heterojunction channels [46]. This is a critical factor for long-term operation and practical applications. Therefore, we conducted stability evaluations under positive and negative gate bias stresses for TFTs of types A, B, C, and D. Moreover, the physical mechanisms behind the ΔV_{th} characteristics of the transfer curves under the gate bias stress are clearly explained through the analysis of the O 1s spectra.

Figure 5a shows the changes in the transfer curves of TFTs with channel structures A–D under a positive gate bias stress (PGBS). The PGBS was applied at V_G = 30 V for 3600 s, and the transfer curves were measured by sweeping V_G from −30 to 30 V. Figure 5b shows ΔV_{th} over the stress time during PGBS application. With the increase in the stress

time, the V_{th} values of all the TFTs shifted in the positive direction. Heterojunction-channel TFTs generally exhibited superior V_{th} stability compared with single-channel TFTs. The single ZnO channel (A) showed a ΔV_{th} of 2.93 V, while the heterojunction channels showed ΔV_{th} values of 0.36 V (B), 1.35 V (C), and 0.34 V (D), respectively. Under PGBS conditions, ΔV_{th} is primarily attributed to electron trapping at the interface between the channel and gate insulator [47,48]. The conductive IWO layer, rich in indium content, has a high electron concentration. Consequently, numerous electrons in the IWO already occupy interfacial trap sites during PGBS. This phenomenon resulted in high V_{th} stability for B. For C, the reduction in the IWO thickness from 10 to 5 nm resulted in greater ΔV_{th} instability. This is interpreted as a consequence of the relative decrease in the electron concentration, leading to an increase in the unoccupied interfacial trap sites. However, the D TFT showed significantly improved PGBS stability despite the IWO layer thickness being 5 nm. This is interpreted as a result of oxygen annealing improving the interface between the channel and dielectric layers, as well as reducing impurities such as OH^- within the IWO channel, thereby decreasing the interfacial trap sites that can be occupied by electrons. This is explained according to the O 1s spectra analysis obtained from XPS.

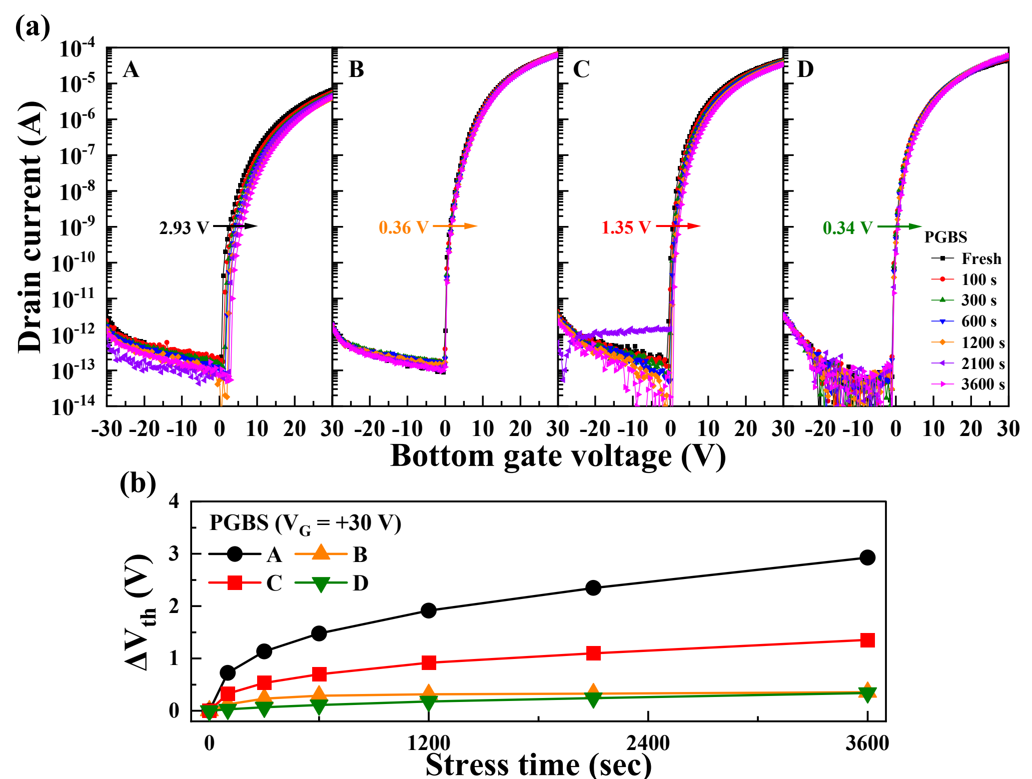

Figure 5. (**a**) Transfer curve instability of ZnO and IWO/ZnO TFTs under positive gate bias stress (PGBS) with V_G = + 30 V; (**b**) variation in the threshold voltage (V_{th}) as a function of the stress time.

The impact of heterojunction channel types on the stability under negative gate bias stress (NGBS) was also investigated. Figure 6a illustrates the changes in the transfer curves of TFTs with channels A–D under NGBS conditions. NGBS was applied at V_G = −30 V for 3600 s, with V_G swept from −30 to 30 V. Figure 6b shows ΔV_{th} during the NGBS. Channel A showed a ΔV_{th} of −0.64 V, while heterojunction channels B, C, and D recorded ΔV_{th} values of −2.22, −1.56, and −0.69 V, respectively, demonstrating varying stability depending on the channel type. ΔV_{th} during NGBS can be primarily attributed to the additional free electrons caused by oxygen vacancy defects near the channel and gate insulator interface [49,50]. Under NGBS, as holes accumulate at the interface, oxygen vacancies (V_O) transition to V_O^{1+} or V_O^{2+}, releasing electrons ($V_O + h^+ \longrightarrow V_O^{1+} + e^-$ or $V_O + 2h^+ \longrightarrow V_O^{2+} + 2e^-$) [51]. This process increases the electron concentration in the

channel layer, consequently shifting V_{th} in the negative direction. In B, the presence of V_O in the interfacial IWO layer was a major factor in reducing NGBS stability by generating more doubly ionized oxygen vacancies (V_O^{2+}) in the channel under NGBS conditions. As the thickness of the front IWO layer decreased in C, the reduction in the front IWO layer thickness led to a decrease in V_O, thereby improving the NGBS stability. D, annealed in oxygen, exhibited reduced V_O compared with C, which was annealed in air, demonstrating the highest NGBS stability among the fabricated heterojunction channels. The results regarding V_O under the annealing ambient conditions are explained in Figure 7.

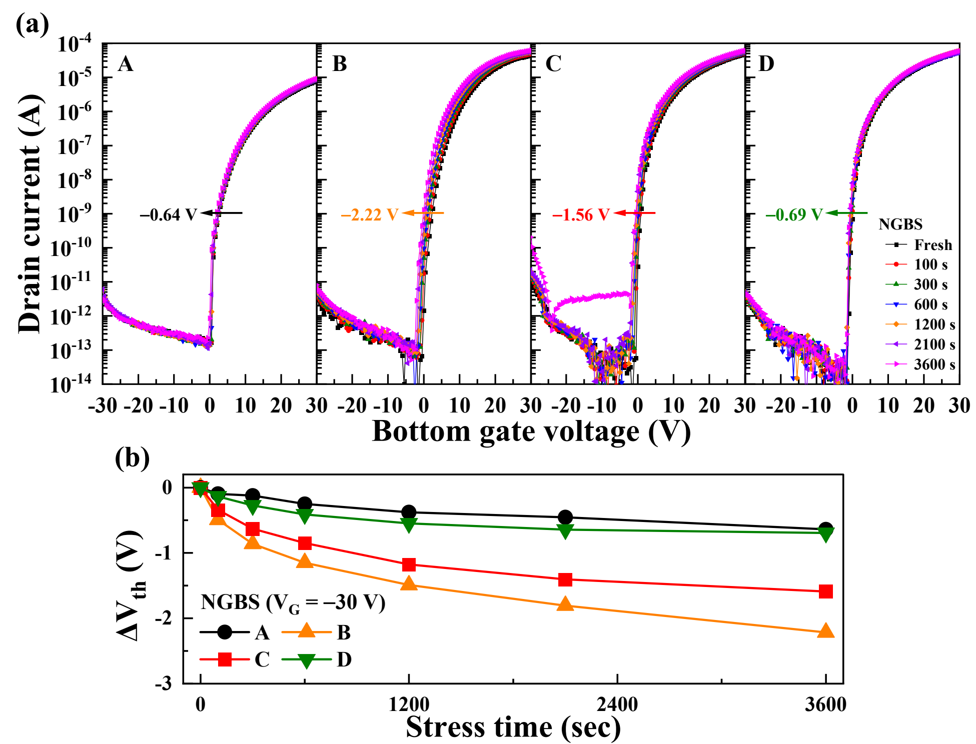

Figure 6. (**a**) Instability of the transfer curves for ZnO and IWO/ZnO TFTs under NGBS with $V_G = -30$ V; (**b**) variation in V_{th} as a function of the stress time.

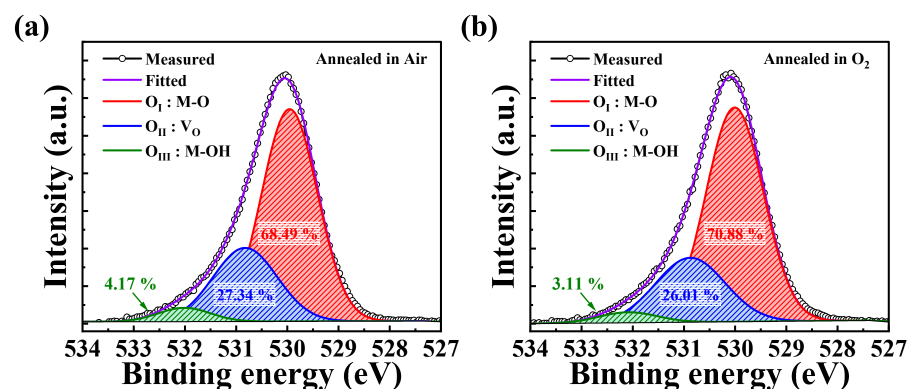

Figure 7. XPS analysis of the O 1s spectra of IWO films under different annealing ambient conditions: (**a**) air and (**b**) O_2.

As part of the mechanism analysis of the ΔV_{th} results under gate bias stress, we conducted an XPS analysis of IWO thin films under different annealing ambient conditions (air, O_2). Figure 7a,b show the O 1s spectra obtained from the XPS analysis. These spectra can be divided into three subpeaks, designated as O_I, O_{II}, and O_{III}, centered at binding energies of 530.1 ± 0.2 eV, 530.8 ± 0.2 eV, and 532.1 ± 0.2 eV, respectively, using Gaussian

fitting [52–54]. Each peak corresponds to different chemical states, namely metal–oxygen (M–O) bonds, oxygen vacancies (V_O), and impurities such as hydroxyl groups (-OH), which are known as trapping sites at the interface [55]. The IWO layer annealed in O_2 showed an increase in the M–O bond ratio from 68.49% to 70.88% compared with the IWO layer annealed in air. Moreover, the ratios of V_O and -OH decreased from 27.34% to 26.01% and from 4.17% to 3.11%, respectively. As a result, an analysis of the O 1s spectra from the D TFT annealed in O_2 ambient indicates that the increase in the M–O concentration enhances the percolation conduction path, thereby improving mobility [56,57]. The reduction in V_O decreases electron emission, enhancing the stability under NGBS conditions. Further, a decrease in the -OH concentration indicates a reduction in the number of impurities within the channel layer, contributing to excellent stability under PGBS conditions [58].

3.3. Reliability Evaluation of Heterojunction Channel under Bias Temperature Stress

Based on comprehensive evaluation results, heterojunction channel D demonstrated excellent performance as a transistor through process optimization and exhibited outstanding stability even under high voltage stress. To further assess the reliability of the D TFT, we conducted a thermal stability test under bias. Since thermal stress significantly affects electron mobility and trap states, it ensures the long-term reliability of the TFT [59]. In this study, we detailed the effects of charge trapping and defects under high-voltage negative and positive bias temperature stresses. Figure 8a,b present the ΔV_{th} values of A and D over time under positive bias temperature stress (PBTS) and negative bias temperature stress (NBTS) at various temperatures. The PBTS and NBTS tests were conducted at 25, 55, and 85 °C with $V_G = V_{th0} \pm 30$ V for 3600 s, where V_{th0} represents the initial V_{th} before applying the gate bias stress. The ΔV_{th} values of all the TFTs increased proportionally with time and temperature. During PBTS, the ΔV_{th} values for A and D were measured to be 2.80 and 0.50 V at 25 °C, 5.72 and 1.04 V at 55 °C, and 7.60 and 2.03 V at 85 °C, respectively. During NBTS, the ΔV_{th} values for A and D were −0.68 and −0.70 V at 25 °C, −1.75 and −1.26 V at 55 °C, and −4.05 and −2.47 V at 85 °C, respectively. As a result, A exhibited a high increase rate of ΔV_{th} with increasing stress temperature, whereas D maintained a relatively stable ΔV_{th} even under high-temperature stress conditions. Notably, under NBTS conditions, both channels exhibited similar ΔV_{th} at 25 °C, but as the temperature increased to 55 °C and 85 °C, the ΔV_{th} value of A increased significantly. This indicates that heterojunction channel D provides excellent stability under thermal stress. The experimental data for ΔV_{th} were fitted using a stretched-exponential equation, defined as follows [60,61]:

$$\Delta V_{th}(t) = \Delta V_{th0}\left\{1 - exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{5}$$

where ΔV_{th0} is $\Delta V_{th}(t)$ at infinite time; β is the stretched-exponential exponent; t is the stress time; and τ represents the characteristic charge-trapping time from the channel to the dielectric layer, which depends on the temperature. The dotted line in Figure 8a and the solid line in Figure 8b are fitted using the stretched-exponential equation, showing a good agreement with the experimental results. This suggests that ΔV_{th} in the gate bias temperature stress evaluation is due to a thermally activated charge-trapping mechanism.

Figure 9a,b depict the τ values extracted from the time-dependent ΔV_{th} during the PBTS and NBTS tests shown in Figure 8a,b; τ represents the time for carriers to become trapped within the insulator or at the interface between the channel and insulator. In the stretched-exponential equation, τ for thermally activated carriers is expressed as follows:

$$\tau = \tau_0 exp\left(\frac{E_\tau}{k_B T}\right) = \nu^{-1} exp\left(\frac{E_\tau}{k_B T}\right) \tag{6}$$

where the thermal activation energy is denoted by $E_a = E_\tau \beta$, with E_τ representing the average effective energy barrier that electrons in the channel must overcome before entering

the gate insulator [62]. Here, τ_0 is the thermal pre-factor, and ν is the frequency pre-factor for emission over the barrier.

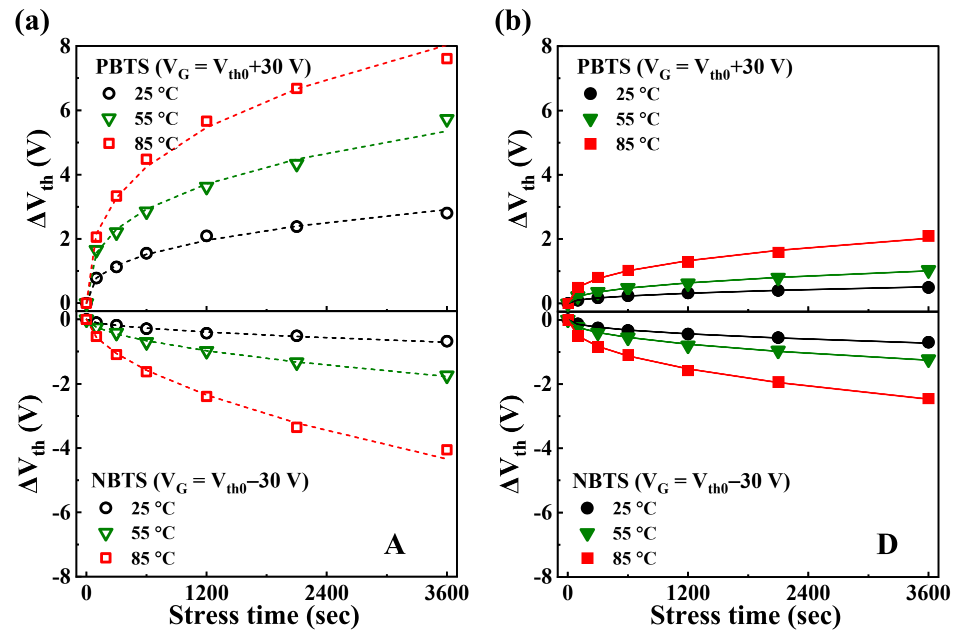

Figure 8. Temperature dependence of ΔV_{th} under PBTS (V_G = V_{th0} + 30 V) and NBTS (V_G = V_{th0} − 30 V) tests for (**a**) A and (**b**) D devices, conducted at 25, 55, and 85 °C. The curves were fitted using the stretched-exponential equation.

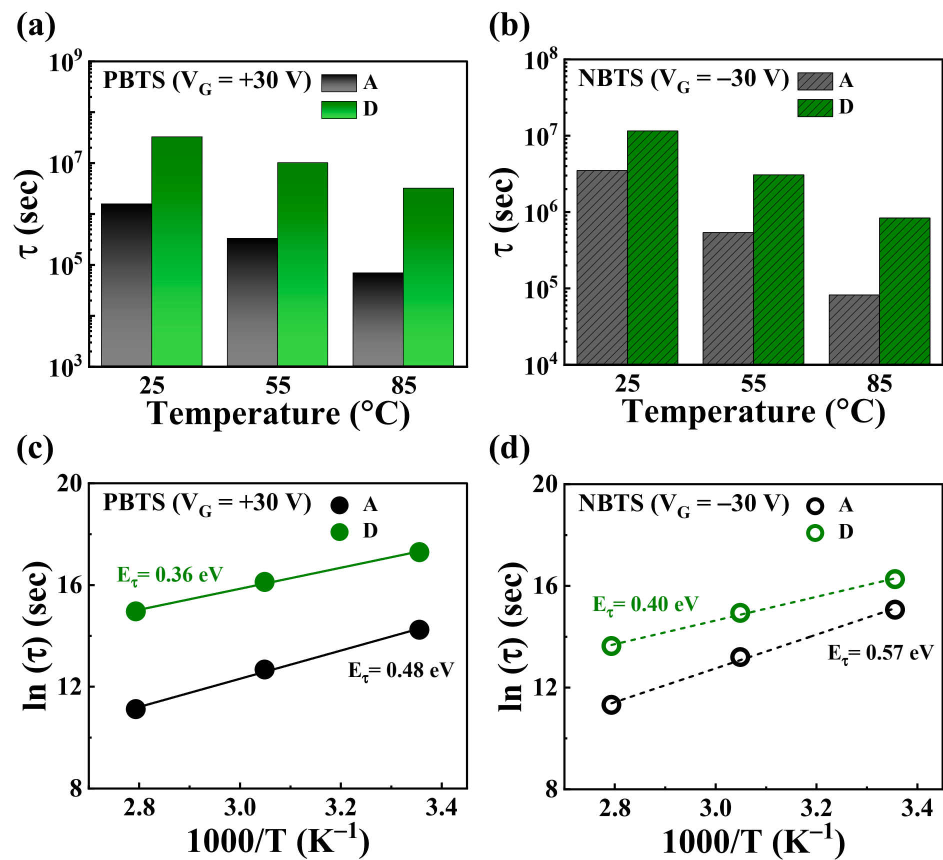

Figure 9. Box plots of the charge-trapping time (τ) for A and D during (**a**) PBTS and (**b**) NBTS. Arrhenius plots of ln(τ) versus the reciprocal of the temperature during (**c**) PBTS and (**d**) NBTS tests.

Table 2 presents the values of τ and β calculated using this equation. During PBTS and NBTS, Device D exhibited significantly higher τ values across all the tested temperatures. Specifically, at 25 °C, the τ values were 21 and 3 times higher for D compared with A. At 55 °C, they were 31 and 5 times higher, and at 85 °C, they were 46 and 10 times higher. While τ values gradually decreased with increasing test temperature for both devices, the decrease was more pronounced in Device A. This suggests potential long-term reliability issues in Device A due to rapid carrier trapping.

Table 2. Charge-trapping time (τ) and stretched-exponential exponent (β) extracted from ΔV_{th} measurements for TFTs A and D.

Temperature [°C]	**PBTS**				**NBTS**			
	A		**D**		**A**		**D**	
	τ	β	τ	β	τ	β	τ	β
25	1.5×10^6	0.38	3.2×10^7	0.54	3.5×10^6	0.44	1.2×10^7	0.46
55	3.2×10^5	0.36	1.0×10^7	0.56	5.4×10^5	0.43	3.0×10^6	0.47
85	6.7×10^4	0.39	3.1×10^6	0.58	8.2×10^4	0.41	8.4×10^5	0.45

Figure 9c,d present the Arrhenius plots of ln(τ) versus the reciprocal of the absolute temperature ($1/T$) for TFTs in Device A and Device D during PBTS and NBTS tests. The linear relationship between ln(τ) and $1/T$ indicates a thermally activated charge-trapping process. In these plots, the slope corresponds to E_τ for charge transport. Under PBTS, A and D exhibited E_τ values of 0.36 eV and 0.48 eV, respectively, while under NBTS, these values were 0.40 eV and 0.57 eV, respectively. Lower E_τ values are associated with fewer defects and a more ordered channel structure, suggesting that heterojunction channel D can mitigate charge-trapping issues and enhance device reliability [63].

Finally, as part of the evaluation of the enhanced performance and reliability of the proposed optimal heterojunction TFT, a comparison was conducted with reported single-channel IWO and ZnO TFTs. Table 3 presents the key electrical performance parameters and gate bias stability characteristics of the single-channel IWO and ZnO TFTs deposited through sputtering, as well as the heterojunction TFTs fabricated in this study. To ensure reliable results in the gate bias stability evaluation, the ΔV_{th} values for each group were compared under similar stress durations (approximately 3600 s). Compared to all single-channel TFTs, the proposed heterojunction TFT showed competitive mobility (26.28 $cm^2/V{\cdot}s$) and excellent stability (ΔV_{th} under PGBS = 0.34 V, ΔV_{th} under NGBS = −0.97 V). In particular, compared to single-channel ZnO TFT, the mobility was more than double, and the ΔV_{th} values were significantly lower, indicating superior reliability.

Table 3. Comparison of key electrical performance parameters and gate bias stability of heterojunction and single-channel TFTs from the literature and this work.

Channel Layer	**Gate Insulator /Thickness [nm]**	V_{th} **[V]**	μ_{FE} **[cm²/V·s]**	*S.S* **[V/dec]**	ΔV_{th} **under PGBS [V]**	ΔV_{th} **under NGBS [V]**	**Ref.**
ZnO	SiO_2/100	4.3 ± 0.5	11.5 ± 1.3	0.65 ± 0.08	8.7 ± 0.8	−9.6 ± 0.9	[64]
ZnO	SiO_2/150	15	8.1	1.35	3	N/A	[65]
ZnO	SiO_2/100	4.1 ± 0.6	10.5 ± 0.5	0.45 ± 0.07	2.7	−3.2	[66]
IWO	SiO_2/100	−3.4	36.7	0.39	≈2.5	N/A	[67]
IWO	SiO_2/100	0.5	27.55	0.5	4.5	−0.92	[68]
IWO	SiO_2/100	−0.5	21.7	0.47	N/A	N/A	[69]
[D] IWO/ZnO	SiO_2/100	−0.44	26.28	0.17	0.34	−0.97	This work

4. Conclusions

Single-phase ZnO channels are associated with limitations in terms of their electron mobility and stability. To address these issues, we engineered heterojunction channels using IWO/ZnO structures, resulting in significant performance improvements. First, energy band diagrams were computed for IWO and ZnO junctions, elucidating the mechanism behind the improved electron mobility in the IWO/ZnO heterojunction channel. The extracted parameters from the transfer curves (μ_{FE} = 26.28 cm^2/V·s, $I_{ON/OFF}$ = 7.5 × 10^9, SS = 0.17 V/dec) demonstrated substantial performance improvements compared with single ZnO channels, corroborating theoretical expectations. Further, under PGBS testing, the maximum ΔV_{th} values for IWO/ZnO and single ZnO were 0.34 V and 2.93 V, respectively, highlighting a significant difference of 2.59 V, which is crucial for the reliability of TFTs. Moreover, an O 1s XPS analysis of IWO films under varied annealing ambient conditions distinctly illustrated the basis for superior mobility and stability in the optimized heterojunction channel. Finally, an analysis of the parameters derived from bias temperature stress evaluations confirmed the superior charge-trapping characteristics and structural stability within the channel compared with the single ZnO channels.

In conclusion, the IWO/ZnO heterojunction channel exhibited promising potential for advancing high-performance oxide semiconductors, overcoming the mobility and stability limitations encountered in both single ZnO channels and previously known oxide semiconductors.

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References

1. Kamiya, T.; Nomura, K.; Hosono, H. Present status of amorphous in-Ga-Zn-O thin-film transistors. *Sci. Technol. Adv. Mater.* **2010**, *11*, 044305. [CrossRef] [PubMed]
2. Fortunato, E.; Barquinha, P.; Martins, R. Oxide semiconductor thin-film transistors: A review of recent advances. *Adv. Mater.* **2012**, *24*, 2945–2986. [CrossRef] [PubMed]
3. Yabuta, H.; Sano, M.; Abe, K.; Aiba, T.; Den, T.; Kumomi, H.; Nomura, K.; Kamiya, T.; Hosono, H. High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature rf-magnetron sputtering. *Appl. Phys. Lett.* **2006**, *89*, 112123. [CrossRef]
4. Nathan, A.; Lee, S.; Jeon, S.; Robertson, J. Amorphous oxide semiconductor TFTs for displays and imaging. *J. Display Technol.* **2014**, *10*, 917–927. [CrossRef]
5. Petti, L.; Münzenrieder, N.; Vogt, C.; Faber, H.; Büthe, L.; Cantarella, G.; Bottacchi, F.; Anthopoulos, T.D.; Tröster, G. Metal oxide semiconductor thin-film transistors for flexible electronics. *Appl. Phys. Rev.* **2016**, *3*, 021303. [CrossRef]
6. Shi, J.; Zhang, J.; Yang, L.; Qu, M.; Qi, D.C.; Zhang, K.H.L. Wide bandgap oxide semiconductors: From materials physics to optoelectronic devices. *Adv. Mater.* **2021**, *33*, e2006230. [CrossRef] [PubMed]
7. Fortunato, E.M.; Barquinha, P.M.; Pimentel, A.C.M.B.G.; Gonçalves, A.M.; Marques, A.J.; Pereira, L.M.; Martins, R.F. Fully transparent ZnO thin-film transistor produced at room temperature. *Adv. Mater.* **2005**, *17*, 590–594. [CrossRef]
8. Park, S.H.K.; Hwang, C.S.; Ryu, M.; Yang, S.; Byun, C.; Shin, J.; Lee, J.I.; Lee, K.; Oh, M.S.; Im, S. Transparent and Photo-stable ZnO Thin-film Transistors to Drive an Active Matrix Organic-Light- Emitting-Diode Display Panel. *Adv. Mater.* **2009**, *21*, 678–682. [CrossRef]
9. Zhang, L.; Zhang, H.; Bai, Y.; Ma, J.W.; Cao, J.; Jiang, X.; Zhang, Z.L. Enhanced performances of ZnO-TFT by improving surface properties of channel layer. *Solid State Commun.* **2008**, *146*, 387–390. [CrossRef]

10. Chauhan, R.N.; Tiwari, N.; Shieh, H.P.D.; Liu, P.T. Electrical performance and stability of tungsten indium zinc oxide thin-film transistors. *Mater. Lett.* **2018**, *214*, 293–296. [CrossRef]
11. Chauhan, R.N.; Tiwari, N.; Liu, P.T.; Shieh, H.P.D.; Kumar, J. Silicon induced stability and mobility of indium zinc oxide based bilayer thin film transistors. *Appl. Phys. Lett.* **2016**, *109*, 202107. [CrossRef]
12. Choi, J.Y.; Heo, K.; Cho, K.S.; Hwang, S.W.; Chung, J.; Kim, S.; Lee, B.H.; Lee, S.Y. Effect of Si on the energy band gap modulation and performance of silicon indium zinc oxide thin-film transistors. *Sci. Rep.* **2017**, *7*, 15392. [CrossRef] [PubMed]
13. Park, H.W.; Song, A.; Choi, D.; Kim, H.J.; Kwon, J.Y.; Chung, K.B. Enhancement of the device performance and the stability with a homojunction-structured tungsten indium zinc oxide thin film transistor. *Sci. Rep.* **2017**, *7*, 11634. [CrossRef] [PubMed]
14. Park, J.S.; Maeng, W.J.; Kim, H.S.; Park, J.S. Review of recent developments in amorphous oxide semiconductor thin-film transistor devices. *Thin Solid Films* **2012**, *520*, 1679–1693. [CrossRef]
15. Itagaki, N.; Iwasaki, T.; Kumomi, H.; Den, T.; Nomura, K.; Kamiya, T.O.S.H.I.O.; Hosono, H. Zn–In–O based thin-film transistors: Compositional dependence. *Phys. Status Solidi (a)* **2008**, *205*, 1915–1919. [CrossRef]
16. Shiah, Y.S.; Sim, K.; Shi, Y.; Abe, K.; Ueda, S.; Sasase, M.; Kim, J.; Hosono, H. Mobility–stability trade-off in oxide thin-film transistors. *Nat. Electron.* **2021**, *4*, 800–807. [CrossRef]
17. Paine, D.C.; Yaglioglu, B.; Beiley, Z.; Lee, S. Amorphous IZO-based transparent thin film transistors. *Thin Solid Films* **2008**, *516*, 5894–5898. [CrossRef]
18. Lee, E.; Benayad, A.; Shin, T.; Lee, H.; Ko, D.S.; Kim, T.S.; Son, K.S.; Ryu, M.; Jeon, S.; Park, G.S. Nanocrystalline ZnON.; High mobility and low band gap semiconductor material for high performance switch transistor and image sensor application. *Sci. Rep.* **2014**, *4*, 4948. [CrossRef] [PubMed]
19. Lee, B.H.; Sohn, A.; Kim, S.; Lee, S.Y. Mechanism of carrier controllability with metal capping layer on amorphous oxide SiZnSnO semiconductor. *Sci. Rep.* **2019**, *9*, 886. [CrossRef]
20. Zhang, X.; Lee, H.; Kwon, J.H.; Kim, E.J.; Park, J. Low-concentration indium doping in solution-processed zinc oxide films for thin-film transistors. *Materials* **2017**, *10*, 880. [CrossRef]
21. Barquinha, P.; Gonçalves, G.; Pereira, L.; Martins, R.; Fortunato, E. Effect of annealing temperature on the properties of IZO films and IZO based transparent TFTs. *Thin Solid Films* **2007**, *515*, 8450–8454. [CrossRef]
22. Lee, J.; Chung, D.S. Heterojunction oxide thin film transistors: A review of recent advances. *J. Mater. Chem. C* **2023**, *11*, 5241–5256. [CrossRef]
23. Furuta, M.; Koretomo, D.; Magari, Y.; Aman, S.G.M.; Higashi, R.; Hamada, S. Heterojunction channel engineering to enhance performance and reliability of amorphous In–Ga–Zn–O thin-film transistors. *Jpn. J. Appl. Phys.* **2019**, *58*, 090604. [CrossRef]
24. Liang, K.; Wang, Y.; Shao, S.; Luo, M.; Pecunia, V.; Shao, L.; Zhao, J.; Chen, Z.; Mo, L.; Cui, Z. High-performance metal-oxide thin-film transistors based on inkjet-printed self-confined bilayer heterojunction channels. *J. Mater. Chem. C* **2019**, *7*, 6169–6177. [CrossRef]
25. Khim, D.; Lin, Y.H.; Nam, S.; Faber, H.; Tetzner, K.; Li, R.; Zhang, Q.; Li, J.; Zhang, X.; Anthopoulos, T.D. Modulation-doped In_2O_3/ZnO heterojunction transistors processed from solution. *Adv. Mater.* **2017**, *29*, 1605837. [CrossRef] [PubMed]
26. AlGhamdi, W.S.; Fakieh, A.; Faber, H.; Lin, Y.H.; Lin, W.Z.; Lu, P.Y.; Liu, C.H.; Salama, K.N.; Anthopoulos, T.D. Impact of layer thickness on the operating characteristics of In_2O_3/ZnO heterojunction thin-film transistors. *Appl. Phys. Lett.* **2022**, *121*, 233503. [CrossRef]
27. Li, Q.; Dong, J.; Han, D.; Wang, Y. Effects of channel thickness on electrical performance and stability of high-performance InSnO Thin-Film Transistors. *Membranes* **2021**, *11*, 929. [CrossRef] [PubMed]
28. Koretomo, D.; Hashimoto, Y.; Hamada, S.; Miyanaga, M.; Furuta, M. Influence of a SiO_2 passivation on electrical properties and reliability of In–W–Zn–O thin-film transistor. *Jpn. J. Appl. Phys.* **2019**, *58*, 018003. [CrossRef]
29. Minutolo, P.; Gambi, G.; D'Alessio, A. The optical band gap model in the interpretation of the UV-visible absorption spectra of rich premixed flames. *Symp. (Int.) Combust.* **1996**, *26*, 951–957. [CrossRef]
30. Zhou, X.; Han, D.; Dong, J.; Li, H.; Yi, Z.; Zhang, X.; Wang, Y. The effects of post annealing process on the electrical performance and stability of Al-Zn-O thin-film transistors. *IEEE Electron Device Lett.* **2020**, *41*, 569–572. [CrossRef]
31. Yang, H.; Zhou, X.; Lu, L.; Zhang, S. Investigation to the carrier transport properties in heterojunction-channel amorphous oxides thin-film transistors using dual-gate bias. *IEEE Electron Device Lett.* **2022**, *44*, 68–71. [CrossRef]
32. Rhee, J.; Choi, S.; Kang, H.; Kim, J.Y.; Ko, D.; Ahn, G.; Jung, H.; Choi, S.J.; Myong Kim, D.M.; Kim, D.H. The electron trap parameter extraction-based investigation of the relationship between charge trapping and activation energy in IGZO TFTs under positive bias temperature stress. *Solid State Electron.* **2018**, *140*, 90–95. [CrossRef]
33. Kim, M.H.; Park, J.W.; Lim, J.H.; Choi, D.K. The effect of hydrogen on the device stability of amorphous. InGaZnO Thin-Film Transistors under Positive Bias with Various Temperature Stresses. *Phys. Status Solidi (a)* **2019**, *216*, 1900297. [CrossRef]
34. Chong, E.; Chun, Y.S.; Lee, S.Y. Effect of trap density on the stability of SiInZnO thin-film transistor under temperature and bias-induced stress. *Electrochem. Solid-State Lett.* **2011**, *14*, H96. [CrossRef]
35. Bediako, D.K.; Rezaee, M.; Yoo, H.; Larson, D.T.; Zhao, S.Y.F.; Taniguchi, T.; Watanabe, K.; Brower-Thomas, T.L.; Kaxiras, E.; Kim, P. Heterointerface effects in the electrointercalation of van der Waals heterostructures. *Nature* **2018**, *558*, 425–429. [CrossRef] [PubMed]
36. Ji, X.; Yuan, Y.; Yin, X.; Yan, S.; Xin, Q.; Song, A. High-performance thin-film transistors with sputtered IGZO/Ga_2O_3 Heterojunction. *IEEE Trans. Electron Devices* **2022**, *69*, 6783–6788. [CrossRef]

37. Kim, H.; Gilmore, C.M.; Piqué, A.; Horwitz, J.S.; Mattoussi, H.; Murata, H.; Kafafi, Z.H.; Chrisey, D.B. Electrical, optical, and structural properties of indium-tin-oxide thin films for organic light-emitting devices. *J. Appl. Phys.* **1999**, *86*, 6451–6461. [CrossRef]
38. Tauc, J.; Grigorovici, R.; Vancu, A. Optical properties and electronic structure of amorphous germanium. *Phys. Status Solidi (b)* **1966**, *15*, 627–637. [CrossRef]
39. Lee, M.; Jo, J.W.; Kim, Y.J.; Choi, S.; Kwon, S.M.; Jeon, S.P.; Facchetti, A.; Kim, Y.H.; Park, S.K. Corrugated heterojunction metal-oxide thin-film transistors with high electron mobility via vertical interface manipulation. *Adv. Mater.* **2018**, *30*, e1804120. [CrossRef] [PubMed]
40. Khim, D.; Lin, Y.H.; Anthopoulos, T.D. Impact of layer configuration and doping on electron transport and bias stability in heterojunction and superlattice metal oxide transistors. *Adv. Funct. Mater.* **2019**, *29*, 1902591. [CrossRef]
41. Li, Z.; Hao, Y.; Zhang, C.; Xu, Y.; Zhang, J.; Cheng, Y.; Chen, D.; Feng, Q.; Xu, S.; Zhang, Y.; et al. Flexible solar-blind Ga_2O_3 ultraviolet photodetectors with high responsivity and photo-to-dark current ratio. *IEEE Photonics J.* **2019**, *11*, 6803709. [CrossRef]
42. Faber, H.; Das, S.; Lin, Y.H.; Pliatsikas, N.; Zhao, K.; Kehagias, T.; Dimitrakopulos, G.; Amassian, A.; Patsalas, P.A.; Anthopoulos, T.D. Heterojunction oxide thin-film transistors with unprecedented electron mobility grown from solution. *Sci. Adv.* **2017**, *3*, e1602640. [CrossRef] [PubMed]
43. Lin, Y.H.; Faber, H.; Labram, J.G.; Stratakis, E.; Sygellou, L.; Kymakis, E.; Hastas, N.A.; Li, R.; Zhao, K.; Amassian, A.; et al. High Electron mobility thin-film transistors based on solution-processed semiconducting metal oxide heterojunctions and quasi-superlattices. *Adv. Sci.* **2015**, *2*, 1500058. [CrossRef] [PubMed]
44. Wang, B.S.; Li, Y.S.; Cheng, I.C. Mobility enhancement in RF-sputtered MgZnO/ZnO heterostructure thin-film transistors. *IEEE Trans. Electron Devices* **2016**, *63*, 1545–1549. [CrossRef]
45. Kwon, S.; Bang, S.; Lee, S.; Jeon, S.; Jeong, W.; Kim, H.; Gong, S.C.; Chang, H.J.; Park, H.H.; Jeon, H. Characteristics of the ZnO thin film transistor by atomic layer deposition at various temperatures. *Semicond. Sci. Technol.* **2009**, *24*, 035015. [CrossRef]
46. Conley, J.F. Instabilities in amorphous oxide semiconductor thin-film transistors. *IEEE Trans. Device Mater. Reliab.* **2010**, *10*, 460–475. [CrossRef]
47. Cho, I.T.; Lee, J.M.; Lee, J.H.; Kwon, H.I. Charge trapping and detrapping characteristics in amorphous. InGaZnO TFTs under static and dynamic stresses. *Semicond. Sci. Technol.* **2008**, *24*, 015013. [CrossRef]
48. Powell, M.J. The physics of amorphous-silicon thin-film transistors. *IEEE Trans. Electron Devices* **1989**, *36*, 2753–2763. [CrossRef]
49. Park, J.; Rim, Y.S.; Li, C.; Wu, J.; Goorsky, M.; Streit, D. Defect-induced instability mechanisms of sputtered amorphous indium tin zinc oxide thin-film transistors. *J. Appl. Phys.* **2018**, *123*, 161568. [CrossRef]
50. Jeong, J.K. Photo-bias instability of metal oxide thin film transistors for advanced active matrix displays. *J. Mater. Res.* **2013**, *28*, 2071–2084. [CrossRef]
51. Kim, Y.; Kim, S.; Kim, W.; Bae, M.; Jeong, H.K.; Kong, D.; Choi, S.; Kim, D.M.; Kim, D.H. Amorphous InGaZnO Thin-Film Transistors—Part II: Modeling and Simulation of Negative Bias Illumination Stress-Induced Instability. *IEEE Trans. Electron Devices* **2012**, *59*, 2699–2706. [CrossRef]
52. Chen, X.; Wan, J.; Wu, H.; Liu, C. ZnO bilayer thin film transistors using H_2O and O_3 as oxidants by atomic layer deposition. *Acta Mater.* **2020**, *185*, 204–210. [CrossRef]
53. Park, B.; Nam, S.; Kang, Y.; Jeon, S.P.; Jo, J.W.; Park, S.K.; Kim, Y.H. Cation doping strategy for improved carrier mobility and stability in metal-oxide Heterojunction thin-film transistors. *Mater. Today Electron.* **2024**, *8*, 100090. [CrossRef]
54. Seul, H.J.; Cho, J.H.; Hur, J.S.; Cho, M.H.; Cho, M.H.; Ryu, M.T.; Jeong, J.K. Improvement in carrier mobility through band-gap engineering in atomic-layer-deposited In-Ga-Zn-O stacks. *J. Alloys Compd.* **2022**, *903*, 163876. [CrossRef]
55. Yao, J.; Xu, N.; Deng, S.; Chen, J.; She, J.; Shieh, H.D.; Liu, P.T.; Huang, Y.P. Electrical and photosensitive characteristics of a-IGZO TFTs related to oxygen vacancy. *IEEE Trans. Electron Devices* **2011**, *58*, 1121–1126. [CrossRef]
56. Bukke, R.N.; Avis, C.; Jang, J. Solution-processed amorphous In–Zn–Sn oxide thin-film transistor performance improvement by solution-processed Y_2O_3 passivation. *IEEE Electron Device Lett.* **2016**, *37*, 433–436. [CrossRef]
57. Mude, N.N.; Bukke, R.N.; Saha, J.K.; Avis, C.; Jang, J. Highly stable, solution-processed Ga-doped IZTO thin film transistor by Ar/O_2 plasma treatment. *Adv. Electron. Mater.* **2019**, *5*, 1900768. [CrossRef]
58. Li, L.; Xu, Y.; Wang, Q.; Nakamura, R.; Jiang, Y.; Ao, J.P. Metal-oxide-semiconductor AlGaN/GaN heterostructure field-effect transistors using TiN/AlO stack gate layer deposited by reactive sputtering. *Semicond. Sci. Technol.* **2015**, *30*, 015019. [CrossRef]
59. Han, C.H.; Kim, S.S.; Kim, K.R.; Baek, D.H.; Kim, S.S.; Choi, B.D. Effects of electron trapping and interface state generation on bias stress induced in indium–gallium–zinc oxide thin-film transistors. *Jpn. J. Appl. Phys.* **2014**, *53*, 08NG04. [CrossRef]
60. Zafar, S.; Callegari, A.; Gusev, E.; Fischetti, M.V. Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks. *J. Appl. Phys.* **2003**, *93*, 9298–9303. [CrossRef]
61. Suresh, A.; Muth, J.F. Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors. *Appl. Phys. Lett.* **2008**, *92*, 033502. [CrossRef]
62. Qiang, L.; Liang, X.; Pei, Y.; Yao, R.; Wang, G. Extraction method of trap densities for indium zinc oxide thin-film transistors processed by solution method. *Thin Solid Films* **2018**, *649*, 51–56. [CrossRef]
63. Nomura, K.; Kamiya, T.; Hirano, M.; Hosono, H. Origins of threshold voltage shifts in room-temperature deposited and annealed a-In–Ga–Zn–O thin-film transistors. *Appl. Phys. Lett.* **2009**, *95*, 013502. [CrossRef]

64. Han, J.; Abliz, A.; Wan, D. Impact of hydrogen plasma treatment on the electrical performances of ZnO thin-film transistors. *Chin. J. Phys.* **2022**, *77*, 327–334. [CrossRef]
65. Zhang, L.; Li, J.; Zhang, X.W.; Yu, D.B.; Lin, H.P.; Jiang, X.Y.; Zhang, Z.L. The influence of the SiO_2 deposition condition on the ZnO thin-film transistor performance. *Superlattices Microstruct.* **2010**, *48*, 198–205. [CrossRef]
66. Abliz, A.; Huang, C.W.; Wang, J.; Xu, L.; Liao, L.; Xiao, X.; Wu, W.W.; Fan, Z.; Jiang, C.; Li, J.; et al. Rational design of ZnO: H/ZnO bilayer structure for high-performance thin-film transistors. *ACS Appl. Mater. Interfaces* **2016**, *8*, 7862–7868. [CrossRef] [PubMed]
67. Liu, P.T.; Chang, C.H.; Chang, C.J. Reliability enhancement of high-mobility amorphous indium-tungsten oxide thin film transistor. *ECS Trans.* **2015**, *67*, 9. [CrossRef]
68. Qu, M.; Chang, C.H.; Meng, T.; Zhang, Q.; Liu, P.T.; Shieh, H.P.D. Stability study of indium tungsten oxide thin-film transistors annealed under various ambient conditions. *Phys. Status Solidi (a)* **2017**, *214*, 1600465. [CrossRef]
69. Aikawa, S.; Darmawan, P.; Yanagisawa, K.; Nabatame, T.; Abe, Y.; Tsukagoshi, K. Thin-film transistors fabricated by low-temperature process based on Ga-and Zn-free amorphous oxide semiconductor. *Appl. Phys. Lett.* **2013**, *102*, 102101. [CrossRef]

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