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Thermally stable Bi_2Te_3/WSe_2 Van Der Waals contacts for pMOSFETs application

Wen Hsin Chang[1]✉, Shogo Hatayama[1], Yuta Saito[1,2,3]✉, Naoya Okada[1], Takahiko Endo[4], Yasumitsu Miyata[4] & Toshifumi Irisawa[1]

Novel van der Waals (vdW) contacts formed by layered Bi_2Te_3 are found effective in improving the performance of WSe_2 pMOSFETs. As compared with conventional transition metal-based Ni/Au S/D contacts, over 10^3 times on-state current improvement is achieved. vdW interface formation between Bi_2Te_3 and WSe_2 is confirmed by X-ray diffraction analysis and scanning transmission electron microscope observation. An atomically flat Bi_2Te_3/WSe_2 vdW interface, where the number of defects could be reduced as small as possible, contributes to the suppression of Fermi-level pinning caused by defect-induced gap states. Moreover, the semimetal-like characteristics of Bi_2Te_3 are also effective in minimizing the impact of metal-induced gap states. These features offer WSe_2 pMOSFETs with exceptional S/D junction characteristics, including suppressed off-state leakage and a higher on–off ratio. In addition, it is found that WSe_2 pMOSFETs with Bi_2Te_3 S/D contacts have excellent thermal stability, maintaining device performance even after 400 °C annealing, which is very promising for CMOS back-end-of-line application. The layered tellurides, reconciling low contact resistance and high thermal stability, are promising, particularly from the perspective of their application in the manufacturing process.

The device performance of transition metal dichalcogenide (TMDC) metal-oxide-semiconductor field-effect transistors (MOSFETs) has been constrained by a large contact resistance owing to severe Fermi level pinning (FLP) between metal electrodes and TMDCs[1–3]. The origins of FLP are usually attributed to the metal-induced gap states (MIGS) owing to metal wave function tailing into forbidden energy states[4] or disorder-induced gap states (DIGS) owing to interfacial disorders/defects at metal/semiconductor interface[5]. For the past few decades, several approaches have been studied on TMDC for both n and pMOSFETs to alleviate FLP. Semimetal bismuth (Bi) has been shown to reduce MIGS because of its small density of states (DOS) near the Fermi level, which is very promising to enhance the device performance of MoS_2 nMOSFETs[6]. However, the thermal stability of Bi is a major concern when considering its application to CMOS fabrication[7]. Besides semimetal material, van der Waals (vdW) contacts were also found effective in enhancing the device performance of MoS_2 nMOSFETs as well as WSe_2 pMOSFETs with metal contacts including In[8], Au[9], $SnSe_2$[10], NiSe[11], and a-GeTe[12]. In the meantime, the atomically flat vdW interface has a great potential to eliminate the interfacial disorders/defects between the contact material and TMDC, where the DIGS can also be suppressed. Nevertheless, the thermal stability of these kinds of contact materials are still unclear.

Recently, Sb_2Te_3, a famous and well-studied layered phase-change memory material[13,14], has been proven as a promising S/D contact material for MoS_2 nMOSFETs with low contact resistance[15]. Through appropriate post-metallization annealing (PMA), the well-aligned vdW Sb_2Te_3/MoS_2 interface can be achieved by the sputtering technique. Besides, Sb_2Te_3 is a degenerate narrow band gap (~ 0.3 eV) semiconductor with p-type conduction, where the Fermi level of Sb_2Te_3 usually resides around the valence band maximum[16–18]. This feature allows Sb_2Te_3 to possess a semimetal-like characteristics. Meanwhile, since the Fermi level of Sb_2Te_3 is aligned near the conduction band minimum of MoS_2, Sb_2Te_3 can reduce the contact resistance of MoS_2 nMOSFETs by a mechanism of suppressing the FLP and resultant small barrier height for electrons. However, for realizing TMDC CMOS logic devices, not only MoS_2 nMOSFETs but also pMOSFETs should be considered. WSe_2 is a well-known p-type TMDC material, showing high intrinsic hole mobility[19]. Although high-performance MoS_2

[1]Semiconductor Frontier Research Center, National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba Central 2, 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan. [2]Research Center for Green X-Tech, Tohoku University, 6-6-11, Aoba-Yama, Aoba-Ku, Sendai 980-8579, Japan. [3]Department of Materials Science, Graduate School of Engineering, Tohoku University, 6-6-11, Aoba-Yama, Aoba-Ku, Sendai 980-8579, Japan. [4]Department of Physics, Tokyo Metropolitan University, 1-1 Minami-Osawa, Hachioji, Tokyo 192-0397, Japan. ✉email: wh-chang@aist.go.jp; yuta.saito.e5@tohoku.ac.jp

nMOSFETs with high-quality CVD-grown MoS_2 channels have been generally demonstrated worldwide, the WSe_2 pMOSFETs with comparable performance to the MoS_2 nMOSFETs are still beset with difficulties[20–22], owing to unstable monolayer channel quality[23], ambipolar transport behavior[24] and large contact resistance[22].

Searching for a similar Te-based material but with high electron affinity/work function for WSe_2 pMOSFETs application, we found Bi_2Te_3 is a promising candidate. Bi_2Te_3 shows the similar crystal structure as Sb_2Te_3 with slightly different lattice constants. Nevertheless, Bi_2Te_3 exhibits a tendency to become a degenerate n-type semiconductor, where its Fermi-level locates near the conduction band minimum[25]. Figure 1 shows the comparison of band alignment of Sb_2Te_3 with MoS_2 and Bi_2Te_3 with WSe_2 as depicted using the theoretical/experimental band parameters[25–29]. As mentioned and already demonstrated, judging from the band alignment, Sb_2Te_3 is suitable for MoS_2 nMOSFETs, while Bi_2Te_3 has a potential being compatible for WSe_2 pMOSFETs.

In this work, monolayer (1L) WSe_2 pMOSFETs with Bi_2Te_3 S/D contacts were fabricated and subjected to PMA at different temperatures to verify the feasibility of Bi_2Te_3 as a contact material and to investigate its thermal stability. The Bi_2Te_3/WSe_2 can also form a well-aligned vdW interface under appropriate thermal treatment, just like that of Sb_2Te_3 on MoS_2. It is worth noting that significant device performance enhancement of the WSe_2 pMOSFET with Bi_2Te_3 S/D contacts was observed as compared with the controlled device using the Ni/Au contacts, indicating the possibility of contact resistance reduction at the Bi_2Te_3/WSe_2 interface. Most important of all, the S/D contact characteristics and device performance can maintain or even improve after 400 °C PMA, suggesting the high thermal stability of Bi_2Te_3 and the feasibility of applying it to CMOS fabrication.

Results and discussion

Figure 2a is the top view of optical microscope (OM) image of CVD-grown WSe_2 flakes, where the WSe_2 flakes consist of WSe_2 with different thickness including 1L, two-layer (2L) and bulk region with layer numbers over 10L. The comparison of Raman spectra of WSe_2 with different thicknesses is shown in Fig. 2b. It is found that the distribution of Raman peaks is very sensitive to WSe_2 thickness and can be used as a fingerprint for WSe_2 with different layer numbers. For WSe_2 with multi-layers over 10L, obvious E^1_{2g} (248. 1 cm^{-1}) mode and A_{1g} mode (251.8 cm^{-1}) peaks were observed, which agrees with the spectra extracted from a WSe_2 bulk crystal[30]. On the other hand, for few-layer WSe_2, the E^1_{2g} mode and A_{1g} mode merged or degenerated into a single peak and 2LA(M) mode near 261.2 cm^{-1} resulting from the second-order Raman mode owing to two-phonon scattering at the M point of the Brillouin zone[31,32] appeared. Besides, as compared with multi-layer WSe_2 (the inset of Fig. 2b), the absence of B^1_{2g} peak at around 308.5 cm^{-1} is a signature to confirm the monolayer thickness of the WSe_2 channel[30,33].

The WSe_2 samples used for X-ray diffraction (XRD) analysis can be separated into two kinds. One mainly consists of 1L WSe_2 with small portion (< 10%) of multi-layer WSe_2, which will be referred to as 1L WSe_2 afterward. The other mainly consists of multi-layer WSe_2 with layer numbers over 10L, which will be referred to as > 10L WSe_2 afterward. Figure 3a,b shows the XRD $\theta/2\theta$ scan of $W/Bi_2Te_3/WSe_2/SiO_2/Si$ stacked films before and after PMA at temperatures from 200 to 450 °C extracted from 1L WSe_2 and > 10L WSe_2 samples. For the as-deposited sample, a small peak of Bi_2Te_3 015 can be found at around $2\theta = 28°$. This is the strongest peak observed for the powder sample[34], indicating the as-deposited Bi_2Te_3 film consists of randomly oriented

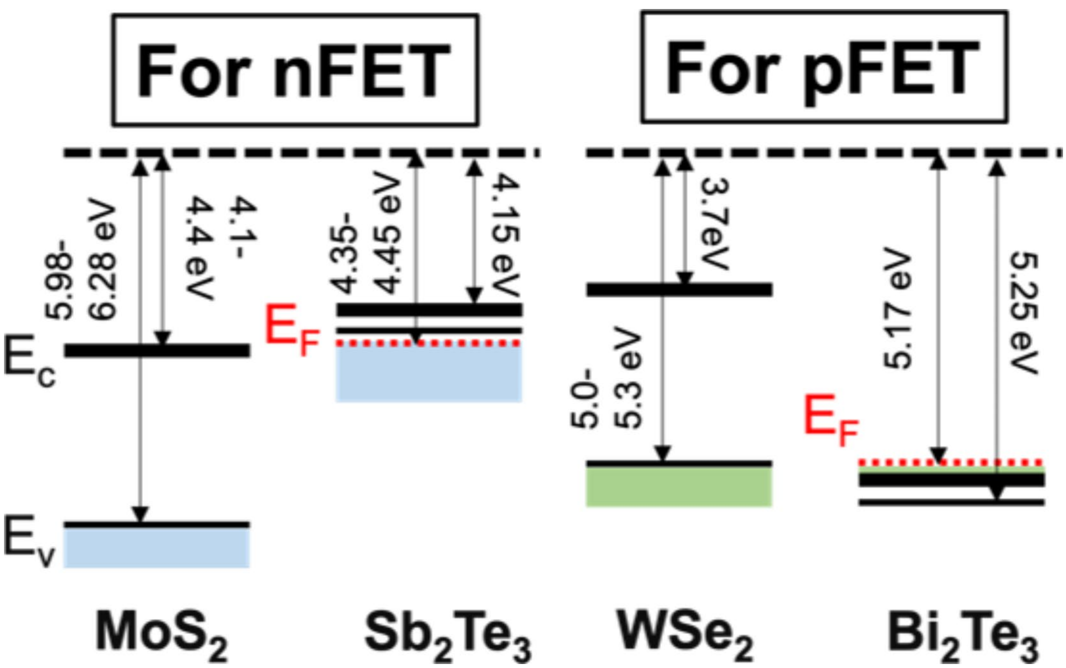

Fig. 1. The band alignment of Sb_2Te_3/MoS_2 and Bi_2Te_3/WSe_2, indicating the Te-based contacts are suitable for fabricating MoS_2 nMOSFETs and WSe_2 pMOSFETs. The figure is remodified from Fig. 5a in Ref. 15.

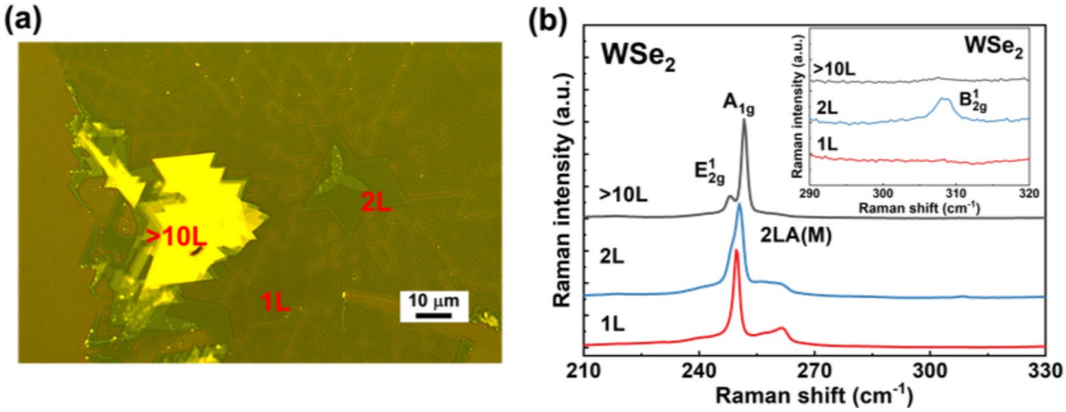

Fig. 2. (**a**) The optical microscope (OM) image of the top view of CVD-grown WSe_2 with different thicknesses. The scale bar is 10 µm. (**b**) The comparison of Raman spectra of WSe_2 with different thicknesses. The fingerprint of Raman peaks is very sensitive to WSe_2 thickness. The inset shows WSe_2 Raman spectra focusing on Raman shift from 290 to 320 cm^{-1}.

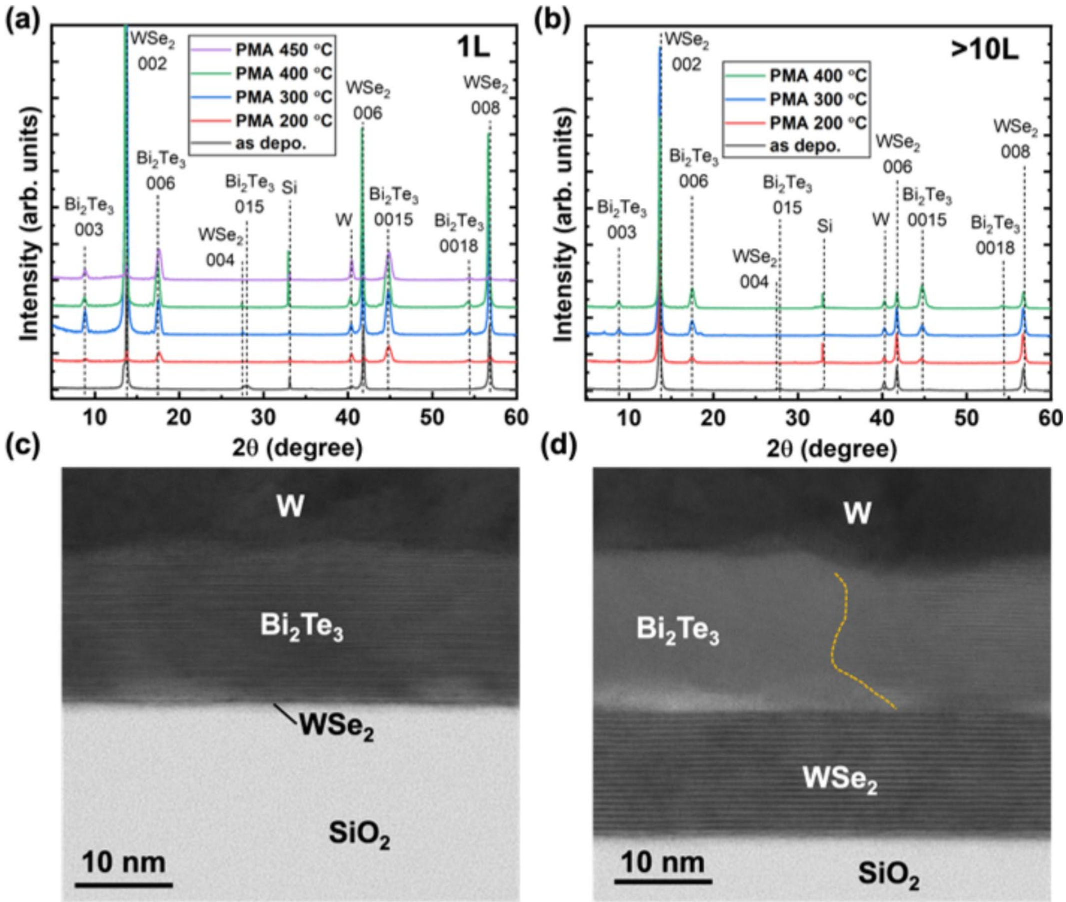

Fig. 3. XRD *θ/2θ* scan of $W/Bi_2Te_3/WSe_2/SiO_2/Si$ stacked films before and after PMA from 200 to 450 °C extracted from (**a**) 1L WSe_2 and (**b**) > 10L WSe_2. The high-resolution scanning transmission electron microscope (STEM) cross-sectional images of 400 °C annealed W/Bi_2Te_3 stacked film as deposited on (**c**) 1L WSe_2 and (**d**) > 10L WSe_2. The yellow dashed line indicates the boundary between polycrystalline Bi_2Te_3 with tiny grain size and layered Bi_2Te_3.

polycrystalline with tiny grain size. The Bragg reflections of the crystalline Bi_2Te_3 (*001*) plane emerged after 200 °C PMA and became much stronger after 400 °C PMA, indicating that the Bi_2Te_3 crystal grains changed the orientation from random to *c*-axis oriented through thermal treatment. Note that highly *c*-axis oriented Bi_2Te_3 and WSe_2 peaks were still present even after 400 °C PMA, suggesting that the layer structure of Bi_2Te_3 film and the well-aligned Bi_2Te_3/WSe_2 interface preserved. This behavior of thermal-induced crystallization of Bi_2Te_3 on WSe_2 is very similar to that of Sb_2Te_3/MoS_2 case[15]. However, further annealing at 450 °C resulted in a decrease of the peak intensity for both Bi_2Te_3 and WSe_2 peaks, indicating the degradation of the interfacial quality of the heterostructure. From a materials point of view, the Bi_2Te_3/WSe_2 heterostructure can sustain at least 400 °C annealing, which meets the thermal budget requirement of back-end-of-line (BEOL) for CMOS fabrication. Moreover, the peak intensity of Bi_2Te_3 006 and 0015 peaks is much stronger for Bi_2Te_3 on 1L WSe_2 (Fig. 3a) as compared with those on > 10L WSe_2 (Fig. 3b), suggesting Bi_2Te_3 has better crystallinity on 1L WSe_2. This phenomenon was also confirmed in the STEM cross-sectional images as shown in Fig. 3c,d for W/Bi_2Te_3 stacked film deposited on 1L WSe_2 and > 10L WSe_2 after 400 °C annealing. For W/Bi_2Te_3 on 1L WSe_2 (Fig. 3c), a well-aligned layered structure of Bi_2Te_3 is clearly observed without any in-plane grain boundaries and distinct defects at this scale. Conversely, a clear grain boundary (yellow dashed line) was observed for those on > 10L WSe_2 (Fig. 3d). It is found that SeO_x on the surface of > 10L WSe_2 hinders the atomic alignment between Bi_2Te_3 and WSe_2. Moreover, some grains do not show *c*-axis orientation as indicated by absence of lattice fringes parallel to the substrate surface. Since selenium (Se) has very low chemical reactivity and the selenization of WO_3 only happens at certain growth condition, the Se may tend to pile up on > 10L WSe_2 during CVD growth owing to incomplete reaction[35]. The Se residues will then lead to SeO_x formation after air exposure.

A detailed energy dispersive X-ray (EDX) mapping analysis of the Fig. 3d is presented. (see Supplementary Fig. S1). In addition, surface roughness for thick WSe_2 film may affect the growth behavior of Bi_2Te_3 film. This evidence indicates that the surface cleanness as well as flatness of WSe_2 are key factors for transferring poly crystalline Bi_2Te_3 into a highly oriented structure during thermal treatment.

Figure 4a shows the smallest repeating cell of the Bi_2Te_3/WSe_2 vdW interface viewed from the [001] (*c*-axis) direction based on the lattice information, where Bi_2Te_3 possesses lattice constants of $a = b = 4.388$ Å and $c = 30.46$ Å[36], and those of WSe_2 are $a = b = 3.288$ Å and $c = 12.989$ Å[37]. Note that since both materials adopt hexagonal symmetry, the deposited Bi_2Te_3 could follow the atomic alignment of underlayer WSe_2, where the atomic positions of terminated Te and Se nearly match every three and four unit cells, respectively, along the in-plane direction. Moreover, thanks to the layered nature of Bi_2Te_3, the large in-plane lattice mismatch does not influence the growth on WSe_2, which is known as the vdW epitaxy[38]. Figure 4b shows the High-Angle Annular Dark Field (HAADF)-STEM images focusing on the interface between Bi_2Te_3 and WSe_2, where Bi_2Te_3 is also fabricated by sputtering as mentioned in Fig. 3, and Fig. 4c–f correspond to the EDX mapping analysis of W, Se, Bi, and Te. The heterostructure is subjected to a 400 °C annealing process. Note that as can be seen in Fig. 4c, the elemental mapping of W exhibits two lateral lines, indicating the observed area contains bilayer WSe_2.

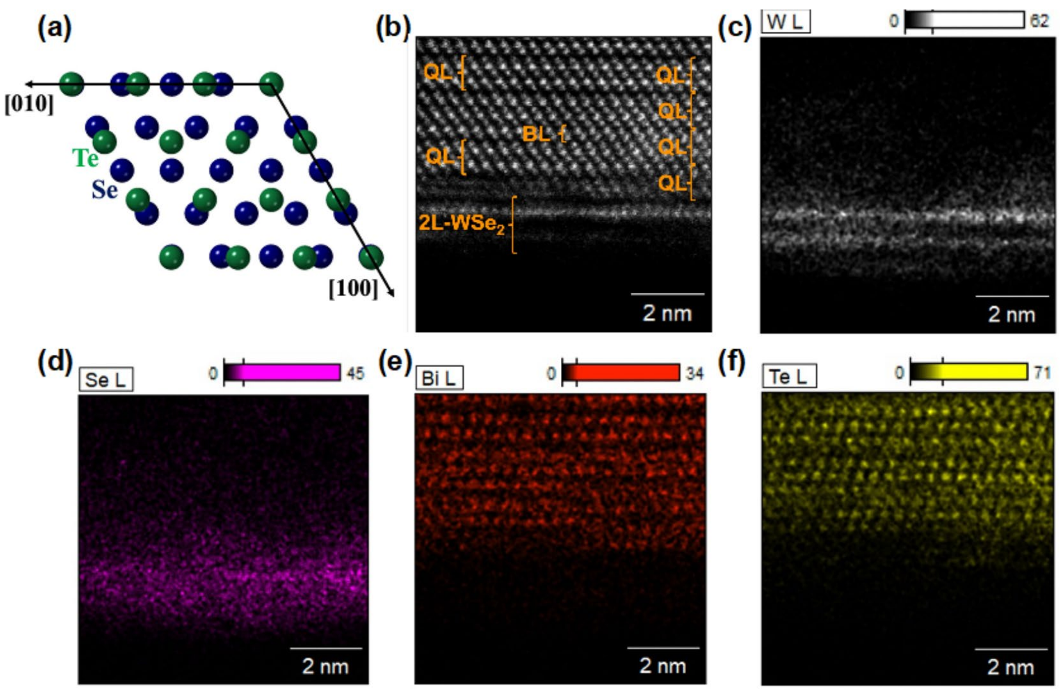

Fig. 4. (**a**) A top-view illustration of the smallest repeating cell of the Bi_2Te_3/WSe_2 vdW interface. To prevent complexity, only Te and Se atoms adjacent to a vdW gap are shown. (**b**) The enlarged HAADF-STEM images of the Bi_2Te_3/WSe_2 interface, indicating the formation of the vdW interface. The EDX mapping of (**c**) W, (**d**) Se, (**e**) Bi, and (**f**) Te at the Bi_2Te_3/WSe_2 interface, suggesting no chemical interaction occurs.

Nevertheless, the discussion regarding the interfacial stability is still valid for Bi_2Te_3/2L-WSe_2 heterostructure. A vdW interface composed of Bi_2Te_3 quintuple layer (QL) (Te-Bi-Te-Bi-Te stacking) and WSe_2 monolayer (Se-W-Se stacking) is clearly visible. It was found that the Bi_2Te_3 layer contains not only QLs but the bilayer (BL) can be also seen (Fig. 4b).

The same BL stacking fault, known as bilayer swapping, was reported for Sb_2Te_3, but the electrical properties such as carrier concentration are not largely influenced by the presence of BL[39,40]. According to the EDX mapping, neither interfacial mixing nor interdiffusion is observed at the Bi_2Te_3/WSe_2 interface, indicating that the vdW interface can be maintained even after 400 °C annealing. We believe that the almost defect-free and highly stable vdW interface could provide the Fermi-level unpinning at the Bi_2Te_3/WSe_2 interface, which helps to enhance the device performance of the WSe_2 device.

Figure 5 shows the typical height and average work function (WF) profile of the Bi_2Te_3/WSe_2 and Ni/WSe_2 interface extracted by Kelvin Probe Force Microscopy (KPFM), respectively. Since the electrodes on WSe_2 were fabricated through lift-off process, the abrupt edge between electrodes and WSe_2 is hard to obtain owing to the photoresist residue. We define the averaged CPD of WSe_2 away from the interface about 1 µm. The averaged WF value of WSe_2 of 5.37 eV was derived through the CPD difference from Au (5.47 eV)[41] reference pad on WSe_2. The corresponding optical images and KPFM CPD images are also presented (see Supplementary Fig. S2). The WF of Bi_2Te_3 and Ni were then determined to be 5.21 and 5.02 eV, respectively. The obtained WF value of WSe_2 and Bi_2Te_3 are all very close to the theoretical value as depicted in Fig. 1. Moreover, a lower Fermi-level difference is expected for Bi_2Te_3/WSe_2 than that of Ni on WSe_2. If the Fermi-level is unpinned, Bi_2Te_3 has a great potential to achieve better p-type transport properties on WSe_2.

To investigate the electrical properties of Bi_2Te_3 on WSe_2 as a contact material, we fabricated the back gate 1L WSe_2 pMOSFETs with Bi_2Te_3 contact. Figure 6a is the detailed process flow and a schematic cross-sectional figure of a 1L WSe_2 pMOSFET with Bi_2Te_3 S/D contacts. Figure 6b shows the Raman spectrum obtained from the channel region between the S/D metal pads of WSe_2 pMOSFET, as shown in the inset, where the electrode gap size is around 5 µm. The peak position shift between E^1_{2g} mode and A_{1g} mode and the absence of B^1_{2g} peak is in good agreement with 1L WSe_2, as mentioned in Fig. 2.

Figure 7a compares the I_D–V_G transfer curves extracted from the 1L WSe_2 pMOSFETs with Bi_2Te_3 and Ni/Au S/D contacts. For a fair comparison, all the devices were subjected to PMA at 200 °C for 10 min. The 5-µm-gate-length WSe_2 pMOSFETs with Bi_2Te_3/W contacts exhibited significant device performance enhancement as compared with those of Ni/Au control devices. A high on–off ratio of ~10^6 was obtained at a V_D of -50 mV. Moreover, the on-state current (I_{on}) of the devices with Bi_2Te_3/W contacts considerably increases to approximately 10^3 times greater than that of the MOSFETs using Ni/Au for S/D contacts. These results suggest a significant contact resistance reduction by employing Bi_2Te_3 contacts, which can be attributed

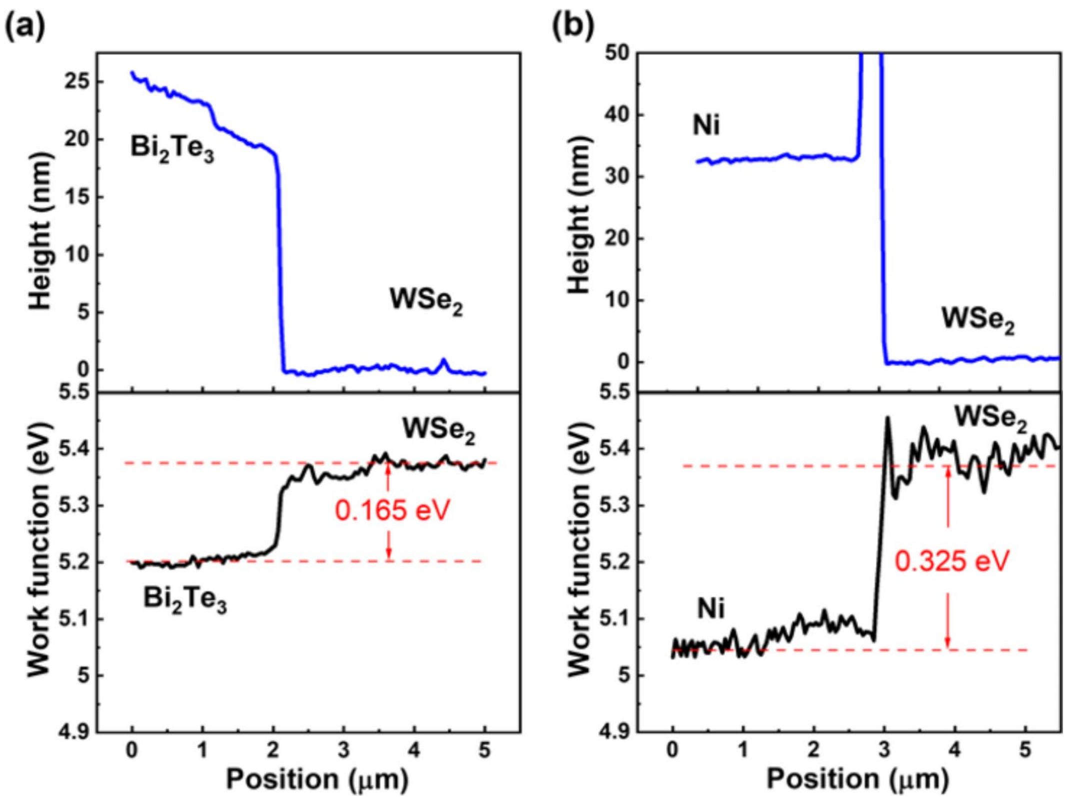

Fig. 5. Height profile and corresponding averaged work function profile of the (**a**) Bi_2Te_3/WSe_2 and (**b**) Ni/WSe_2 interface.

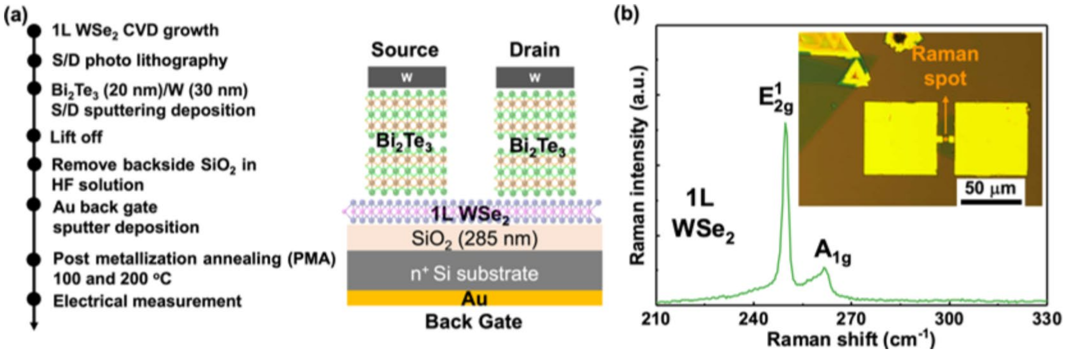

Fig. 6. (**a**) The detailed process flow and a schematic cross-sectional figure of a 1L WSe_2 pMOSFET with Bi_2Te_3 contacts and Au back-gate. (**b**) 1L WSe_2 Raman spectrum obtained from the channel region between the S/D metal pads. The inset shows the OM image of a top view of the back-gate 1L WSe_2 pMOSFET.

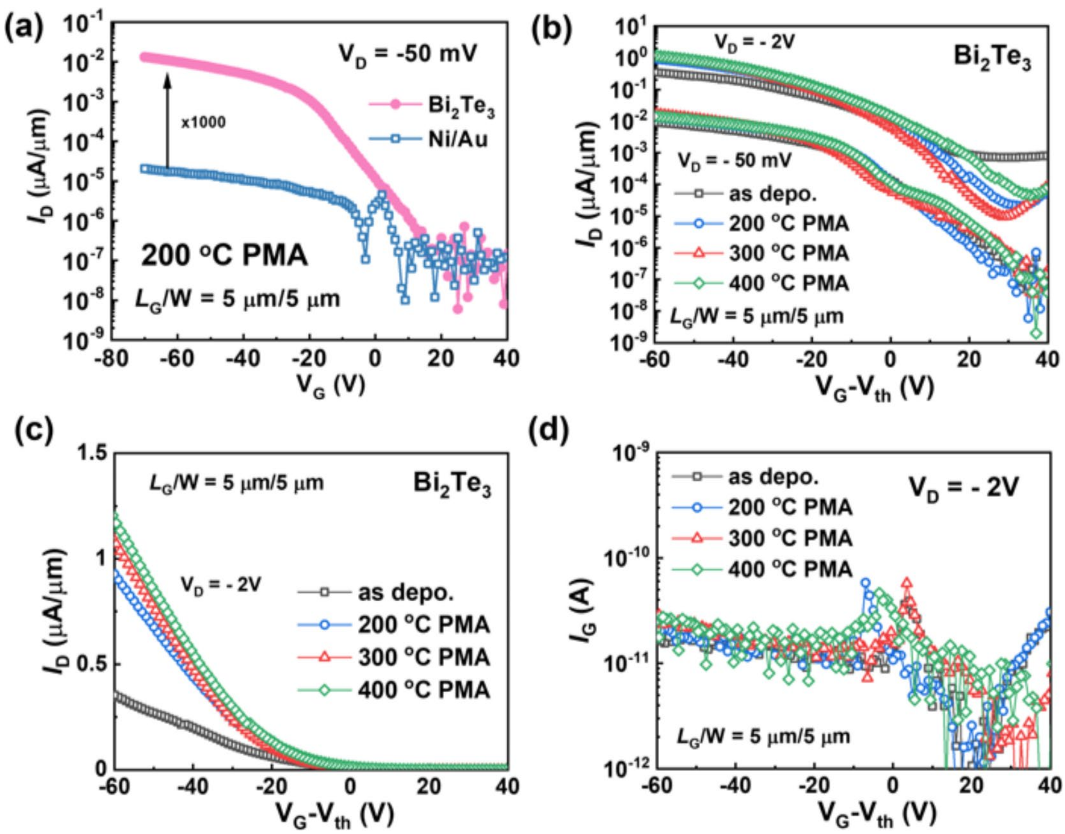

Fig. 7. (**a**) Comparison of I_D-V_G transfer curves of devices with Bi_2Te_3/W and Ni/Au S/D contacts on 285-nm-thick SiO_2 dielectrics. (**b**) Comparison of I_D-V_G transfer curves of devices with Bi_2Te_3/W contacts before and after the PMA process at different temperatures. (**c**) The linear scale of I_D-V_G transfer curves shown in Fig. 6b. (**d**) The comparison of I_G of devices with Bi_2Te_3/W contacts before and after the PMA process at different temperatures.

to the low Fermi-level difference between Bi_2Te_3 and WSe_2 (Fig. 5). Due to the semi-metallic characteristics of Bi_2Te_3 for suppressing MIGS and vdW interface for suppressing DIGS, the Fermi-level between Bi_2Te_3 and WSe_2 tends to unpin, so the small Fermi-level difference can be maintained and leads to better device performance. Besides Ni/Au S/D contacts, we also compare Bi_2Te_3 contacts with Cr/Au contact (see Supplementary Fig. S3). Significant device performance enhancement was also observed, suggesting the effectiveness of Bi_2Te_3 contacts for improving junction characteristics on WSe_2. The thermal stability of 1L WSe_2 pMOSFETs was also investigated. Figure 7b shows the comparison of I_D-V_G transfer curves at V_D of -50 mV and -2 V for 1L WSe_2 pMOSFETs with Bi_2Te_3/W contacts before and after the PMA process at different temperatures. Reduced off-state leakage (I_{off}) and enlarged on–off ratio with increasing PMA temperature are visible, indicating the S/D junction characteristics improvement through thermal treatment. At V_D of − 2 V, increasing I_{on} is observed with increasing PMA temperature, which is more obvious in the linear scale as shown in Fig. 7c. This indicates the contact resistance reduction and the high thermal stability of Bi_2Te_3/WSe_2 contacts. Approximately 3 times I_{on} enhancement was achieved after 400 °C PMA as compared with its as-deposited counterpart, suggesting the benefits of vdW interface formation for reducing contact resistance. The I_{on} enhancement mainly resulted from the contact resistance reduction instead of gate leakage current (I_G), as I_G remains considerably low during the thermal treatment, as shown in the Fig. 7d.

Nevertheless, kinks at the subthreshold region were visible after thermal treatment and got worse at 400 °C. Since the WSe_2 of our devices is not covered by any protection layer, this phenomenon may be attributed to the interfacial degradation between WSe_2 and backside SiO_2 and the damage of WSe_2 itself.

Conclusion

Thermally stable Bi_2Te_3/WSe_2 vdW contact up to 400 °C was fabricated, and significant device performance improvement was realized owing to the atomic-level defect-free vdW interface. The Bi_2Te_3/WSe_2 heterostructure can go through and maintain its quality at least after 400 °C annealing, which fulfills the requirement for the BEOL CMOS process. Moreover, significant enhancement of device performance in terms of up to 10^3 times current improvement was demonstrated using Bi_2Te_3/WSe_2 contacts as compared with conventional transition metal contacts. This also indicates significant contact resistance reduction. All evidence shown in this work supports that layered tellurides can be applied to not only MoS_2 nMOSFETs but also WSe_2 pMOSFETs as S/D contacts, which is very promising for TMDC CMOS applications.

Methods

Synthesis of WSe_2

By using chemical vapor deposition (CVD), WSe_2 flakes were deposited on SiO_2 (285 nm)/Si substrates at 880 °C with WO_3 powder, Se beads, and KBr powder[42,43]. KBr powder was used as the growth promoter[44].

Bi_2Te_3 deposition by sputtering

To investigate the crystal quality of Bi_2Te_3 on WSe_2 and its applicability to contact material, 20-nm-thick Bi_2Te_3 and 30-nm-thick tungsten (W) films were deposited onto the WSe_2 by magnetron sputtering at room temperature (300 K) (QAM-4, ULVAC KYUSYU Corp.)[14,45]. W was treated as a protection layer for Bi_2Te_3 during the thermal treatment.

Material characterization

Raman analysis was used to determine the thickness of the WSe_2 layer. The Raman spectra were extracted from the HORIBA LabRAM Raman spectrometer with 488 nm wavelength laser excitation using a power of 5 mW. X-ray diffraction (XRD) and scanning transmission electron microscope (STEM) were used to investigate the crystallinity of Bi_2Te_3 and the Bi_2Te_3/WSe_2 interface. For XRD analysis, Cu-Ka (l = 1.542 Å) was used in a Bragg–Brentano geometry (Ultima IV, Rigaku Corp.). A focused ion beam (FIB) technique was used to prepare the STEM sample, and JEM-ARM200F (JEOL, Ltd.) was used to study the cross-sectional images of Bi_2Te_3 and WSe_2 and energy dispersive X-ray (EDX) mapping with an accelerating voltage of 200 kV was performed. Kelvin probe force microscopy (KPFM) was used to measure the contact potential difference (CPD), which can be used to extract the work function difference between metal electrodes and WSe_2. A standard atomic force microscope (Park Systems NX10) was utilized with a conductive cantilever (Olympus AC240TM, Pt coat) for CPD measurement under ambient condition.

Fabrication of back gate 1L WSe_2 MOSFETs

After WSe_2 growth, photolithography was used for defining S/D regions. 20-nm-thick Bi_2Te_3 and 30-nm-thick W films were then deposited onto the WSe_2 layer by magnetron sputtering. The S/D contacts were then fabricated through a lift-off process using acetone and isopropanol (IPA) at 25 °C. Subsequently, the backside SiO_2 of the samples was removed using hydrogen fluoride (HF) solution, followed by back-gate Au deposition using sputtering. Post metallization annealing (PMA) was performed in Ar ambient for 10 min at 200, 300 and 400 °C. The back-gate devices with Ni (50 nm)/Au (50 nm) S/D metal contacts were also fabricated for comparison. Ni and Au were deposited by e-beam evaporator, respectively. To eliminate the impact from WSe_2 quality and WSe_2/SiO_2 interfacial condition on device performance, we fabricated the devices with different S/D metal contacts on the same WSe_2 sample grown by CVD.

Electrical characterization

All electrical characterization of WSe_2 MOSFETs was performed in a standard probe station under atmospheric condition at room temperature, and Keysight B1500A was used for electrical measurements.

Data availability

The datasets used and/or analyzed during the current study available from the corresponing author on reasonable request.

Received: 6 September 2024; Accepted: 12 November 2024
Published online: 19 November 2024

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Acknowledgements
This work is supported by JST-MIRAI (JPMJMI22708192), JST FOREST Program (JPMJFR213X), JST-CREST (JPMJCR23A4), NICT (05901), and Kakenhi Grants-in-Aid (JP21H05232, JP21H05234, JP22H04957) from the Japan Society for the Promotion of Science (JSPS).

Author contributions
T. I. supervised the overall project. T. I., W. H. C., and N. O. planned and conceived the research and experiment. S. H. and Y. S. contributed to the Bi_2Te_3 deposition and XRD analysis. T. E. and Y. M. contributed to the WSe_2 CVD growth. W. H. C. contributed to the device fabrication, electrical properties measurement, KPFM measurement and data analysis. The manuscript was written by W. H. C., S. H., Y. S., and T. I. with discussion and inputs from all authors.

Competing interests
The authors declare no competing interests.

Additional information
Supplementary Information The online version contains supplementary material available at https://doi.org/10.1038/s41598-024-79750-z.

Correspondence and requests for materials should be addressed to W.H.C. or Y.S.