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High-Performance Memristive Synapse Based on Space-Charge-Limited Conduction in $LiNbO_3$

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Abstract: Advancing neuromorphic computing technology requires the development of versatile synaptic devices. In this study, we fabricated a high-performance Al/$LiNbO_3$/Pt memristive synapse and emulated various synaptic functions using its primary key operating mechanism, known as oxygen vacancy-mediated valence charge migration (V_O-VCM). The voltage-controlled V_O-VCM induced space-charge-limited conduction and self-rectifying asymmetric hysteresis behaviors. Moreover, the device exhibited voltage pulse-tunable multi-state memory characteristics because the degree of V_O-VCM was dependent on the applied pulse parameters (e.g., polarity, amplitude, width, and interval). As a result, synaptic functions such as short-term memory, dynamic range-tunable long-term memory, and spike time-dependent synaptic plasticity were successfully demonstrated by modulating those pulse parameters. Additionally, simulation studies on hand-written image pattern recognition confirmed that the present device performed with high accuracy, reaching up to 95.2%. The findings suggest that the V_O-VCM-based Al/$LiNbO_3$/Pt memristive synapse holds significant promise as a brain-inspired neuromorphic device.

Keywords: $LiNbO_3$; oxygen vacancy migration; memristive effect; electronic synapse

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1. Introduction

Recent advances in information and intelligence technologies, such as the Internet of Things, big data analysis, data-intensive image process, and artificial intelligence, have significantly increased the demand for novel electronic devices that enable fast and efficient data computation [1,2]. The conventional von Neumann architecture is anticipated to encounter inherent limitations due to its bottleneck effect, which arises from serial data processing and high power consumption. This bottleneck is primarily due to the separation of data processing units and memory units in von Neumann computing architectures [3,4]. To address this critical issue, neuromorphic computing devices have garnered substantial interest. Neuromorphic computing aims to replicate the functionality of the human brain, particularly in processing, storing, and transmitting data in parallel [5,6]. The parallel processing capability of neuromorphic computing allows simultaneous data computation across multiple interconnected nodes, which can effectively mimic the neural networks of the human brain. This can lead to exceptional performance in complex data processing, pattern recognition, and autonomous learning, with remarkable power efficiency [7,8].

In biological neural networks, data processing occurs through the modulation of synaptic plasticity, which connects multiple neurons [6,9,10]. The memristive behaviors of analog memristors closely mimic the key functionalities of biological synapses. Specifically, memristors exhibit voltage-controlled dynamic changes in electrical conductance as well as nonvolatile data retention [11]. This allows analog memristors to act as electronic synapses capable of expressing electronic data in multi-level conductance states across a large dynamic range, enabling synaptic weight updates with high linearity and symmetry and ensuring spatiotemporal variability with fluctuation [1,12]. These characteristics enable analog memristors to mimic the learning capabilities of biological synapses.

Consequently, various in-memory architectures, known as memristive synapses, have been demonstrated based on several memristive switching mechanisms, including the electromigration of valence charges (e.g., defect charges [13,14] and metal ions [15,16]), electrochemical metallization [17,18], phase transitions [19,20], ferroelectric polarization [21,22], and redox reactions in organic materials [23,24]. Among these, oxygen vacancy (V_O)-mediated valance charge migration (VCM) in oxide materials is particularly advantageous. The electric field-controlled V_O-VCM not only allows reversible filamentary switching but also enables fine-tuning of resistance levels [25,26]. In essence, the degree of V_O-VCM can be precisely controlled by adjusting the parameters of the applied voltage pulses to the device (e.g., polarity, amplitude, width, and interval) [27].

To demonstrate V_O-VCM-based memristive synapses, various oxide materials such as HfO_2 [28–30], TiO_2 [31,32], WO_3 [33,34], Ta_2O_5 [27,35], and $LiNbO_3$ [36,37] have garnered significant attention due to their intrinsic point defects, diverse growth methods, valence charge control techniques, and excellent resistive switching characteristics. Among these oxide materials, $LiNbO_3$ stands out for its potential to achieve uniform analog switching, owing to its oxygen octahedron structure [38,39]. In rhombohedral $LiNbO_3$, oxygen atoms share faces along the polar trigonal axis, and these oxygen octahedra are interspersed with Li and Nb atoms. This arrangement provides four pathways along the edges of the octahedron, allowing for easy migration of V_O within the lattice [40,41]. Given these intrinsic advantages, $LiNbO_3$-based synaptic devices have recently attracted considerable interest [42–48]. As noted earlier, the degree of V_O-VCM directly influences the synaptic characteristics of memristive devices. Consequently, the V_O-VCM behavior in $LiNbO_3$ can effectively emulate synaptic characteristics, such as the linear and symmetric potentiation/depression of synaptic weights [36,37,44] as well as spike-timing-dependent synaptic plasticity [42]. To enhance the V_O-VCM properties in $LiNbO_3$, several techniques have been recently proposed and demonstrated to control the V_O density in single-crystalline $LiNbO_3$. For example, methods like crystal ion slicing using low-energy Ar^+ irradiation [42–46] and locally tailored strain doping through He^+ or H^+ ion implantation are effective for controlling the V_O density in $LiNbO_3$ [47,48]. However, despite the previse V_O control offered by these techniques, they complicate the device fabrication process. Therefore, a simpler, more straightforward method is needed to fabricate V_O-VCM-mediated $LiNbO_3$ memristors. For future applications in artificial neural networks, it is essential to develop a memristive synapse array in a crossbar architecture that utilizes a simplified fabrication process. In this context, directly growing $LiNbO_3$ onto the electrode material is crucial.

In this work, we investigate the facile fabrication of simple V_O-VCM-based Au/$LiNbO_3$/Pt memristive synapses and characterize their synaptic characteristics. The top-to-bottom Au/$LiNbO_3$/Pt devices were fabricated by directly sputtering $LiNbO_3$ onto the Pt bottom electrode, followed by the formation of an Al top electrode onto the $LiNbO_3$ active layer. Here, we report the effects of $LiNbO_3$ growth temperature on the material properties and their corresponding synaptic characteristics in V_O-VCM-based Au/$LiNbO_3$/Pt memristors. To provide insight into the device operation, the charge transport mechanisms are also thoroughly analyzed and discussed in detail.

2. Experimental Details

Figure 1a shows the fabricated device structure of the top-to-bottom contact two-terminal Al/$LiNbO_3$/Pt memristor. First, a Ti adhesion layer (≈3 nm thick) was deposited by D.C. sputtering at 450 °C onto the SiO_2/Si substrate to enhance adhesion between the Pt bottom electrode and the substrate. Subsequently, a 120 nm thick, mirror-like Pt (111) layer was deposited onto the Ti adhesion layer via D.C. sputtering at 500 °C. Next, a 50 nm thick $LiNbO_3$ layer was grown at 180–320 °C on the Pt/SiO_2/Si substrate using R.F. magnetron sputtering with an R.F. power of 80 W. During the 60 min $LiNbO_3$ deposition, the working pressure was maintained at 25 mTorr, while a gas mixture of Ar (12 sccm) and O_2 (6 sccm) was continuously supplied. Finally, circular Al top electrodes (100 µm in diameter) were formed onto the $LiNbO_3$ layers.

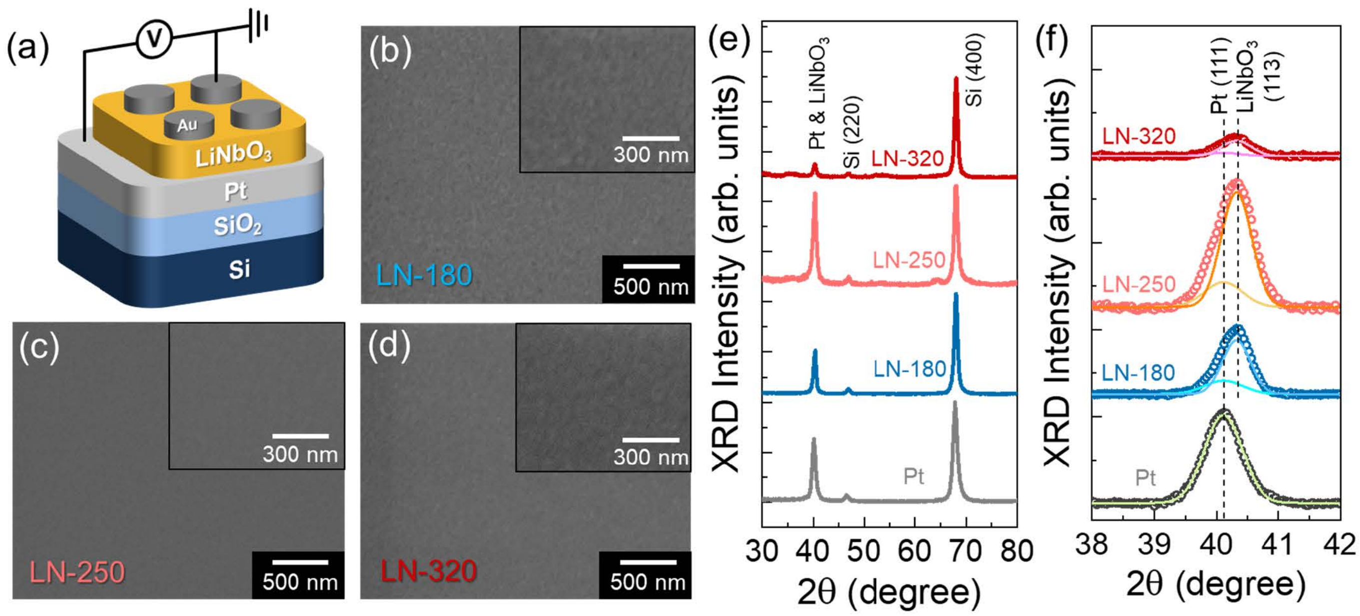

Figure 1. (**a**) Schematic of the Al/$LiNbO_3$/Pt memristive synapse. Surface FE-SEM images of the (**b**) LN-180, (**c**) LN-250, and (**d**) LN-320 layers grown on (111) Pt/SiO_2/Si substrates at different temperatures of 180, 250, and 320 °C, respectively. (**e**) Wide-angle XRD patterns of the LN-180, LN-250, and LN-320 samples. (**f**) Deconvoluted XRD pattern at the Bragg angle of ~40.1°, showing the portions of (111) Pt and (113) $LiNbO_3$ phases. The insets in (**b**–**d**) show the zoomed-in view of each sample.

The surface morphology of the $LiNbO_3$ layers was monitored using field-emission scanning electron microscopy (FE-SEM) with a Hitachi S4800 electron microscope (Tokyo, Japan). Crystallographic structures and lattice phases were analyzed via X-ray diffraction (XRD) using a Bruker D8 Advance (Madison, WI, USA) with a Cu Kα_1 radiation source. The valence states of the $LiNbO_3$ components were examined using X-ray photoelectron spectroscopy (XPS) with a Thermos Fisher Scientific ESCALab250Xi system (Waltham, MA, USA). The ferroelectric properties of the $LiNbO_3$ layers were evaluated using polarization vs. voltage (P–V) measurements with a Precision RT66C Ferroelectric Tester (Radiant, Albuquerque, NM, USA). The electrical characteristics and synaptic functions of the Al/$LiNbO_3$/Pt memristor were assessed using a B1500A/B1530A semiconductor parameter analyzer (Keysight, Santa Rasa, CA, USA).

3. Results and Discussion

In thin-film devices, the homogeneity of crystal grains is crucial for maintaining stable on-state current flow because crystalline defects such as grain boundaries and pits can increase leakage current, potentially leading to device failure. To investigate the effect of growth temperature on the film texture, we deposited three different $LiNbO_3$ layers at 180, 250, and 320 °C and assessed their morphological properties. For simplicity, we refer to the samples grown at these temperatures as LN-180, LN-250, and LN-320, respectively. As shown in the FE-SEM image of LN-180 (Figure 1b), the $LiNbO_3$ layer grown at the low temperature of 180 °C displayed an inhomogeneous and rough surface. However, when the growth temperature increased to 250 °C, the LN-250 sample exhibited a smooth and well-merged surface (Figure 1c). In contrast, the surface of the LN-320 sample became rough again when the growth temperature increased up to 320 °C (Figure 1d).

The surface morphology is closely related to the crystallographic properties of thin films. Therefore, we performed XRD analysis on the $LiNbO_3$ samples. Figure 1e shows the XRD patterns of LN-180, LN-250, and LN-320 layers deposited onto Pt (111)/SiO_2/Si substrates. In all samples, three predominant XRD peaks were observed at Bragg angles of ~40.1°, ~46.7°, and ~67.8°. The peaks at ~46.6° and ~67.8° are well known to correspond to the (220) and (400) crystal planes of diamond-structured Si [49], while the peak at approximately 40° is associated with both the (111) Pt and (113) $LiNbO_3$ phases [50]. As deconvoluted in Figure 1f, the XRD peak at ~40.1° originated from the (111) phase of cubic Pt [51], while that at ~40.3° was attributed to the (113) phase of rhombohedral $LiNbO_3$ [52]. According to a previous study by Ono et al. [50], when $LiNbO_3$ is grown on a (111) Pt substrate, it tends to increase along preferential orientations perpendicular to the (001) and (113) directions. This suggests that the $LiNbO_3$ layers in this study were effectively grown along the rhombohedral (113) phase direction without segregation into Nb_2O_5 and $LiNb_3O_8$. When comparing the intensity of the (113) $LiNbO_3$ peak, the XRD results correlate well with the FE-SEM images. Specifically, the LN-250 sample exhibited a stronger (113) $LiNbO_3$ peak intensity than LN-180, while LN-320 showed a significant degradation in crystallinity. Based on the XRD and FE-SEM analyses, we can conclude that the $LiNbO_3$ sample grown at 250 °C is more suitable for fabricating high-quality memristive devices than those grown at other temperatures.

Next, the valence states of the elemental species were investigated through XPS analysis. Figure 2a–c present the Li 1s and Nb 4s core-level spectra of the $LiNbO_3$ layers grown at 180–320 °C, respectively. In all samples, distinct peaks were observed for both Li 1s and Nb 4s at 54.9 and 60.3 eV, respectively.

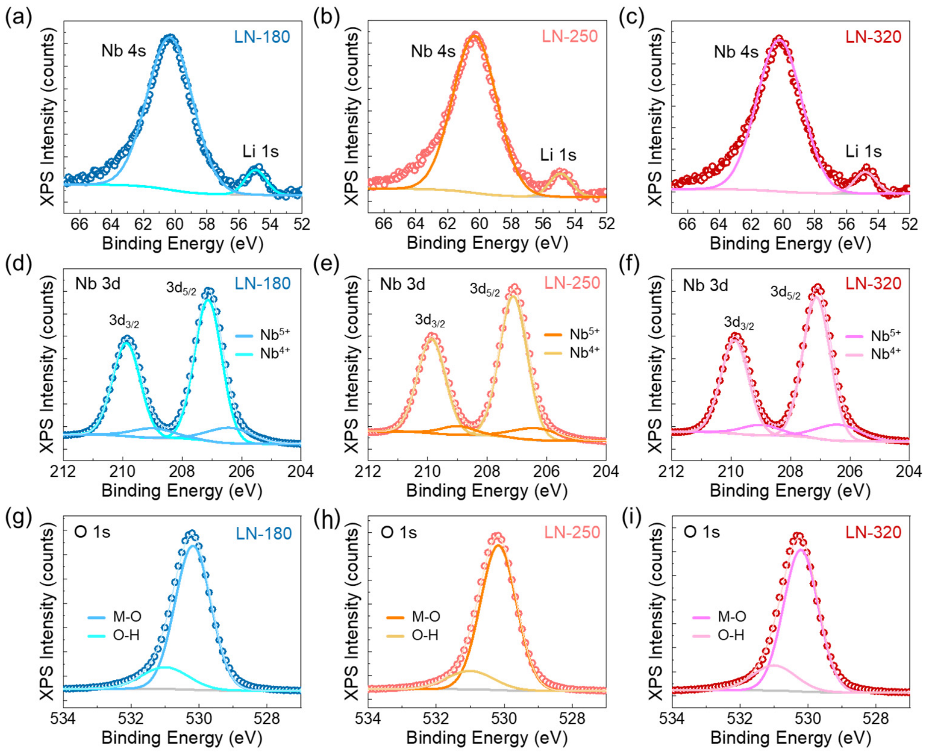

Figure 2. XPS spectra of the $LiNbO_3$ layers grown at different temperatures. Li 1s and Nb 4s core levels of (**a**) LN-180, (**b**) LN-250, and (**c**) LN-320. Nb 3d core levels of (**d**) LN-180, (**e**) LN-250, and (**f**) LN-320. O 1s core levels of (**g**) LN-180, (**h**) LN-250, and (**i**) LN-320.

Regardless of the growth temperature, there were no significant changes in the peak positions or the intensity ratio between Li 1s to Nb 4s, as seen in Figure 2a–c. This indicates that the stoichiometric composition of Li and Nb remained nearly identical across the LN-180, LN-250, and LN-320 samples [53,54]. To further explore the valence states of Nb, high-resolution XPS measurements were performed for the Nb 3d core level. Figure 2d–f show that the Nb 3d spectrum can be deconvoluted into two distinct components: Nb^{5+} and Nb^{4+}. The doublet peaks of $3d_{5/2}$ at 209.8 eV and $3d_{3/2}$ at 207.1 eV correspond to Nb^{5+} [54,55], while additional doublet peaks at 209.1 eV ($3d_{5/2}$) and 206.4 ($3d_{3/2}$) represent Nb^{4+}. The presence of Nb^{4+} in $LiNbO_3$ is closely related to the formation of V_O, which compensates for two electrons within the Nb site [56,57]. Eventually, V_O acts as a donor within the $LiNbO_3$ lattice [58]. The existence of V_O was further confirmed through the O 1s core-level spectra, as shown in Figure 2g–i, where two characteristic oxygen bonds are evident: Nb-O-Li at 530.1 eV and V_O at 531 eV [53].

As previously discussed, V_O plays a crucial role in facilitating the VCM-based memristive switching behavior in $LiNbO_3$. Therefore, we evaluated the current–voltage (I–V) characteristics of the Al/$LiNbO_3$/Pt memristors. It was observed that the I–V characteristics varied depending on the morphological properties of $LiNbO_3$. Particularly, the memristors fabricated with LN-320 exhibited unstable and leaky I–V curves, while the devices using LN-180 and LN-250 demonstrated stable memristive switching characteristics (see Figure S1). However, when the sweep voltage (V_{sw}) exceeded ±3 V, the LN-180 device also showed unstable I–V behaviors with sudden glitches (Figure S1a–c). Based upon these results, we accordingly focused further electrical characterization on the LN-250 sample. As shown in Figure 3a, the LN-250 memristor clearly revealed voltage polarity-dependent asymmetric hysteresis loops (see the inset of Figure 3a). Moreover, both the memory window and on-state current increased progressively with increasing V_{sw}. The device demonstrated robust self-rectifying memristive characteristics [42–48], which are advantageous for controlling the linear and symmetric potentiation/depression of synaptic weights [36,44] and for suppressing sneak path currents during the depression process [59,60].

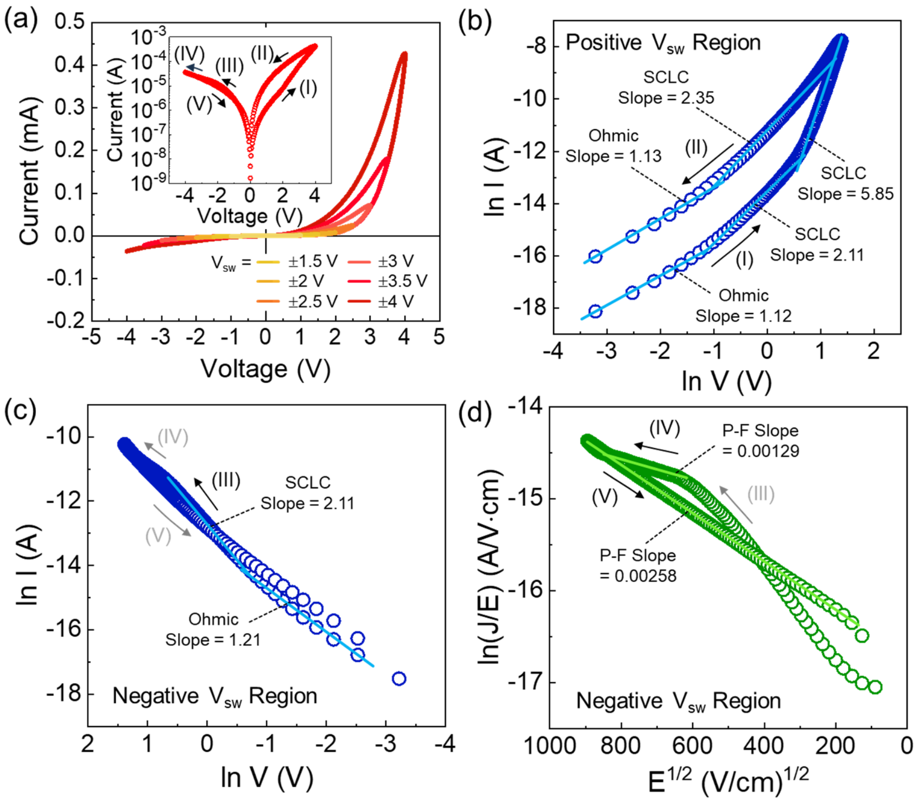

Figure 3. (**a**) I–V characteristic curves of the Al/$LiNbO_3$/Pt memristive synapse (LN-250) measured under various V_{sw} ranges. SCLC plots in the (**b**) positive and (**c**) negative V_{sw} regions. (**d**) P-F plot in the negative V_{sw} region. The inset in (**a**) illustrates the hysteretic behavior represented by the semi-logarithmic I–V curve.

In V_O-VCM-based memristors, the memristive switching behaviors can be attributed to two primary mechanisms. The first involves the migration and redistribution of V_O, leading to changes in electrical conductance by forming V_O channels, resulting in filamentary conduction (i.e., memristive switching via filamentary conduction) [36,45]. The second mechanism is the gradual change in the on-state current, mediated by V_O-VCM, which modulates the potential barrier at the electrode/oxide interface (i.e., memristive switching via interfacial barrier modulation) [44,46,61]. To gain further insight into the observed switching behavior of the LN-250 memristor, we analyzed its conduction mechanism using the space-charge-limited conduction (SCLC) model [62,63], which is associated with the V_O-VCM behavior in oxide materials [43–46]. The I–V relationship for SCLC conduction is given by the following:

$$J_{SCLC} = \frac{9}{8}\varepsilon_i \mu \theta \frac{V^2}{d^3}, \tag{1}$$

where ε_i is the static dielectric constant of the oxide, μ is the carrier mobility, θ is the ratio of free carrier density to trapped charge density, and d is the oxide thickness.

In Region I (see inset in Figure 3a), when a low positive voltage ($V_{sw} > 0$) was applied to the device, the current increased linearly with the applied voltage (i.e., slope ≈ 1.12). As the magnitude of V_{sw} further increased, the current followed Child's law with a slope of approximately 2.11 (i.e., $I \propto V^2$). After this point, the slope sharply increased to 5.85, indicating that the high-electric field created a temporary conductive area region, corresponding to trap-limited SCLC [36,45]. Upon returning to the lower V_{sw} region in Region II (see inset in Figure 3a), the current followed Child's law again, with a slope of approximately 2.35, consistent with the trap-filled SCLC mechanism [46]. In the negative V_{sw} region (Region III, Figure 3c), the slope was found to be 2.11, also consistent with the trap-limited SCLC mechanism. However, in Region IV, at higher negative voltages, the slope changed, indicating that charge transport shifted to a different mechanism than SCLC. To identify the appropriate mechanism in Region IV, we replotted and analyzed the I–V curve using several transport models, such as Poole–Frenkel (P-F) emission, Fowler-Northeim tunneling, and Schottky emission. Then, we found that the P-F emission model provided the best fit to the measured I–V curve (see Figure S2). According to the literature [48,64], P-F emission is predominantly governed by the trap-limited bulk conduction mechanism, given by the following:

$$J_{PF} = q\mu N_c E exp\left[\frac{-q\left(\phi_T - \sqrt{qE/\pi\varepsilon_0\varepsilon_r}\right)}{kT}\right], \tag{2}$$

where q is the elementary charge, μ is the electronic drift mobility, N_c is the density of states in the conduction band, E is the electric field, k is a Boltzmann constant, ϕ_T is the trap energy level, ε_0 is the permittivity of free space, and ε_r is the dielectric constant of the material. From this, the slope in the P-F plot can be given as follows:

$$Slope = m\left(\frac{q^3}{\pi\varepsilon_0\varepsilon_r (kT)^2}\right)^{1/2}, \tag{3}$$

where m is the constant that distinguishes the main conduction mechanism. For example, m = 1 for P-F emission, and m = 2 for shallow traps [64,65]. From the $\ln(J/E)$ vs. $E^{1/2}$ plot (Figure 3d), two distinct slopes were observed: 0.00129 and 0.00258 in Regions IV and V, respectively. Since the refractive index (${\varepsilon_r}^{1/2}$) of $LiNbO_3$ is reported to be 2.28 in the literature [43,48,66], the value of m in Region IV was found to be unity. This suggests that P-F emission dominates the charge conduction in Region IV. Similarly, the m value in Region V was found to be 2, indicating that shallow trap-mediated P-F emission governs the conduction in this region.

Based on the above results, we here interpret the plausible charge transport mechanism in the present Au/$LiNbO_3$/Pt memristor. Figure 4 illustrates the V_O-VCM-mediated SCLC behavior at various bias voltages. From the XPS results, we assume the existence of V_O in the $LiNbO_3$ active layer. During the fabrication of the Au/$LiNbO_3$/Pt device, the $LiNbO_3$ layer was grown directly onto the Pt metallic electrode. Consequently, a large amount of V_O is likely to be distributed at the bottom region of $LiNbO_3$ near the Pt electrode, as the high density of grain boundaries forms in the initial $LiNbO_3$ layer deposited on the Pt electrode [45]. At zero bias (Figure 4a), the potential barrier at the $LiNbO_3$/Pt interface (i.e., Schottky-like barrier at the metal/oxide interface) is expected to be slightly lower due to the reduction in electrochemical potential caused by V_O [43,46]. Similarly, the potential barrier at the Au/$LiNbO_3$ interface is also reduced, as abundant V_O is generated during the final growth stage of $LiNbO_3$ that resides underneath the Au top electrode. As shown on the right side of Figure 4a, the fabricated Au/$LiNbO_3$/Pt device thus acts like a two-diode-connected resistor. Here, it should be noted that the exact origin of the Schottky-like potential barrier remains unclear. However, prior studies [43–46,67–70] have observed rectifying behaviors at metal/$LiNbO_3$ interfaces (e.g., Au, Cr, Pt, and Ti), likely due to V_O-induced Fermi-level pinning [69,70], which contributes to the formation of Schottky-like barriers.

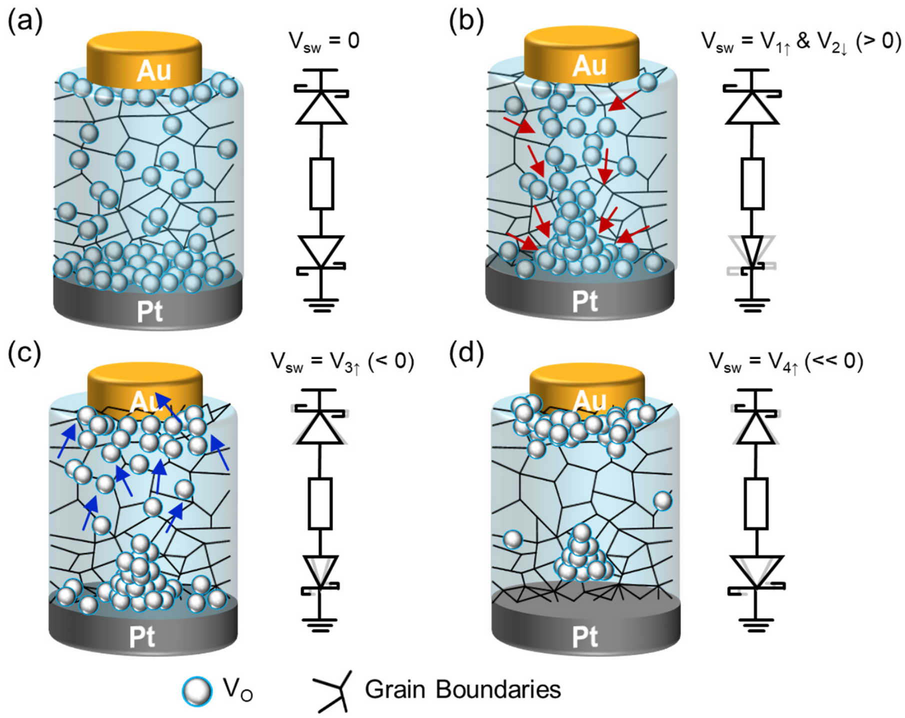

Figure 4. V_O-VCM behaviors in the Al/$LiNbO_3$/Pt memristive synapse at (**a**) $V_{sw} = 0$ V, (**b**) $V_{sw} = V_{1\uparrow}$ and $V_{2\downarrow}$ (>0), (**c**) $V_{sw} = V_{3\downarrow}$, (<0), and (**d**) $V_{sw} = V_{4\uparrow}$ (<<0).

When a positive bias ($V_{sw} = V_{1\uparrow} > 0$) is applied with the Pt electrode grounded, V_O migrates (i.e., V_O-VCM) toward the Pt electrode along the grain boundaries (Figure 4b), resulting in the formation of localized V_O clusters (i.e., V_O group) near the Pt interface due to vacancy–vacancy interactions [71,72]. Simultaneously, the charges from the migrating V_O contribute to trap-controlled SCLC within the $LiNbO_3$ active layer (e.g., Region I). As V_O clusters near the Pt electrode, they reduce the local electrochemical potential, further lowering the potential barrier at the $LiNbO_3$/Pt interface [43,47]. This process sustains a high on-state current at a relatively high bias voltage (V_{sw}). The on-state current persists until the V_O clusters are redistributed by applying a negative V_{sw}. Therefore, the high on-state current remains even when the V_{sw} decreases to a lower voltage (e.g., $V_{sw} = V_{2\downarrow} < V_{1\uparrow}$ in Region II), leading to memristive hysteresis in the I–V characteristics of the Au/$LiNbO_3$/Pt device.

After switching the voltage (V_{sw}) to the negative $V_{3\uparrow}$ (Figure 4c), the clustered V_O groups begin to disintegrate, allowing V_O to migrate toward the Au/$LiNbO_3$ interface. This initiates trap-controlled SCLC at this bias state (e.g., Region III). It is important to note that the density of migrated V_O will not increase further, even with the application of a higher negative V_{sw}. This is because V_O clusters near the $LiNbO_3$/Pt interface tend to remain stable. Specifically, since V_O tends to stabilize in its neutral valence state ($V_O{}^0$) [73], the density of electromigrating V_O is limited. Hence, the charge transport mechanism changes from trap-controlled SCLC to P-F emission, characterized by minimal current flow (e.g., Region IV). When a more negative voltage ($V_{sw} = V_{4\uparrow} << 0$) is applied, the conducting path is abruptly disconnected due to the rupture of [47] localized V_O clusters at the $LiNbO_3$/Pt interface (Figure 4d). Consequently, the potential barrier at the $LiNbO_3$/Pt interface significantly increases, allowing only a small current to flow through the shallow trap-mediated P-F emission (e.g., Region V). Therefore, this type of Au/$LiNbO_3$/Pt memristor exhibits the rectified asymmetric hysteresis characteristics.

The V_O-VCM-mediated potential barrier modulation presents an opportunity to emulate synaptic functions because multiple memristive states with varying on-state current levels can be achieved by adjusting the potential barrier at both the Au/$LiNbO_3$ and $LiNbO_3$/Pt interfaces. To explore this, we examined the synaptic functions of the LN-250 memristor. First, we evaluated the dependence of memristive hysteresis characteristics on the number of voltage sweeps (n_{sw}). Figure 5a,b show the evolution of the on-state current observed after applying 20 consecutive voltage sweeps with a dual-sweep mode and a single-sweep mode, respectively. For the dual-sweep mode with a sweep time (t_{sweep}) of 2 s (see inset in Figure 5a), the device clearly exhibited the hysteresis loops, while the maximum current increased rapidly and tended to saturate as the n_{sw} increased (see also Figure 5c). In the case of the single-sweep mode with a t_{sweep} of 1 s (see inset in Figure 5b), similarly, the maximum current increased with increasing the n_{sw} (see also Figure 5d). These indicate that the LN-250 memristor could demonstrate data accumulation in response to the number of consecutive voltage biases (i.e., cumulative learning behavior). Additionally, the device displayed the stable retention characteristics of the multilevel conductance states, which are essential for demonstrating the synaptic functions. As shown in Figure 5e, the device exhibited tenacious data retention characteristics for multiple memory states. Namely, four clear multilevel states, which had been performed by applying voltage pulses with pulse amplitudes (V_{pulse}) of +5, +4, +3, and −4 V, were tenaciously maintained after 5000 s (Figure 5e). Similarly, as can be seen from Figure 5f, four different tenacious memory states were also achieved by changing the pulse width (t_{pulse}).

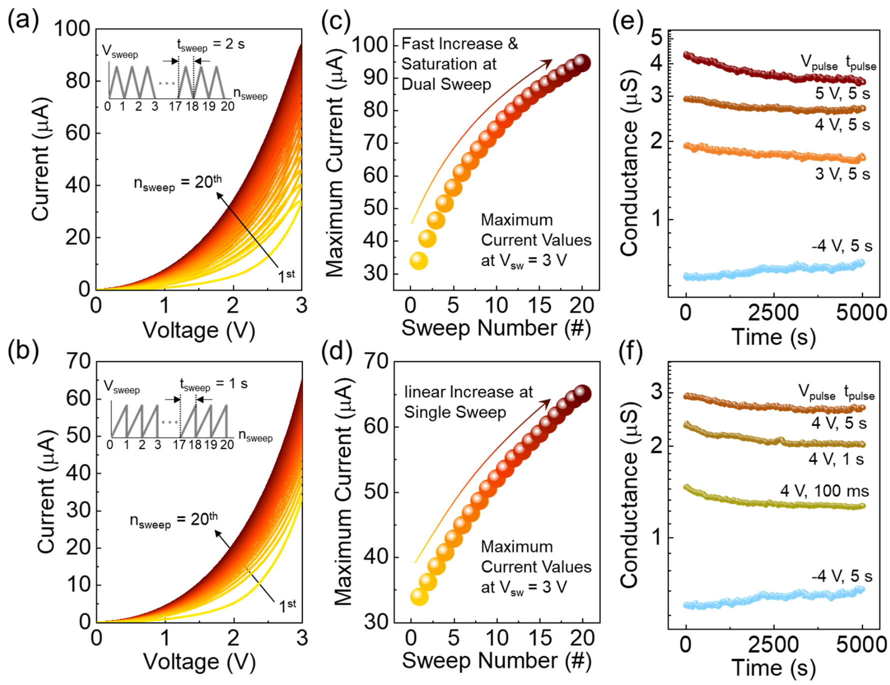

Figure 5. I–V characteristic curves measured over 20 consecutive voltage sweeps at V_{sw} = 0–3 V performed by the (**a**) dual-sweep mode and the (**b**) single-sweep mode. Maximum current evolution as a function of n_{sw} for the (**c**) dual-sweep and (**d**) single-sweep modes. Retention characteristics at quadruple states demonstrated by changing the (**e**) magnitude of V_{pro} and the (**f**) value of t_{pro}.

These basic learning behaviors and tenaciously retainable multi-states characteristics are evident for the synaptic activity of the Au/$LiNbO_3$/Pt memristor. To examine the synaptic functionality, firstly, we thus measured the excitatory postsynaptic current (EPSC) characteristics. Figure 6a displays the EPSC transient curves of the LN-250 memristor, measured at a read-out voltage (V_{read}) of 1.2 V after applying a single voltage pulse with varying V_{pulse} and t_{pulse}. When a single voltage pulse (i.e., a presynaptic stimulus) was applied to the device, the electric pulse-stimulated postsynaptic current (ΔPSC) stabilized rapidly after an initial decay. Notably, the magnitude of the retained ΔPSC depended on both V_{pulse} and t_{pulse}. For instance, when V_{pulse} = 4 V (left panel of Figure 6a), the residual ΔPSC increased with longer t_{pulse}. Furthermore, the device demonstrated a V_{pulse}-dependent enhancement of ΔPSC, with greater ΔPSC values observed at V_{pulse} = 4.5 V (right panel of Figure 6a) compared to V_{pulse} = 4 and 4.25 V. These behaviors are similar to biological synapses, where synaptic plasticity depends on the duration and strength of the stimuli. Thus, it can be inferred that applying consecutive stimuli with moderate V_{pulse} and t_{pulse} gradually strengthens the synaptic plasticity, enabling the LN-250 memristor to mimic biological synaptic functions.

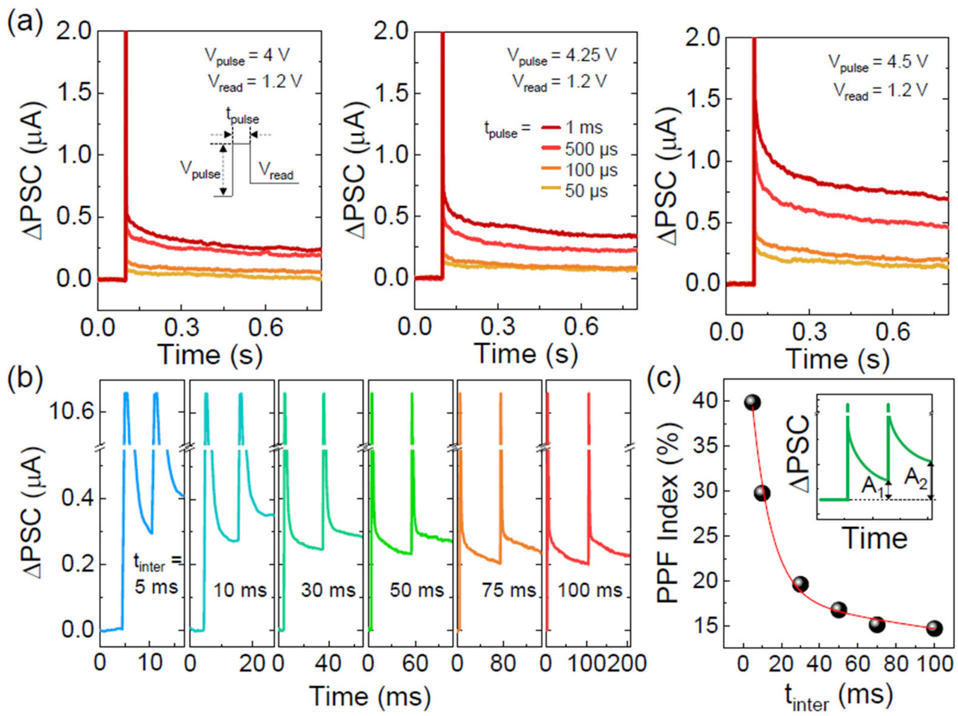

Figure 6. Basic synaptic characteristics of the Al/$LiNbO_3$/Pt memristive synapse (LN-250). (**a**) EPSC functions performed at different V_{pulse} (4–4.5 V) with different t_{pulse} (50 μs–1 ms). (**b**) Dependence of PPF characteristics on t_{inter}, where V_{pulse}, t_{pulse}, and V_{read} were fixed at 4 V, 500 μs, and 1.2 V, respectively. (**c**) PPF index as a function of t_{inter}.

The above hypothesis can be tested by examining the short- and long-term-memory (STM/LTM) characteristics. As a first step, we evaluated the paired pulse facilitation (PPF) characteristics to investigate the short-term enhancement of synaptic strength. PPF measures the cumulative ΔPSC when two consecutive stimuli are applied. The interval between the two pulses (t_{inter}) is critical for determining PPF activity because the ΔPSC triggered by the second pulse plays a key role for updating the synaptic weight from its previous state. To assess PPF, we measured the ΔPSC values as a function of t_{inter}, which varied from 5 to 100 ms, while keeping t_{pulse}, V_{pulse}, and V_{read} constant at 500 μs, 4 V, and 1.2 V, respectively. Similar to the EPSC characteristics, the PPF curves exhibited typical transient behavior in response to the applied voltage pulses. However, in the case of PPF, the residual ΔPSC value increased following the second pulse (Figure 6b), indicating that the synaptic weights were enhanced from the initial ΔPSC triggered by first pulse to the updated ΔPSC state induced by the second pulse. Notably, as t_{inter} increased, the updated ΔPSC values significantly decreased, leading to a weakening of data retention. This is likely due to the diffusion of grouped V_O clusters into the bulk region during t_{inter} period, driven by concentration gradients [73]. Furthermore, the difference between the first pulse-initiated and second pulse-updated ΔPSC values ($A_2 - A_1$) decreased exponentially with increasing t_{inter}. Consequently, the PPF index ($(A_2 - A_1)/A_1 \times 100\%$) also showed an exponential decay as a function of t_{inter} (Figure 6c). This t_{inter}-dependent PPF decay can be attributed to two distinct phases of synaptic weight relaxation [74,75]:

$$PF\ index = C_1 \exp(-t/\tau_1) + C_2 \exp(-t/\tau_2), \quad (4)$$

where C_1 and C_2 are the initial PPF values for the rapid and slow relaxation phases, respectively; τ_1 and τ_2 are the time constants associated with these two phases, respectively. By fitting the experimental data to Equation (4) (shown as the red line in Figure 6c), τ_1 and τ_2 of the LN-250 memristor were estimated to be 10.09 and 434.08 ms, respectively. In biological synapses, the fast relaxation time enables producing a temporally enhanced synaptic response by short-interval stimuli through rapid resetting of synaptic response. In contrast, the slow relaxation time supports long-term synaptic plasticity even with prolonged intervals in between repeated stimuli [76]. These time constants of biological synapses differ, depending on the characteristics of various synapses (e.g., neurotransmittances, receptor properties, and synaptic roles) [77,78]. Among biological synapses that are responsible for the learning action, the rapid relaxation time typically ranges from a few milliseconds to tens of milliseconds, while the slow relaxation time persists from a hundred milliseconds to a few seconds [79,80]. Therefore, it can be surmised that the present Au/$LiNbO_3$/Pt memristor may effectively replicate the basic synaptic functions of biological synapses.

In biological synapses, the transition from STM to LTM plays a fundamental role in synaptic learning. STM temporarily updates the memory state, with the corresponding synaptic weight rapidly reverting to its initial state. In contrast, LTM represents a semipermanent change in synaptic weight, achievable through the application of a large number of consecutive stimuli. This is akin to the rehearsal ability of the human brain [74,81], which can enhance the STM-to-LTM transition probability through repetitive practices. Such a rehearsal action can also be demonstrated in the Au/$LiNbO_3$/Pt memristor. After selecting the pulse parameters (i.e., V_{pulse} = 4 V, t_{pulse} = 500 µs, and t_{inter} = 9.5 ms) based on multiple assessments of varying key pulse parameters (see Figure S3), we investigated the STM-to-LTM transition behavior, i.e., rehearsal activity, as a function of the number of applied pulses (n_{pulse} = 16, 32, 64, and 128). As shown in Figure 7, consecutive potentiation pulses led to a sequential update of the synaptic weight. Notably, the device exhibited a strong dependence on both the updated synaptic weight and its retention characteristics as a function of n_{pulse}. Specifically, the consecutive potentiation pulses facilitated an increase un ΔPSC values as n_{pulse} increased. Furthermore, the transient time (τ_{tran}) of the updated ΔPSC also increased from 0.084 to 0.679 s as n_{pulse} was increased from 16 to 128, respectively. These results indicate that the device supports STM-to-LTM transition activity, which is characteristic of synaptic learning and memory functions. This STM-to-LTM transition in the Au/$LiNbO_3$/Pt memristor can be attributed to V_O-VCM-mediated potential barrier modulation. As discussed earlier, applying a positive bias voltage promotes the V_O-VCM behavior within the $LiNbO_3$ active layer. Consequently, the degree of V_O-VCM increases with consecutive voltage pulses, leading to enhanced V_O clusterization. This, in turn, increases SCLC in the $LiNbO_3$ active layer and reduces the potential barrier at the $LiNbO_3$/Pt interface. Moreover, the strong V_O clusterization results in robust retention of the hysteretic memory state. Thus, both ΔPSC and τ_{tran} increase as n_{pulse} increases, enabling the effective STM-to-LTM transition in the Au/$LiNbO_3$/Pt memristor.

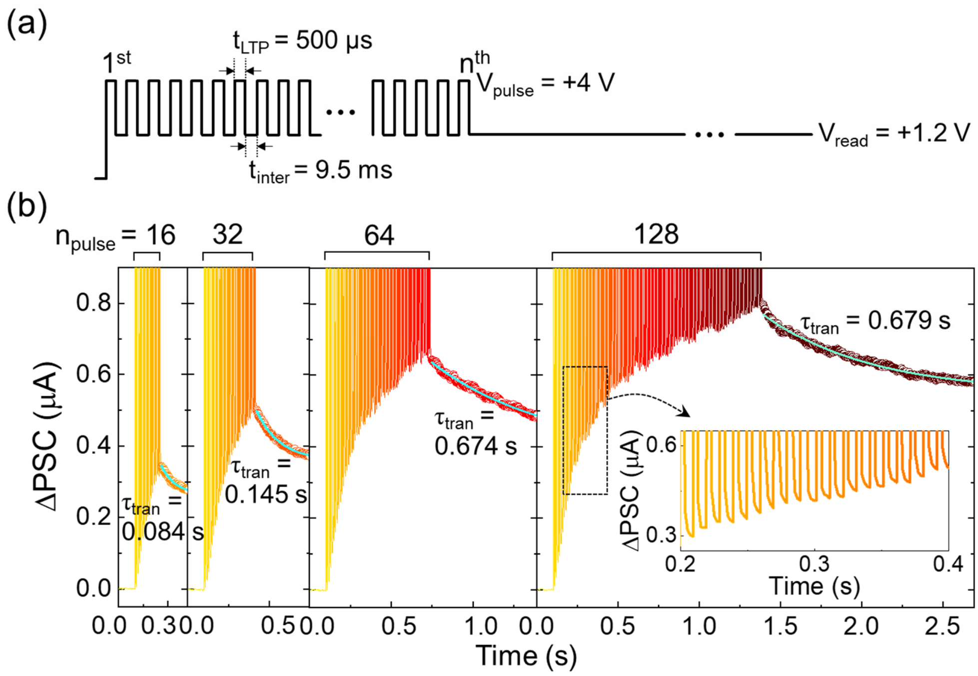

Figure 7. STM-to-LTM transition characteristics of the Al/$LiNbO_3$/Pt memristive synapse (LN-250). (**a**) Applied pulse scheme. (**b**) Dependence of potentiation and data retention characteristics on the number of applied pulses. The inset in (**b**) shows a zoomed-in view of the ΔPCS transient curves.

After observing the STM-to-LTM transition, we examined the long-term potentiation (LTP) and long-term depression (LTD) characteristics by applying continuous 100 LTP and 100 LTD pulses (i.e., V_{LTP} and V_{LTP}). To evaluate the dependence of the ΔPSC dynamic range on the applied V_{pulse} magnitude, we varied both V_{LTP} and V_{LTP} amplitudes, while other parameters were fixed at t_{LTP} = 600 μs, t_{LTD} = 1 ms, t_{inter} = 10 ms, and V_{read} = 1.2 V (see the upper panel of Figure 8a). As shown in Figure 8a, the dynamic range of ΔPSC increased with both V_{LTP} and V_{LTP}. For high learning accuracy and efficient training in the electronic synapse, both a wide dynamic range and good linearity are essential [82]. However, the LN-250 memristor exhibited non-linear and asymmetric LTP/LPD behavior. To improve both the linearity and symmetricity of the LTP/LTD characteristics, pulse modulation techniques such as the pulse magnitude modulation [83,84] and pulse frequency modulation [12,85] have been suggested in the literature. Therefore, we attempted to improve both linearity and symmetricity by using incremental V_{LTP} and V_{LTP} schemes while keeping other parameters fixed at t_{LTP} = 300 μs, t_{LTD} = 500 μs, t_{inter} = 10 ms, and V_{read} = 1.2 V (see the upper panel of Figure 8b). As shown in Figure 8b, both linearity and symmetricity were significantly improved using the incremental pulse scheme.

As noted above, the linearity and symmetricity of the LTP/LTD characteristics directly affect the learning accuracy and training efficiency of the synapse. To assess the impact of these characteristics on image pattern recognition accuracy, we performed a theoretical simulation using the Modified National Institute of Standard and Technology (MNIST) handwritten digit dataset. The MNIST simulation was based on the backpropagation learning rule in an artificial neural network system, which includes 60,000 and 10,000 handwritten training and testing images, respectively. For this simulation, we assumed that the neural network consisted of a synthetic multilayer structure, including one input, three hidden, and one output layers (Figure 9a). Each training image of a handwritten digit was designed as a 28 × 28 pixel grid, converted into 784 input neuron vectors for the input layer. These input vectors were propagated through the three hidden layers (128 → 64 → 32 nodes) to the 10 output neurons. Based on updated synaptic weights for each test image, the pattern recognition accuracy was determined at the output layer by comparing the actual database values with the predicted output value. Then, the overall accuracy for all the test images was calculated as a percentage of the correct prediction by matching and comparing the predicted values with the true values. Through multiple runs of the MNIST simulation using the experimental data from Figure 8a,b, we found that the incremental pulse scheme achieved higher recognition accuracy than the identical pulse scheme (Figure 9b). For example, the pattern recognition accuracy increased from 93.5% (using the identical pulse scheme at 10 epochs) to 95.2% (using the incremental pulse scheme at 10 epochs). These results confirm that higher accuracy can be achieved when symmetric and linear LTP/LTD data are introduced to the neural network.

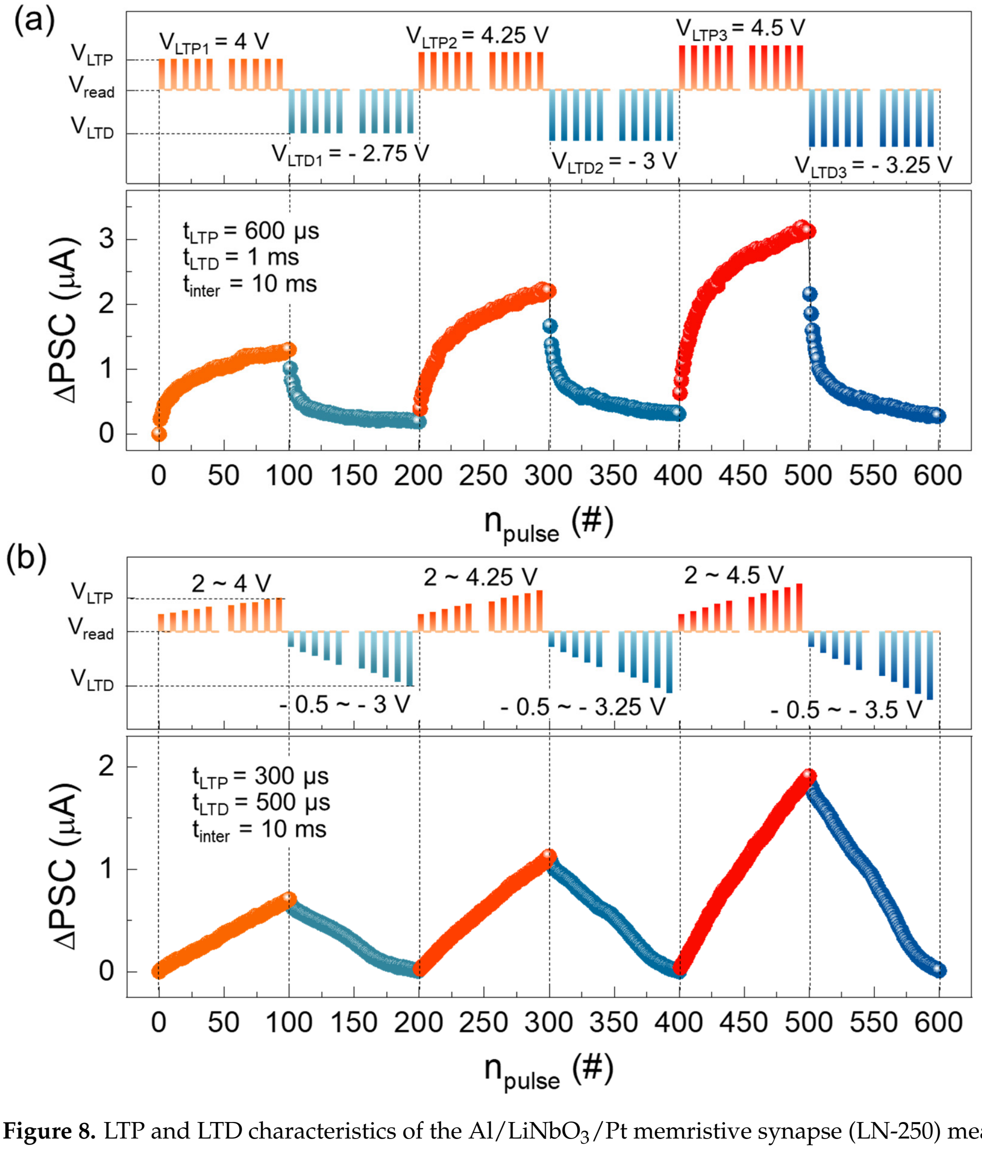

Figure 8. LTP and LTD characteristics of the Al/$LiNbO_3$/Pt memristive synapse (LN-250) measured under (**a**) identical and (**b**) incremental pulse schemes. The upper and lower panels in each figure show the applied pulse scheme and the measured LTP/LTD data, respectively.

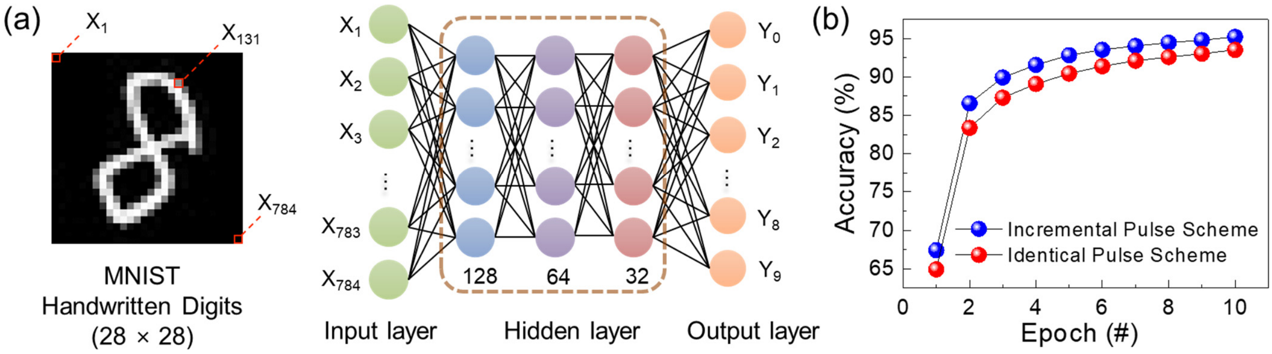

Figure 9. (**a**) Schematic of the artificial neural network designed for the MNIST simulation. (**b**) Pattern recognition accuracy as a function of the epoch. The data points in (**b**) were obtained from the MNIST simulation using the experimental LTP/LTD data shown in Figure 8.

Finally, to examine the perceptron role of the LN-250 memristor as an electronic synapse, we measured its spike-timing-dependent plasticity (STDP) characteristics. In an electronic synapse, the perceptron role can be identified by observing the temporal difference between pre- and postsynaptic states [86–88]. The STDP measurement allows us to determine the synaptic weight change (Δw) by varying the timing difference between pre- and postsynaptic spike pulses (i.e., $\Delta t = t_{post} - t_{pre}$). The variation of Δt-dependent Δw is typically used to assess the perceptron role of the electronic synapse. As shown in Figure 10, the LN-250 memristor successfully demonstrated four different types of Hebbian learning rules. Specifically, the asymmetric Hebbian (Figure 10a), asymmetric anti-Hebbian (Figure 10b), symmetric Hebbian (Figure 10c), and symmetric anti-Hebbian (Figure 10d) rules were realized by varying the polarity and/or shape of the applied spike pulses (see Figures S4–S7 for detailed Δt-dependent spike pulse shapes). As seen in Figure 10a–d, in all four cases, Δw decays exponentially with increasing Δt. From the Δt-dependent Δw decay curves, the STDP time constant (τ_s) can be parametrized using the following equations [89]:

$$\Delta w = A \cdot exp\left(-\frac{\Delta t^2}{\tau_s^2}\right) + \Delta w_0 \text{ (for symmetric Hebbian rules)} \quad (5)$$

$$\Delta w = A \cdot exp\left(-\frac{\Delta t}{\tau_s}\right) + \Delta w_0 \text{ (for asymmetric Hebbian rules)} \quad (6)$$

where A is the scaling factor, and Δw_0 is the constant synaptic weight that is independent of Δt-dependent Δw. By fitting the experimental data to Equations (5) and (6), the τ_s values were estimated to be 21.63, 40.26, 16.21, and 24.58 ms for the asymmetric Hebbian, asymmetric anti-Hebbian, symmetric Hebbian, and symmetric anti-Hebbian cases, respectively. These values fall within the timescale typical for biological synapses in the human brain (i.e., $\tau_s \approx$ a few tens of milliseconds) [90]. Furthermore, since rapid Δw changes within a narrow Δt timescale are essential for parallel computing in neural networks, clear decay of Δt-dependent Δw is advantageous for future neuromorphic circuit applications. In summary, the present Au/$LiNbO_3$/Pt memristive synapse demonstrated excellent functionalities as an electronic synapse, having comparable and even better synaptic performance than other V_O-VCM-based memristive synapses (See Table 1).

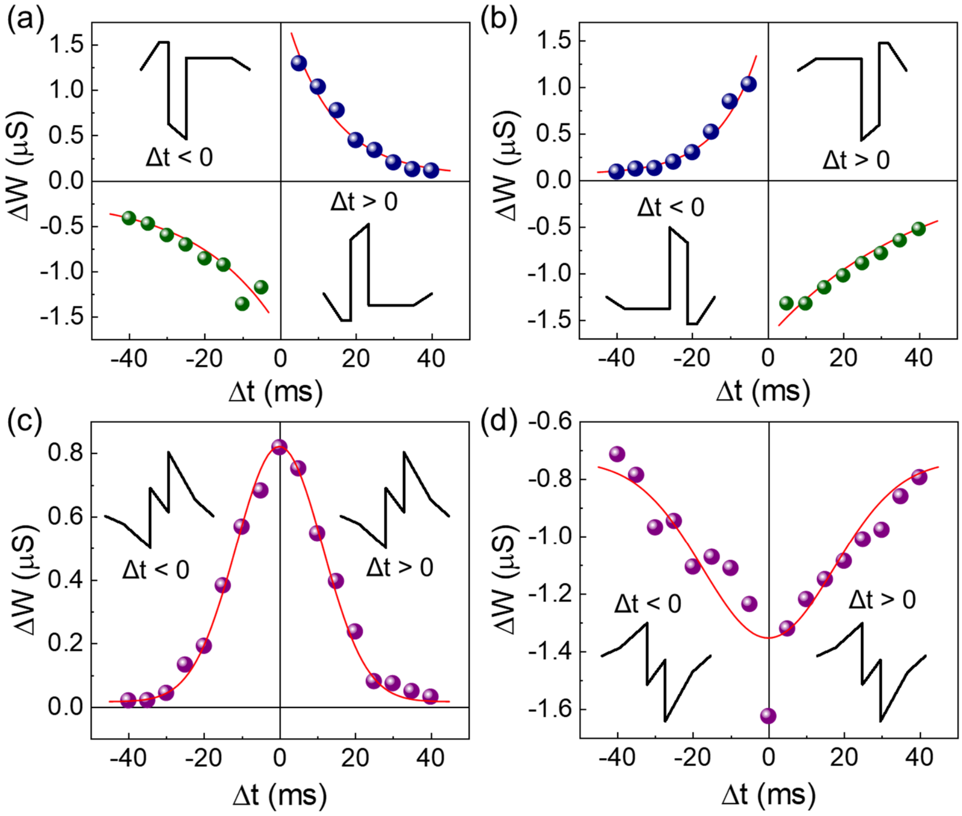

Figure 10. STDP characteristics of the Al/$LiNbO_3$/Pt memristive synapse (LN-250), demonstrating the versatile learning activities of (**a**) asymmetric Hebbian, (**b**) asymmetric anti-Hebbian, (**c**) symmetric Hebbian, and (**d**) symmetric anti-Hebbian rules. Each inset shows the spike pulse scheme used for performing each Hebbian rule.

Table 1. Comparison of materials and synaptic parameters for V_O-VCM-based memristive synapse.

Materials	Pulse Condition for LTP and LTD				Dynamic Range	Linearity (LTP/LTD)	Pattern Recognition Accuracy	Ref.
	Pulse Scheme	V_{LTP}/V_{LTD}	t_{LTP}/t_{LTD}	t_{inter}				
Pt/HfO_2/HfO_x/TiN	Identical	−0.8 V/2 V	1 µs/2 µs		~0.3~0.7 mA			[28]
TiN/Al:HfO_2/TiN	Identical	2.5 V/−2.4 V	100 µs		3~9 µS	22%/60%	94.5%	[29]
Au/TiO_2/Au	Identical	10 V/−10 V	50 ms	50 ms	~0.1~1 µA			[31]
ITO/TiO_x/TiO_y/TiN	Identical	1 V/−1 V	50 µs		~240~47 µA	0.89/0.69		[32]
W/WO_{3-x}/Pt	Identical	1.8 V/−1.8 V	400 µs		~28~32 mA	0.81		[34]
Pt/Ta_2O_5/HfO_2/TiN	Incremental	0.8~−1.2 V/1~1.2 V	10 µs		0~6 mS	27.03%/27.23%	69.88	[35]
Au/$LiNbO_3$/Pt	Identical	+15 V/−15 V	100 ms		~17~23 µA			[37]
Au/$LiNbO_3$/Pt	Identical	4 V/−4 V	40 ms	50 ms	~22~29 µA	1.2/2.7		[36]
This Work	Incremental	2~4.5 V/−0.5~3.5 V	300 µs/500 µs	10 ms	0~2 µA	0.16/0.32	95.2%	

4. Conclusions

The biological synaptic functions were effectively emulated using a memristive synapse, consisting of a top-to-bottom Al/$LiNbO_3$/Pt two-terminal device that operates based on the V_O-VCM mechanism. The device was fabricated by directly depositing a rhombohedral (113) $LiNbO_3$ active layer onto a cubic (111) Pt bottom electrode, followed by the formation of a lithographic Al top electrode. The presence of V_O enabled V_O-VCM-mediated SCLC in the $LiNbO_3$ active layer, resulting in rectified asymmetric hysteresis characteristics. Furthermore, the device successfully demonstrated a range of synaptic functions by manipulating multiple memory states through control of the magnitude of V_{pulse} and the width of t_{pulse}. It achieved an image pattern recognition accuracy of up to 95.2% in the MNIST simulation and exhibited versatile Hebbian learning behaviors in its STDP characteristics. These results highlight the potential of the V_O-VCM-based Al/$LiNbO_3$/Pt memristor for neuromorphic computing applications.

Supplementary Materials: The following supporting information can be downloaded at https://www.mdpi.com/article/10.3390/nano14231884/s1: Figure S1. (a) I–V characteristic curves of the Al/$LiNbO_3$/Pt memristive devices composed of the (a–c) LN-180, (d–f) LN-250, and (g–i) LN-320 layers. Figure S2. (a) Schottky plot, (b) Fowler–Nordheim plot, (c) SCLC plot, and (d) Poole–Flenkel plot at the negative bias voltage region for the LN-250 memristive synapse. Figure S3. Dependence of ΔPSC on tpulse performed at the LTP and LTD operations: (a) t_{pulse} = 200 µs for LTP, (b) t_{pulse} = 400 µs for LTP, (c) t_{pulse} = 600 µs for LTP, (d) t_{pulse} = 800 µs for LTP, (e) t_{pulse} = 1 ms for LTP, and (f) t_{pulse} = 1 ms for LTD. V_{pulse} were 4–4.5 V and −2–−3 for LTP and LPD, respectively. Figure S4. Applied pulse schemes for demonstrating the asymmetric Hebbian learning rule when (a) Δt = −5 ms, (b) Δt = −20 ms, (c) Δt = −40 ms, (d) Δt = +5 ms, (e) Δt = +20 ms, and (f) Δt = +40 ms. Figure S5. Applied pulse schemes for demonstrating the asymmetric anti-Hebbian learning rule when (a) Δt = −5 ms, (b) Δt = −20 ms, (c) Δt = −40 ms, (d) Δt = +5 ms, (e) Δt = +20 ms, and (f) Δt = +40 ms. Figure S6. Applied pulse schemes for demonstrating the symmetric Hebbian learning rule when (a) Δt = −5 ms, (b) Δt = −20 ms, (c) Δt = −40 ms, (d) Δt = +5 ms, (e) Δt = +20 ms, and (f) Δt = +40 ms. Figure S7. Applied pulse schemes for demonstrating the symmetric anti-Hebbian learning rule when (a) Δt = −5 ms, (b) Δt = −20 ms, (c) Δt = −40 ms, (d) Δt = +5 ms, (e) Δt = +20 ms, and (f) Δt = +40 ms.

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