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A Reconfigurable Polarimetric Photodetector Based on the $MoS_2/PdSe_2$ Heterostructure with a Charge-Trap Gate Stack

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Abstract: Besides the intensity and wavelength, the ability to analyze the optical polarization of detected light can provide a new degree of freedom for numerous applications, such as object recognition, biomedical applications, environmental monitoring, and remote sensing imaging. However, conventional filter-integrated polarimetric sensing systems require complex optical components and a complicated fabrication process, severely limiting their on-chip miniaturization and functionalities. Herein, the reconfigurable polarimetric photodetection with photovoltaic mode is developed based on a few-layer $MoS_2/PdSe_2$ heterostructure channel and a charge-trap structure composed of $Al_2O_3/HfO_2/Al_2O_3$ (AHA)-stacked dielectrics. Because of the remarkable charge-trapping ability of carriers in the AHA stack, the $MoS_2/PdSe_2$ channel exhibits a high program/erase current ratio of 10^5 and a memory window exceeding 20 V. Moreover, the photovoltaic mode of the $MoS_2/PdSe_2$ Schottky diode can be operated and manipulable, resulting in high and distinct responsivities in the visible broadband. Interestingly, the linear polarization of the device can be modulated under program/erase states, enabling the reconfigurable capability of linearly polarized photodetection. This study demonstrates a new prototype heterostructure-based photodetector with the capability of both tunable responsivity and linear polarization, demonstrating great potential application toward reconfigurable photosensing and polarization-resolved imaging applications.

Keywords: polarimetric photodetector; reconfiguration; two-dimensional heterostructure; charge-trap gate stack

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1. Introduction

The technology of polarization-sensitive photodetection plays a vital role in both civilian and military fields, such as biomedical imaging, quantum communication, and three-dimensional (3D) holographic displays [1–3]. In the past, conventional polarimetric photodetectors required the integration of a prepositive polarizer, lens, or polarization coding system, which increased the fabrication complexity and cost of the imaging systems [4]. Therefore, developing the architecture of polarizer-free polarimetric photodetection becomes crucial for satisfying the needs of on-chip integration, miniaturization, and multi-functionalities.

Recently, low symmetric two-dimensional (2D) semiconductors with in-plane anisotropic crystal structures have shown great potential for linear polarization photodetection. This capability arises from their intrinsic linear dichroism as well as the absence of surface dangling bonds, which allows for integration into complex heterostructures regardless of lattice mismatch [5–8]. Among 2D materials and their heterojunctions, including black phosphorous [9], ReS_2 [10], GeAs [11], 1T′-$MoTe_2$ [12], 1T′-WTe_2 [13], as well as WSe2/$ReSe_2$ [14], WS_2/GeAs [15], and graphene/$PdSe_2$/Ge [2], they have been widely used to build polarization-sensitive photodetectors with high detectivity, fast speed, and broad-band sensitivity.

Some previous architectures of the device have been proposed; however, the existing technologies have still been unable to realize multifunctional photodetection with tunable responsivity and polarization sensitivity. The capability for reconfigurable polarimetric photodetection could enable higher-resolution polarimetric imaging. To achieve tunable responsivity and polarization sensitivity, configurations such as a split-gate configuration [16] or ferroelectric polarization [17] have been employed. However, these approaches suffer from the complicated design of four electrical terminals and the high energy consumption required. At the same time, nonvolatile polarimetric photodetection, in which the reconfigurable responsivity and polarization sensitivity are necessary schemes for the integration of multi-functional modules, realizes an "All-in-one" system, such as in-memory sensing technology [18], vision acquisition [19], and high-level cognitive computing [20]. However, the tunable nonvolatile and reconfigurable polarimetric photodetection in 2D devices still remains rarely studied.

This work demonstrates a novel multifunctional photodetector engineered to offer reconfiguration in both responsivity and polarization sensitivity. It is developed on a few-layer MoS_2/$PdSe_2$ heterostructure and an Al_2O_3/HfO_2/Al_2O_3 (AHA) charge-trap gate stack. Our elaborately designed photodetector exhibits a remarkable photovoltaic photodetection performance under visible illumination, which can be attributed to the built-in electrical driving effect of the MoS_2/$PdSe_2$-based Schottky diode. Under modulation of the AHA charge-trap gate stack, the electrical characteristics of the MoS_2/$PdSe_2$ Schottky diode can be tuned and maintained at the program/erase state, exhibiting an unprecedented memory window exceeding 20 V and the program/erase current ratio of 10^5. Moreover, the photovoltaic mode of the MoS_2/$PdSe_2$ Schottky diode is operated and switchable, resulting in high and distinct responsivities in the visible spectral band. Interestingly, linear polarization can be further modulated under the program/erase state, enabling the reconfigurable capability of linearly polarized photodetection. Our work provides promising solutions for increasing the versatility of applications for reconfigurable photodetection. Importantly, the charge-trap gate stack was first applied on the 2D heterostructure to engineer the band alignment type, enhance the photodetection performance, and enrich functionalities.

2. Materials and Methods

MoS_2 is one of the most studied 2D materials, and it demonstrates the ability to have remarkable electronic and optoelectronic properties, which makes it a great potential photodetector candidate. Considering the large carrier density and high work function of $PdSe_2$, a depletion region of the junction can be formed by stacking the MoS_2/$PdSe_2$ heterostructure. Multilayers of MoS_2 and $PdSe_2$ were subsequently exfoliated and stacked together (Figure 1a). The details of device fabrication are provided in Section S1 of Supplementary Materials. The schematic of the MoS_2/$PdSe_2$ photodetector is shown in Figure 1b. Figure 1c shows the distinct Raman peaks of the MoS_2/$PdSe_2$ heterostructure, which correspond to 382 cm^{-1} (E^1_{2g}) and 407 cm^{-1} (A_{1g}) for MoS_2 and 144 cm^{-1} (A^1_g), 203 cm^{-1} (A^2_g), 222 cm^{-1} (B^2_{1g}), and 258 cm^{-1} (A^3_g) for $PdSe_2$. Figure 1d and e show the I_{ds}–V_{ds} curves under different gate voltages V_G for MoS_2 and $PdSe_2$ field-effect transistor (FET), respectively. Notably, both I_{ds}–V_{ds} curves demonstrate obvious linearity, and it can be proved to be Ohmic source-drain contact for both FETs, which is necessary for optoelectronic characteristics of the MoS_2/$PdSe_2$ photodetector. Furthermore, the output curves

of I_{ds}–V_{ds} for MoS_2 FET exhibit a n-type ambipolar conducting behavior at V_G from −5 to 5 V. By contrast, the current slightly increases with decreasing negative V_G for $PdSe_2$ FET, which indicates the semi-metallic behavior. Given the bandgaps of multilayer MoS_2 and $PdSe_2$ are previously reported to be 1.2 and 0.03 eV [21,22], the band alignment of the MoS_2/$PdSe_2$ heterojunction is illustrated in Figure 1f. The Schottky barrier can be formed at the interface of the MoS_2/$PdSe_2$ heterojunction, and the I_{ds}–V_{ds} curve exhibits a rectification behavior, demonstrating a rectification ratio of I_{on}/I_{off} up to 10.

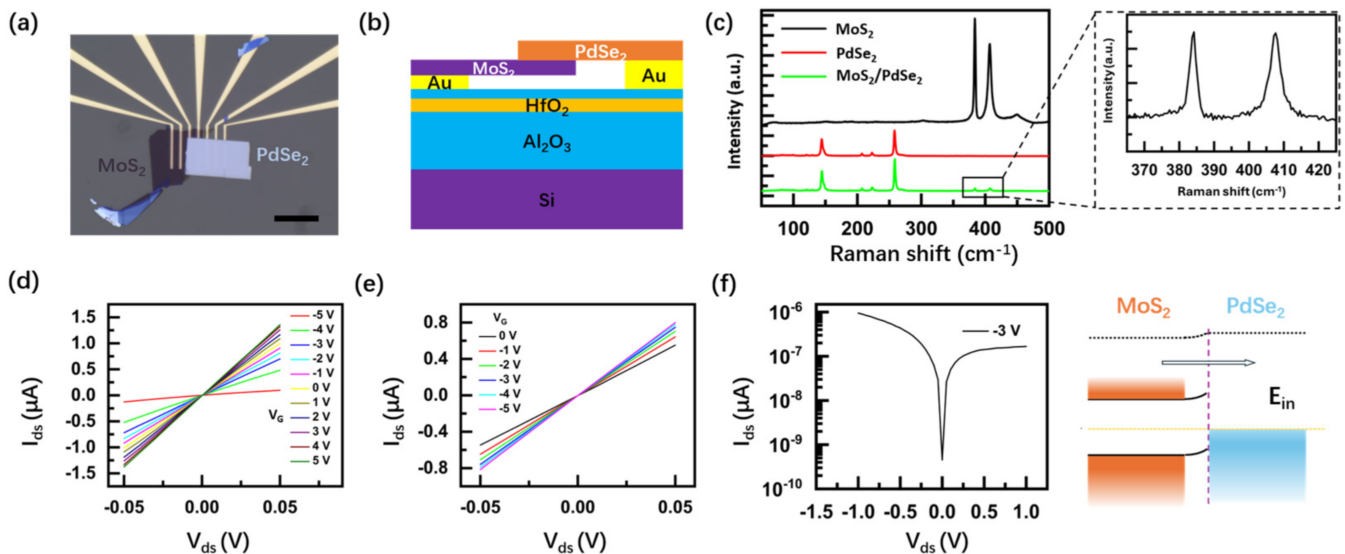

Figure 1. Schematics and characterization of the MoS_2/$PdSe_2$ heterostructure device: (**a**,**b**) Schematic and picture of MoS_2/$PdSe_2$ heterostructure photodetector. The scale bar is 20 μm; (**c**) Raman spectra of the multilayer MoS_2 flakes, $PdSe_2$ flakes, and heterostructure, respectively; (**d**,**e**) I_{ds}–V_{ds} relationship of MoS_2 and $PdSe_2$, respectively; (**f**) the transfer characteristics of the MoS_2/$PdSe_2$ heterostructure under the bias of −3 V and schematic of the MoS_2/$PdSe_2$ heterostructure-based Schottky barrier.

3. Results

3.1. Transfer Characteristics and Static Memory Behavior

A charge-trap stack of Al_2O_3/HfO_2/Al_2O_3 (6 nm/8 nm/32 nm) was deposited via atomic layer deposition (ALD). Figure 2a shows the transfer curves of the MoS_2/$PdSe_2$ Schottky diode. The transfer curves were acquired by sweeping the gate voltage V_G in a closed loop (from negative to positive values) under a fixed V_{ds} of −1 V, exhibiting a clear hysteresis window, and the hysteresis enables widening as the V_G sweep range increases from 5 to 25 V. The I_{ds}–V_G curves exhibit a clockwise memory window. The extraction of memory window ΔV increases almost linearly with the maximum V_G and reaches a maximum of 20 V when the V_G sweeps to 25 V (Figure 2b). The transfer curve of I_{ds}–V_G decreases with increasing negative V_G, suggesting that n-type MoS_2 dominates the transfer characteristics of the device. Figure 2c illuminates the device operation process. When a high positive/negative V_G was applied to the gate, the band alignment started favoring the tunneling in/out of electrons from the MoS_2/$PdSe_2$ channel to the HfO_2 charge-trap layer, which resulted in the change of carrier concentration in MoS_2 and a switch between program and erase state, respectively.

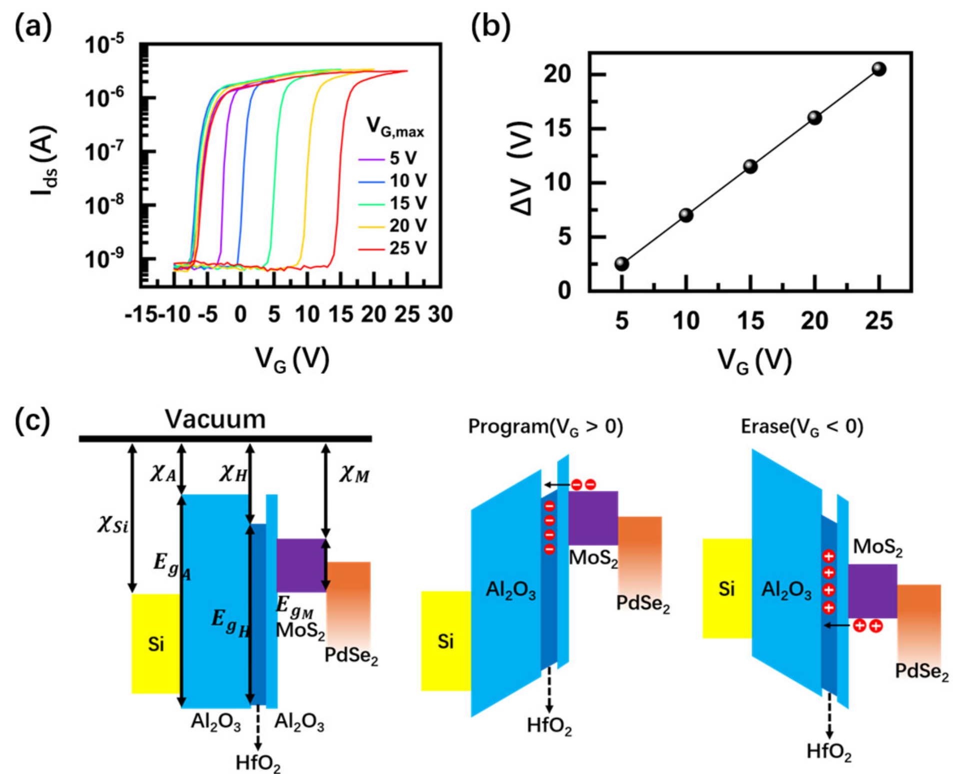

Figure 2. The statical behavior of the nonvolatile gate charge-trap memory based on $MoS_2/PdSe_2$ heterostructure: (**a**) I_{ds}–V_G characteristics of the device under different V_G at $V_{ds} = -1$ V; (**b**) extraction of memory window ΔV vs. V_G. The memory window increases from 1 to ∼20 V in our experimental settings; (**c**) band diagram of the program/erase state of the device under positive and negative V_G. Positive V_G programs the device. Electrons tunneling from the few-layer MoS_2 channel are accumulated in the HfO_2 charge-trap layer. Negative V_G erases the device. Holes tunnel from the few-layer MoS_2 channel to the HfO_2 charge-trap layer.

3.2. Dynamic Memory Behavior of the Device

The transfer characteristics of the device are further studied under different biases. As shown in Figure 3a,b, they show that an obvious memory window occurs under both a forward bias of −1 V and a reverse bias of +1 V. A maximum program/erase current ratio of 10^5 can be achieved under a forward bias of −1 V. Endurance and retention time of the $MoS_2/PdSe_2$ memory are provided in Section S4 of Supplementary Materials. To explore the dynamic transition of the device, the device was initially set into an erase state by applying a negative gate pulse (−10 V, duration of 2 s). The output curves I_{ds}–V_{ds} were read by sweeping V_{ds} from −1 V to +1 V after applying a series of +25 V gate pulses with different duration times. The output curve I_{ds}–V_{ds} shows a clear decrease and is nearly saturated when the width of the pulse increases to 0.2 s (Figure 3c). According to the expression of the charge-trapping rate [23], the calculated charge-trapping rate varies from 10^{15} $cm^{-2}s^{-1}$ to 10^{14} $cm^{-2}s^{-1}$ when the pulse width changes from 0.01 s to 0.2 s. Figure 3d shows the dependency of output curves I_{ds}–V_{ds} with the amplitude of the gate pulse. It demonstrates that output current decreases with the increase of pulse amplitude. This can be explained by the modulation of the Schottky barrier through the gate pulse, which also suggests that the charge-trapping mechanism of the AHA gate stack dominates the memory behavior of the device.

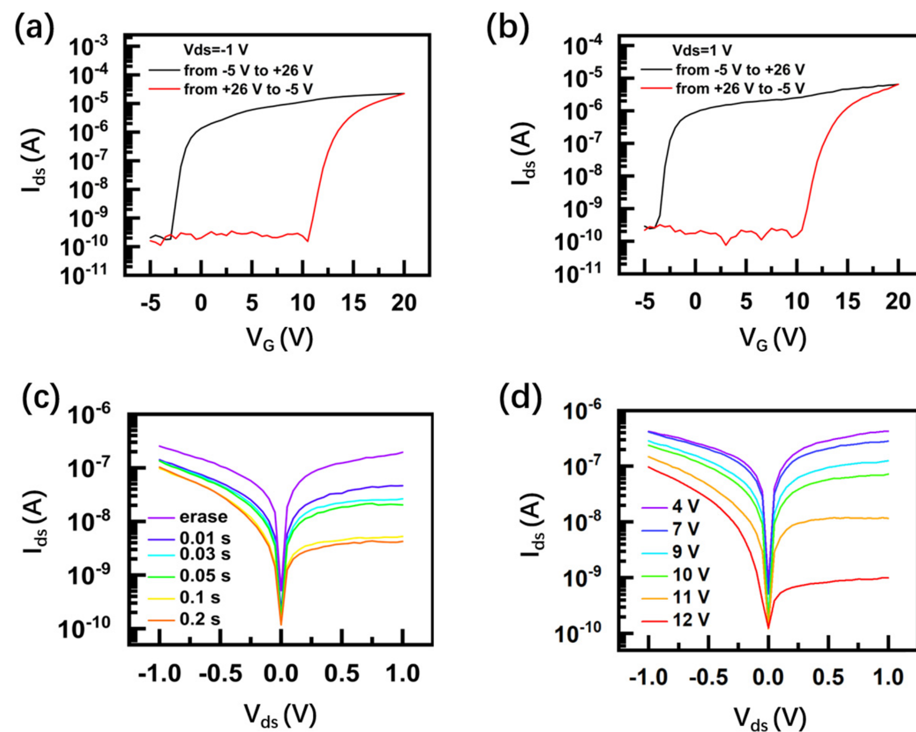

Figure 3. The dynamic behavior of the nonvolatile gate charge-trap memory based on $MoS_2/PdSe_2$ heterostructure: (**a**,**b**) I_{ds}–V_G characteristics of the device under different V_G under the forward bias of −1 V and reverse bias of +1 V, respectively; (**c**,**d**) I_{ds}–V_{ds} characteristics of the device under different pulse durations and amplitudes.

3.3. Photovoltaic Behavior and Reconfigurable Linear Polarization

Given the excellent memory switching properties of the device (including unprecedented memory window, large program/erase current ratio, and nonvolatile switchable Schottky barriers) and strong optical anisotropy of $PdSe_2$, the polarization-modulated photovoltaic behavior in the $MoS_2/PdSe_2$-based photodetector was worthy of investigation. To characterize it, a positive (+25 V) and negative (−10 V) gate pulse with a width of 0.2 s were applied to switch the device into the program and erase state, respectively. In the program/erase state, I_{ds}–V_{ds} characteristics under illumination were recorded by using the polarized 520 nm light with an intensity of 120 mW/cm^2. Figure 4a,b show the I_{ds}–V_{ds} characteristics of the device under parallel (0°) and vertical (90°) polarized light in the program and erase state, respectively (0° and 90° directions correspond to the b-axis and a-axis crystalline direction of $PdSe_2$). The crystalline orientation of $PdSe_2$ was determined by angle-resolved polarized Raman spectroscopy (ARPRS), and details of the measurement are provided in Section S3 of Supplementary Materials. It can be noticed that the device exhibits noticeable photovoltaic responses, including a short-circuit current (I_{sc}) of ~15 nA/30 nA and an open-circuit voltage (V_{oc}) of ~−0.014 V/−0.012 V in the program/erase state under parallel light excitation. After switching the polarization of light to the vertical direction, the illuminated I_{ds}–V_{ds} curves shift toward the higher value, showing that I_{sc} and V_{oc} increase to ~54 nA/82 nA and ~−0.027/−0.025 V in the program/erase state. It is noted that significant photocurrent noise occurs during photocurrent measurement, which can be attributed to the degeneration of 2D flakes and environmental noise. The protection layer of Al_2O_3 on top of the $MoS_2/PdSe_2$ heterostructure and the optimized measurement method can significantly reduce the noise, which is summarized in Section S5 of Supplementary Materials. In addition, gate voltage was applied to modulate the performance of the device. The responsivity was extracted and plotted in Figure 4c at different memory states and polarization of light. The noise equivalent power (NEP) and detectivity of this photodetector were measured and are provided in Section S6 of

Supplementary Materials. The device shows typical transfer characteristics of an n-type MoS_2 semiconductor. As the gate voltage increases from −2 V to 2 V, all of the responsivities increase at V_{ds} = −1 V. A figure of merit of the linear polarized photodetection is the degree of linear polarization (LP), where LP = $(I_{max} - I_{min})/(I_{max} + I_{min})$, where I_{max} and I_{min} are the photocurrents of the detected light parallel and perpendicular to the primary polarization direction, respectively. Figure 4d shows the LP results as a function of V_G. Under 120 mW/cm^2 light illumination, both LP values of the device gradually increase from 0.4/0.36 to 0.55/0.49 in the program/erase state. This indicates that the LP of the device can be effectively modulated by the memory state, and its gap between the program and erase state becomes more obvious under the positive gate voltage.

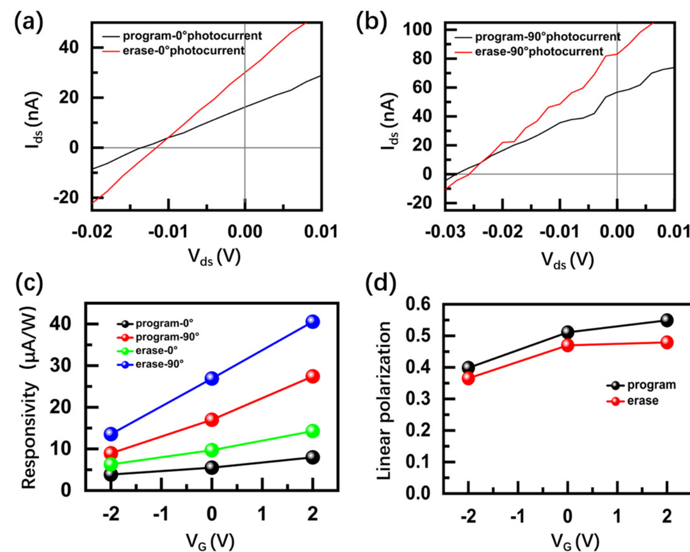

Figure 4. The polarization-modulated photovoltaic behavior of $MoS_2/PdSe_2$ photodetector: (**a**,**b**) Short-circuit current I_{sc} and open-circuit voltage V_{oc} of $MoS_2/PdSe_2$ photodetector under the program and erase state, respectively. (**c**,**d**) Dependency of responsibility and linear polarization with gate voltage V_G under different program/erase states and polarization directions of light.

4. Discussion

To understand the photoresponse mechanism of the $MoS_2/PdSe_2$ device, the energy band structure diagram is illustrated in Figure 5. Since the fermi level of $PdSe_2$ is lower than MoS_2, the electrons will flow from MoS_2 to $PdSe_2$, and the holes diffuse in opposite directions to MoS_2. The opposite diffusion of electrons and holes introduces a Schottky barrier with the build-in field $\mathbf{E_{in}}$ pointing from MoS_2 to $PdSe_2$, which is described in Figure 1f. When the laser shines on the surface of the device, the electrons confined in the valence band will be excited by the conduction bands in both materials. Then, with the help of build-in field $\mathbf{E_{in}}$, the electrons occupied in $PdSe_2$ can be driven to the conduction band of MoS_2, while $\mathbf{E_{in}}$ will force the holes within the MoS_2 valence band to flow into the valence band of $PdSe_2$, resulting in the photovoltaic behavior. When the negative gate voltage pulse is applied to switch the device into an erase state (Figure 5b), the energy band of MoS_2 is lowered, and $\mathbf{E_{in}}$ will increase, which results in the enhancement of separation of photo-generated electron-hole pairs as well as short-circuit current. Meanwhile, the photocurrent generated from MoS_2 increases in the erase state, which results in the decrease of LP because of the intrinsic polarization-insensitivity of MoS_2. On the other hand, the $\mathbf{E_{in}}$ will be reduced in the program state (Figure 5c), which induces the decrease of short-circuit current and increase of LP. In this way, we can adjust the energy band structure of $MoS_2/PdSe_2$ by switching the program/erase state, thereby adjusting the photodetection performance of the device.

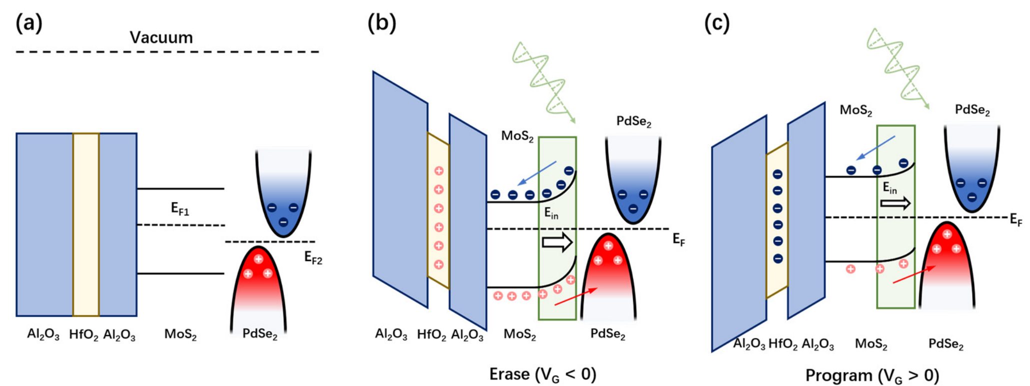

Figure 5. Photoresponse mechanism of reconfigurable $MoS_2/PdSe_2$ photodetector: (**a**) The energy band structure of AHA charge-trap stack and $MoS_2/PdSe_2$ heterostructure before contact; (**b**,**c**) the energy band structure of the device and the flow of photo-generated electron-holes under illumination when the device is set to erase ($V_G < 0$) and program states ($V_G > 0$), respectively.

5. Conclusions

In summary, a multifunctional photovoltaic photodetector was demonstrated, which was composed of in-plane anisotropic $PdSe_2$ and MoS_2 with an AHA charge-trap gate stack. The device exhibits a nonvolatile phenomenon in both electrical and photovoltaic characteristics, resulting from the modulation of band alignment by the gate voltage pulse. Utilizing the AHA charge-trap gate stack, the memory window and program/erase current ratio of $MoS_2/PdSe_2$ can be effectively modulated. Acting as a reconfigurable polarimetric photodetector, the device exhibits a reversible performance of both responsivity and polarization-sensitive photocurrent by switching the program and erase state, rendering it a promising candidate for polarization signal recognition and imaging.

Supplementary Materials: The following supporting information can be downloaded at https://www.mdpi.com/article/10.3390/nano14231936/s1: Figure S1. Thickness of (a) MoS_2 and (b) $PdSe_2$ measured by atomic force microscopy. Figure S2. Angle-resolved polarized Raman spectroscopy of a PdSe2 flake. Figure S3. Endurance of the $MoS_2/PdSe_2$ memory. (a) Endurance of the memory device for 100 cycles with the program/erase voltage being +20 V, 1 s and −10 V, 1 s. (b) The stability of the program/erase state of the device after programming at +20 V, 1 s duration, and erasing at −10 V, 1 s duration (Vds = −1 V). Figure S4. The polarization-modulated photovoltaic behavior of the MoS2/PdSe2 photodetector.: (a) and (b) Short-circuit current Isc and open-circuit voltage Voc of the MoS2/PdSe2 photodetector under the program and erase state, respectively. Figure S5. The NEP and detection limit of the MoS2/PdSe2 photodetector. (a) NEP and (b) detectivity tuned by the gate voltage, indicating the detection limit of our photodetector.

Author Contributions: C.G. and X.H. conceived the research, and Q.B. and T.L. fabricated the samples. Q.B. conducted the measurements. X.H., Q.B., Y.G., Q.L., T.L., W.L., A.J., B.Q., H.Y., B.L. and C.G. discussed the data and contributed to the manuscript. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

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