

# High- $\kappa$ oxide nanoribbons as gate dielectrics for high mobility top-gated graphene transistors

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**Deposition of high- $\kappa$  dielectrics onto graphene is of significant challenge due to the difficulties of nucleating high quality oxide on pristine graphene without introducing defects into the monolayer of carbon lattice. Previous efforts to deposit high- $\kappa$  dielectrics on graphene often resulted in significant degradation in carrier mobility. Here we report an entirely new strategy to integrate high quality high- $\kappa$  dielectrics with graphene by first synthesizing free-standing high- $\kappa$  oxide nanoribbons at high temperature and then transferring them onto graphene at room temperature. We show that single crystalline Al<sub>2</sub>O<sub>3</sub> nanoribbons can be synthesized with excellent dielectric properties. Using such nanoribbons as the gate dielectrics, we have demonstrated top-gated graphene transistors with the highest carrier mobility (up to 23,600 cm<sup>2</sup>/V · s) reported to date, and a more than 10-fold increase in transconductance compared to the back-gated devices. This method opens a new avenue to integrate high- $\kappa$  dielectrics on graphene with the preservation of the pristine nature of graphene and high carrier mobility, representing an important step forward to high-performance graphene electronics.**

graphene dielectric integration | carrier mobility | dielectric nanoribbon | nanoelectronics

Graphene has attracted considerable interest as a potential electronic material due to its exceptionally high carrier mobility and tunable band gap (1–6). Various strategies have been explored to fabricate field-effect transistors based on graphene or graphene nanostructures (6–13). Most of these efforts to date employ a silicon substrate as a global back gate and silicon oxide as the gate dielectric, which have led to many interesting scientific discoveries, but will be of limited use for practical applications due to the high-gate switching voltage required and the inability to independently address individual devices on the same chip. Top-gated devices with high- $\kappa$  dielectrics can significantly reduce the required switching voltage and readily allow independently addressable device arrays and functional circuits, and therefore are of significant interest (14, 15).

The gate dielectric is an essential component of a transistor, which can significantly impact the critical device parameters including transconductance, subthreshold swing and frequency response. Exploring graphene for future electronics requires effective integration of high quality gate dielectrics, in particular the high- $\kappa$  dielectrics. However, it has been rather challenging to deposit oxide dielectrics onto graphene without introducing defects. The deposition of high- $\kappa$  dielectrics is usually achieved using atomic layer deposition (ALD), which requires reactive surface groups (16–20). Functionalization of graphene surface for ALD either introduces undesired impurities or breaks the chemical bonds in the graphene lattice, inevitably leading to a significant degradation in carrier mobilities (20). Physical vapor deposition (PVD) such as electron-beam evaporation or sputtering process has also been used to deposit dielectrics without the need of surface functionalization. Although the PVD process usually yields lower quality dielectrics and can also cause significant damages to graphene (21, 22). As a result, the mobility values observed in the top-gated devices are typically nearly

one order of magnitude smaller than what can be achieved in the back-gated devices (20–23). Recently, the introducing of polymer or aluminum buffer layer for high- $\kappa$  deposition was demonstrated with improved the device mobility (24, 25), which is still lower than that of the best back-gated graphene devices (1, 4, 5). To eventually realize high-performance graphene-based electronics, alternative approaches must be developed to deposit high quality high- $\kappa$  dielectrics without damaging the pristine graphene.

Here we describe an entirely unique strategy to integrate graphene with high quality high- $\kappa$  dielectrics using free-standing dielectric nanoribbons. Nanoribbons can be synthesized at high temperature with nearly perfect crystalline structure, but manipulated and assembled at room temperature. This flexibility allows the integration of normally incompatible materials and processes and can enable unique functions in electronics or photonics (26–30). In this report, the dielectric properties of aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) nanoribbons are explored for graphene-based electronics. Specifically, high quality dielectric Al<sub>2</sub>O<sub>3</sub> nanoribbons were first synthesized, and then transferred onto graphene as the gate dielectrics for top-gated graphene transistors. This integration approach preserves the pristine nature of the graphene and allows us to achieve the highest room temperature carrier mobility (up to 23,600 cm<sup>2</sup>/V · s) in top-gated graphene transistors to date.

## Results and Discussion

Fig. 1 illustrates our approach to fabricate top-gated graphene transistors. Mechanically peeled graphene flakes on silicon substrate were used as the starting materials in initial studies, although the approach described here can be readily extended to graphene obtained through chemical exfoliation or chemical vapour deposition. Al<sub>2</sub>O<sub>3</sub> nanoribbons were aligned on top of the graphene through a physical dry transfer process (*Materials and Methods*), followed by e-beam lithography and metallization process to define the source and drain electrodes (Fig. 1A). Oxygen plasma etch was then used to remove the exposed graphene, leaving only the graphene protected underneath the dielectric nanoribbon and the source drain electrodes (Fig. 1B). The top-gate electrode was then fabricated (Fig. 1C). A typical device consists of source, drain and top-gate electrodes (Ti/Au, 50 nm/50 nm), Al<sub>2</sub>O<sub>3</sub> nanoribbon as the top-gate dielectric, a highly doped p-type silicon substrate (<0.004 ohm · cm) as the back gate, and a 300 nm thermal silicon oxide layer as the back-gate dielectric.

Aluminum oxide, with a dielectric constant of 9.1, is an important high- $\kappa$  material with excellent dielectric properties, thermal

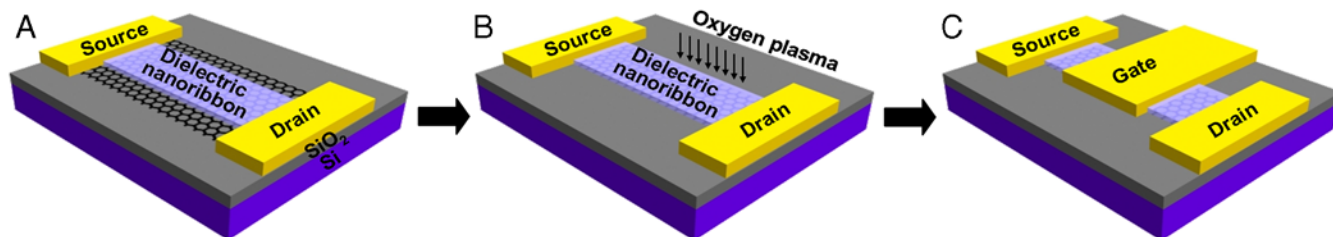
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**Fig. 1.** Schematic illustration of the fabrication process to obtain top-gated graphene transistors using dielectric oxide nanoribbons as the etching mask and top-gate dielectric. (A) A dielectric nanoribbon is aligned on top of graphene using a dry-transfer process without any additional chemical functionalization to minimize the possibility of introducing defects/impurities into the graphene-dielectric interface, and the source-drain electrodes are fabricated by electron-beam lithography. (B) Oxygen plasma etch is used to remove the unprotected graphene, leaving only the graphene underneath the dielectric nanoribbon connected to two large graphene blocks underneath the source and drain electrodes. (C) The top-gate electrode is defined through lithography and metallization process.

and chemical stability (30). In our studies,  $\text{Al}_2\text{O}_3$  nanoribbons were used as an example to demonstrate our concept of using preformed free-standing nanoribbons as the top-gate dielectrics.  $\text{Al}_2\text{O}_3$  nanoribbons were synthesized through a physical vapor transport approach at  $1400^\circ\text{C}$  (*Materials and Methods*). Transmission electron microscope (TEM) studies show that the  $\text{Al}_2\text{O}_3$  nanoribbons typically have a width of  $1\text{--}3\ \mu\text{m}$ , and a length on the order of  $10\ \mu\text{m}$  (Fig. 2A). Selected area electron

diffraction (SAED) study shows the nanoribbon has a single crystalline  $\alpha\text{-Al}_2\text{O}_3$  structure, oriented along  $\langle 110 \rangle$  direction in its long axis, and along  $\langle 001 \rangle$  direction (c-plane) in its thickness (Fig. 2A and *Inset*). The high resolution TEM (HRTEM) image confirms that the nanoribbon is a single crystal with nearly perfect crystalline structure free of any obvious defects (Fig. 2B). Atomic force microscopy (AFM) studies show that the nanoribbons typically have a thickness around  $15\text{--}150\ \text{nm}$  (Fig. 2C), and nearly atomically smooth surface with root mean square roughness  $<0.2\ \text{nm}$  (Fig. 2D).

To understand the intrinsic dielectric properties of the nanoribbons, we have fabricated metal-insulator-metal (MIM) devices (Fig. 2E) to characterize the current tunnelling, breakdown, and dielectric characteristics. Electrical measurements of the MIM device show that current density ( $J$ ) vs. electric field ( $E$ ) relation exhibits typical Fowler–Nordheim (F–N) tunnelling behavior with a breakdown field of  $8.5\ \text{MV/cm}$  (Fig. 2F and *Inset*), comparable to the best quality ALD  $\text{Al}_2\text{O}_3$  film (31). This type of field-assisted tunnelling can be described by charge carrier tunnelling through a triangular barrier with

$$J = AE_{\text{OX}}^2 \exp(-B/E_{\text{OX}}) \quad [1]$$

where

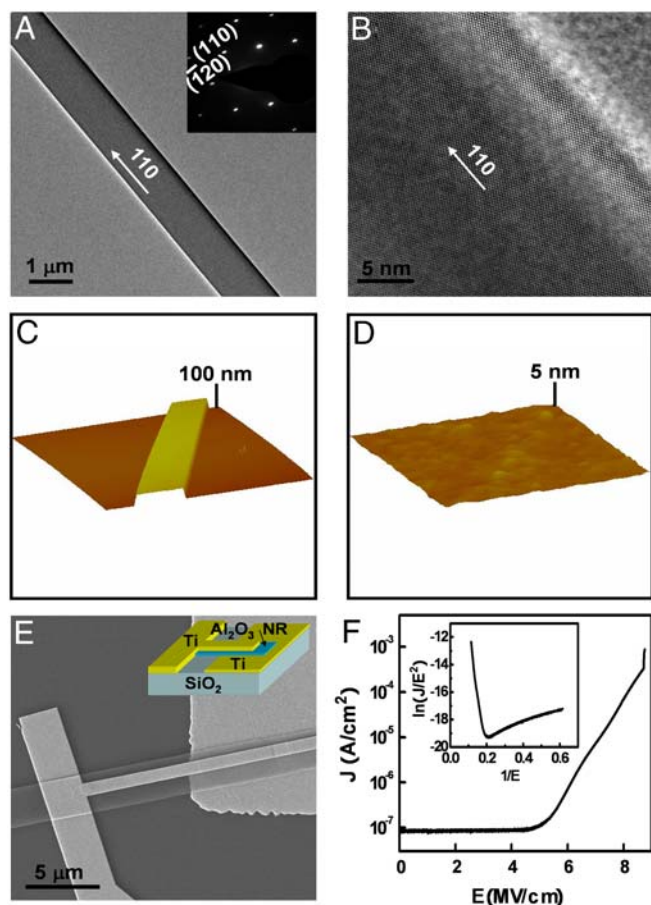
$$A = 1.54 \times 10^{-6} \left\{ \frac{1}{m^* \Phi_B} \right\}, \quad [2]$$

and

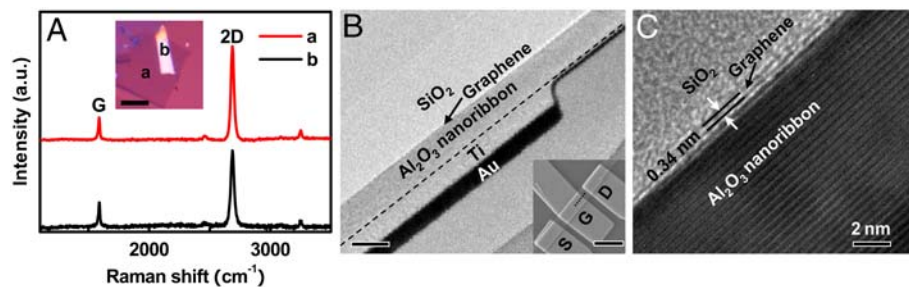
$$B = 6.83 \times 10^7 (m^*)^{1/2} (\Phi_B)^{3/2}. \quad [3]$$

$J$  is current density,  $E_{\text{OX}}$  is the oxide electric field, and  $m^*$  is the effective mass of the charge carrier, which is about  $0.23\ m_e$ , and  $\Phi_B$  is the barrier height (31). Fitting the  $J - E$  characteristics with the F–N tunnelling model gives a tunnel barrier of about  $2.0\ \text{eV}$  between  $\text{Al}_2\text{O}_3$  and Ti, comparable to previous reports of the barrier height between ALD  $\text{Al}_2\text{O}_3$  and metals of similar work function (31, 32). The relative dielectric constant is also determined from capacitance-voltage measurement as  $8.5$ , which is larger than typical values observed in ALD  $\text{Al}_2\text{O}_3$  films (31). These studies clearly demonstrate that the  $\text{Al}_2\text{O}_3$  nanoribbons have dielectric properties comparable to or better than the best quality ALD  $\text{Al}_2\text{O}_3$  film (31), and can function as an excellent dielectric material for top-gated graphene transistors.

The  $\text{Al}_2\text{O}_3$  nanoribbons can be aligned onto the top of the graphene through a physical transfer process (*Materials and Methods*). Previous studies have shown that the deposition of oxide on top of graphene often introduces significant defects into the graphene structure with an obvious defect band (D-band) emerging around  $1350\ \text{cm}^{-1}$  in Raman spectra. To this end, we have employed micro-Raman spectroscopy to investigate the interaction between an  $\text{Al}_2\text{O}_3$  nanoribbon and the underlying graphene (Fig. 3A and *Inset*). Micro-Raman spectra were



**Fig. 2.** Evaluation of the  $\text{Al}_2\text{O}_3$  nanoribbons as dielectric material. (A) TEM image (SAED pattern, *Inset*) and (B) HRTEM image of an  $\text{Al}_2\text{O}_3$  nanoribbon show nearly perfect crystalline structure with  $\alpha\text{-Al}_2\text{O}_3$  structure. (C) AFM image of an  $\text{Al}_2\text{O}_3$  nanoribbon with thickness approximately  $50\ \text{nm}$ . The image area is  $5\ \mu\text{m} \times 5\ \mu\text{m}$ . (D) AFM image of the surface of the  $\text{Al}_2\text{O}_3$  nanoribbon, highlighting the smooth surface with a rms roughness  $<0.2\ \text{nm}$ . The image area is  $250\ \text{nm} \times 250\ \text{nm}$ . (E) The schematic device diagram (*Inset*) and SEM image of an  $\text{Al}_2\text{O}_3$  nanoribbon metal-insulator-metal (MIM) device. (F) Current density-electric field ( $J$ - $E$ ) curve of an MIM device made from an  $\text{Al}_2\text{O}_3$  nanoribbon, and the inset shows the corresponding (F–N) curve.



**Fig. 3.** Characterization of the graphene/ $\text{Al}_2\text{O}_3$  nanoribbon interface. (A) Raman spectra of the graphene with (Point *b*) and without (Point *a*)  $\text{Al}_2\text{O}_3$  nanoribbon covering. The inset shows the optical image of an  $\text{Al}_2\text{O}_3$  nanoribbon on graphene, the scale bar is 2  $\mu\text{m}$ . There is no D-band in either spectrum, indicating that  $\text{Al}_2\text{O}_3$  nanoribbon does not introduce any appreciable defects into graphene lattice. (B) A cross-section TEM image of the top-gate stack, the scale bar is 100 nm. The inset shows an SEM image of a typical device, the scale bar indicates 5  $\mu\text{m}$ . The dotted line in the inset shows the cross-section cutting direction. (C) A cross-section HRTEM image of the interface between  $\text{Al}_2\text{O}_3$  nanoribbon and a trilayer graphene. The partially incomplete graphene layers in the image are caused by electron-beam damage during the TEM imaging process.

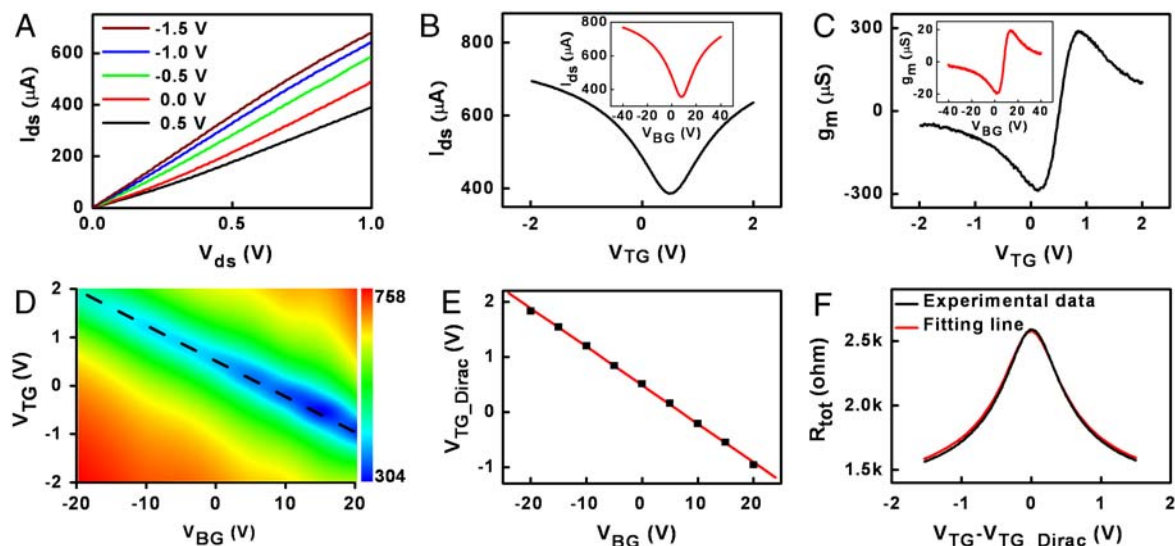
collected from bare graphene (Point *a*) and  $\text{Al}_2\text{O}_3$  nanoribbon covered graphene (Point *b*). Significantly, there is no clear difference between two Raman spectra and there is no obvious D-band (Fig. 3A), in contrast to previous studies where an obvious D-band is observed (33).

The excellent dielectric properties observed in the single crystalline  $\alpha\text{-Al}_2\text{O}_3$  nanoribbons readily allows us to employ them as the gate dielectrics for top-gated graphene transistors (Fig. 3B and Inset). Cross-section TEM was used to study the graphene–dielectric interface (Fig. 3B and C). The gate stack ( $\text{SiO}_2/\text{graphene}/\text{Al}_2\text{O}_3/\text{Ti}/\text{Au}$ ) could be observed in Fig. 3B. The HRTEM image of the device shows that the graphene layers are intimately integrated with the crystalline  $\text{Al}_2\text{O}_3$  nanoribbon without any obvious gap or impurities between them (Fig. 3C). Together, these studies clearly demonstrate that the physical assembly approach can effectively integrate  $\text{Al}_2\text{O}_3$  nanoribbon with graphene without introducing any appreciable defects into the graphene lattice, and thus can effectively preserve the high carrier mobility in the resulting devices.

The electrical transport studies of the top-gated graphene transistors were carried out at room temperature. Fig. 4A shows the drain-source current ( $I_{\text{ds}}$ ) versus drain-source voltage ( $V_{\text{ds}}$ ) output characteristics of the transistor at various top-gate voltage

( $V_{\text{TG}}$ ) of  $-1.5$ ,  $-1.0$ ,  $-0.5$ ,  $0.0$ , and  $0.5$  V. The device delivers an on current of  $675 \mu\text{A}$  at  $V_{\text{ds}} = 1$  V and  $V_{\text{g}} = -1.5$  V. To evaluate the top-gated devices versus standard back-gated devices, we have measured the transfer characteristics,  $I_{\text{ds}}$  versus top-gated voltage ( $V_{\text{TG}}$ ) and back-gated voltage ( $V_{\text{BG}}$ ) (Fig. 4B and Inset). Significantly, the required gate voltage swing to achieve similar current modulation in top-gate configuration is  $>1$  order of magnitude smaller than that in back-gate configuration. The transconductance  $g_m = \frac{dI_{\text{ds}}}{dV_{\text{TG}}}$  can be extracted from the  $I_{\text{ds}}-V_{\text{TG}}$  curve (Fig. 4C). At  $V_{\text{ds}} = 1$  V, the top-gated device exhibits a max  $g_m$  of about  $290 \mu\text{S}$ , which is about 15 times larger than that of the back-gated configuration ( $g_m \sim 19.5 \mu\text{S}$ ).

Fig. 4D further shows two-dimensional plot of the device conductance as a function of varying  $V_{\text{BG}}$  and  $V_{\text{TG}}$  bias, from which we can determine the top-gate Dirac point ( $V_{\text{TG\_Dirac}}$ ) shift as a function of  $V_{\text{BG}}$  (Fig. 4E). It gives the ratio between top-gate and back-gate capacitances,  $C_{\text{TG}}/C_{\text{BG}} \approx 14.3$ . This gate capacitance ratio is consistent with the improvement factor (approximately 15) in transconductance of top- versus back-gated configurations. Using the back-gate capacitance value of  $C_{\text{BG}} = 11.5 \text{ nF}/\text{cm}^2$ , the top-gate capacitance is estimated to be  $C_{\text{TG}} = 164.5 \text{ nF}/\text{cm}^2$ , corresponding to a relative dielectric



**Fig. 4.** Room temperature electrical properties of the top-gated graphene device using  $\text{Al}_2\text{O}_3$  nanoribbon as the gate dielectric. (A)  $I_{\text{ds}}-V_{\text{ds}}$  output characteristics, the channel width and length of the device is 2.1  $\mu\text{m}$  and 4.1  $\mu\text{m}$ . (B) Transfer characteristics at  $V_{\text{ds}} = 1$  V for the device using top and back gate (Inset). (C) Transconductance  $g_m$  as a function of top-gate voltage  $V_{\text{TG}}$ , the inset shows the  $g_m$  vs.  $V_{\text{BG}}$ . The plots indicate the top gate  $g_m$  is about 15 times higher than the back-gate  $g_m$ . (D) Two-dimensional plot of the device conductance at varying  $V_{\text{BG}}$  and  $V_{\text{TG}}$  bias. The unit in the color scale is  $\mu\text{S}$ . (E) The top-gate Dirac point  $V_{\text{TG\_Dirac}}$  at different  $V_{\text{BG}}$ . (F) Experimental plot (Black Line) and modeling fitting (Red Line) of  $R_{\text{tot}}$  vs.  $V_{\text{TG}}-V_{\text{TG\_Dirac}}$  relation to derive the contact resistance and carrier mobility.

**Table 1. The mobility values observed in multiple top-gate graphene transistors with variable Al<sub>2</sub>O<sub>3</sub> thickness.**

Device No.	1	2	3	4	5	6	7	8	9
Thickness (nm)	38	45	48	50	60	65	75	82	150
Mobility (cm <sup>2</sup> /V · s)	23600	22400	18200	22600	11200	15300	21100	11800	13300

constant of 8.4 for Al<sub>2</sub>O<sub>3</sub> nanoribbon, which is also consistent with the value obtained from MIM devices.

To further gauge the transistor performance, it is important to determine the carrier mobility. To accurately derive the mobility value, it is necessary to exclude the contact resistance that is comparable to the graphene transistor channel resistance. The total resistance of the device can be expressed as the following (25):

$$R_{\text{tot}} = R_{\text{contact}} + R_{\text{channel}} = R_{\text{contact}} + \frac{L/W}{ne\mu}. \quad [4]$$

Where  $R_{\text{channel}}$  is the resistance of the graphene channel covered by top-gate electrode, the contact resistance  $R_{\text{contact}}$  consists of the uncovered graphene section resistance and the metal/graphene contact resistance,  $L$  is the channel length,  $W$  is the channel width, and  $n$  is the carrier concentration in the graphene channel region, and can be approximated by the following equation

$$n = \sqrt{n_0^2 + n_{\text{TG}}^2} = \sqrt{n_0^2 + ((C_{\text{TG}}(V_{\text{TG}} - V_{\text{TG,Dirac}})/e)^2} \quad [5]$$

where  $n_0$  is the residual carrier concentration, representing the density of carriers at Dirac point (34);  $n_{\text{TG}} = C_{\text{TG}}(V_{\text{TG}} - V_{\text{TG,Dirac}})/e$  is the carrier concentration induced by the top-gate bias away from the Dirac point,  $C_{\text{TG}}$  can be approximated by the oxide capacitance of 164.5 nF cm<sup>-2</sup> (the quantum capacitance is neglected here as it is >1 order of magnitude larger approximately 2000 nF cm<sup>-2</sup>).

By fitting this model to the measured data in Fig. 4B, we can extract the relevant parameters,  $n_0$ ,  $R_{\text{contact}}$  and  $\mu$ . Fig. 4F shows the measured  $R_{\text{tot}}$  versus  $V_{\text{TG}}$  (Black Line), along with the fitted curve derived from Eq. 4 (Red Line). The fitted curve agrees well with the experimental data, with a single value of the residual concentration  $n_0 = 4.1 \times 10^{11}$  cm<sup>-2</sup>,  $R_{\text{contact}} = 1240 \Omega$ , and the mobility  $\mu = 22,400$  cm<sup>2</sup>/V · s, which represents the highest carrier mobility value observed in top-gated graphene devices to date. The fitted contact resistance  $R_{\text{contact}} \sim 1240 \Omega$  is comparable to the  $R_{\text{contact}}$  determined by four-probe measurements of similar devices (Fig. S1). The mobility value derived from top-gated configuration is also consistent with that obtained from back-gated measurement (25,600 cm<sup>2</sup>/V · s). We have studied multiple devices fabricated with the same approach, all of which exhibited carrier mobilities well exceeding 10,000 cm<sup>2</sup>/V · s (Table 1), comparable to the best reported values in back-gated devices and about one order of magnitude better than typical values previously reported for top-gated devices (17, 20, 21). The variation in mobility values is commonly seen in graphene-based devices (35), which may be attributed to variable local environment with different local potential, defects, impurities, or stress. Together, these studies clearly demonstrate that the presence of Al<sub>2</sub>O<sub>3</sub> nanoribbon on top of graphene does not lead to any mobility degradation, in contrast to previous efforts in using ALD or PVD to deposit dielectrics on graphene.

## Conclusions

In conclusion, a unique strategy has been demonstrated to integrate pristine graphene with high quality high- $\kappa$  dielectrics by

physically assembling free-standing oxide nanoribbons. Using the Al<sub>2</sub>O<sub>3</sub> nanoribbons as the gate dielectrics, the top-gated graphene transistors have been fabricated to exhibit superior performance with the highest carrier mobility observed in top-gated device to date. This method opens a unique avenue to integrate high- $\kappa$  dielectrics on graphene with the preservation of high carrier mobility. With further optimization of nanoribbon growth and assembly process to precisely control their physical dimension and spatial location (36–40), large arrays of top-gated graphene transistors or circuits can be envisioned. This physical assembly and integration approach can thus open a unique avenue to high-performance graphene electronics to impact broadly from high frequency high speed circuits to flexible electronics.

## Materials and Methods

**Synthesis of Al<sub>2</sub>O<sub>3</sub> Nanoribbons.** Aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) nanoribbons were synthesized through a physical vapor transport approach at 1400 °C. To grow Al<sub>2</sub>O<sub>3</sub> nanoribbons, aluminum, and nanometer-sized Al<sub>2</sub>O<sub>3</sub> powders with a molar ratio of 4:1 were used as the starting materials. The ceramic boat with the mixture was placed at the center of a horizontal tube furnace and an alumina piece was placed at the downstream as the deposition substrate. The temperature was raised to target temperature with a flow of 400 sccm Ar as the carrying gas. The temperature was maintained for 1 h and then naturally cooled to the room temperature.

**Dry Transfer of Al<sub>2</sub>O<sub>3</sub> Nanoribbons.** The overall process involves physical transfer of Al<sub>2</sub>O<sub>3</sub> nanoribbons directly from a Al<sub>2</sub>O<sub>3</sub> nanoribbon growth substrate to a graphene substrate via contact printing. Specifically, a graphene device substrate is first firmly attached to a benchtop, and the Al<sub>2</sub>O<sub>3</sub> nanoribbon growth substrate is placed upside down on top of the graphene substrate so that the Al<sub>2</sub>O<sub>3</sub> nanoribbons are in contact with the graphene. A gentle manual pressure is then applied from the top followed by slightly sliding the growth substrate. The Al<sub>2</sub>O<sub>3</sub> nanoribbons are aligned by shear forces during the sliding process. The sliding process results in direct dry transfer of nanoribbons from the growth substrate to the desired graphene substrate. The sample is then rinsed with isopropanol followed by nitrogen blow-dry, in which the capillary drying process near the Al<sub>2</sub>O<sub>3</sub> nanoribbons can help the Al<sub>2</sub>O<sub>3</sub> nanoribbons to be firmly attached to the substrate surface.

## Characterization of Al<sub>2</sub>O<sub>3</sub> Nanoribbons, Device Fabrication, and Measurements.

The microstructures and morphologies of the Al<sub>2</sub>O<sub>3</sub> nanoribbons were characterized by a JEOL 6700 SEM. The lattice image of the Al<sub>2</sub>O<sub>3</sub> nanoribbons was observed by an FEI Titan HRTEM. The thickness was measured using atomic force microscope (AFM, Veeco Dimension 5000). Oxygen plasma (Diener Electronic) was used to selectively etch away the unprotected graphene region and leave graphene ribbons underneath the Al<sub>2</sub>O<sub>3</sub> nanoribbon mask protection. The etch time is about 160 s at a power level of 40 W. The electrical transport properties were measured by a Lakeshore probe station with home built data acquisition system

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