

Rational growth of branched nanowire heterostructures with synthetically encoded properties and function

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Branched nanostructures represent unique, 3D building blocks for the “bottom-up” paradigm of nanoscale science and technology. Here, we report a rational, multistep approach toward the general synthesis of 3D branched nanowire (NW) heterostructures. Single-crystalline semiconductor, including groups IV, III–V, and II–VI, and metal branches have been selectively grown on core or core/shell NW backbones, with the composition, morphology, and doping of core (core/shell) NWs and branch NWs well controlled during synthesis. Measurements made on the different composition branched NW structures demonstrate encoding of functional p-type/n-type diodes and light-emitting diodes (LEDs) as well as field effect transistors with device function localized at the branch/backbone NW junctions. In addition, multibranch/backbone NW structures were synthesized and used to demonstrate capability to create addressable nanoscale LED arrays, logic circuits, and biological sensors. Our work demonstrates a previously undescribed level of structural and functional complexity in NW materials, and more generally, highlights the potential of bottom-up synthesis to yield increasingly complex functional systems in the future.

nanodevices | nanoelectronics | nanophotonics | biosensors | designed synthesis

Design and rational synthesis of semiconductor nanowire (NW) building blocks with well-defined structure and physical properties are central to the “bottom-up” approach for nanoscience and nanotechnology (1–6). To date, significant progress has been made in control of morphology, size, and composition on length scales ranging from the atomic and up (1–28). Branched or tree-like NWs, in which one or more secondary NWs grow in a radial direction from a primary NW backbone, represent an especially interesting class of NW structures because branching naturally provides access to higher dimensionality structures and the capability of achieving parallel connectivity and interconnection during synthesis (12, 13). Indeed, well-controlled variations in the composition and/or doping of backbone and branch NWs could make possible the design and realization of unique electronic and photonic nanodevices via encoding functionality synthetically at branch junctions.

Previous studies of branched NW structures have led to several advances. First, original work in 2004 (12, 13) demonstrated the controlled synthesis of Si (12), GaN (12), and GaP (13) branched NWs via a multistep nanocluster-catalyzed vapor–liquid–solid (VLS) process, in which the diameter, length, and density of nanoscale branches were defined independently from backbone NW growth. Several groups have also employed a single-step, chemical vapor transport and condensation strategy to produce a wide range of straight or twisted semiconductor branched NWs, including ZnO (14, 15), WO₃ (16), PbS (17), and PbSe (18). These studies have provided additional insight into growth mechanisms of branched nanostructures, but exhibited only limited control of the branch synthesis that is ultimately central to

defining functionality for device applications. More recently, the growth of branched heterostructures with different backbone and branch compositions, including ZnSe/CdSe (19) and ZnS/CdS (20, 21), was reported using a multistep approach similar to that described in 2004 (12, 13). This work showed the possibility for encoding distinct composition junctions at branch points through synthesis, but did not demonstrate the critical potential of such branch junctions to serve as electronic and optoelectronic devices. Here, we describe studies that extend in a substantial manner the synthesis of branched NW heterostructures and, significantly, that reveal well-defined electrical and optoelectronic junction properties, including the demonstration of addressable nanoscale light-emitting diode (LED) arrays, logic circuits, and biological sensors.

Results and Discussion

We have focused on two distinct classes of branched NWs, with metal or semiconductor branches grown on either the native surface of semiconductor (type I) or on the oxide surface of core/shell semiconductor/oxide (type II) NW backbones (Fig. 1). The synthesis involves two critical steps following synthesis of the core and core/shell NWs. First, gold nanoparticles (Au-NPs) are selectively deposited onto the respective backbone surfaces using either an in situ solution reduction of AuCl₄[−] on Si-NW surfaces for type I structures or binding of Au-NPs to the oxide surfaces of Si/SiO₂ core/shell NWs for type II structures (see *Materials and Methods*). Transmission electron microscopy (TEM) images demonstrate that these methods provide uniformly dispersed Au-NPs on the Si (Fig. S1A) and Si/SiO₂ (Fig. S1C) NW surfaces, and moreover, high-resolution TEM (HRTEM) images demonstrate intimate contact between Au-NPs and the Si (Fig. S1B) and

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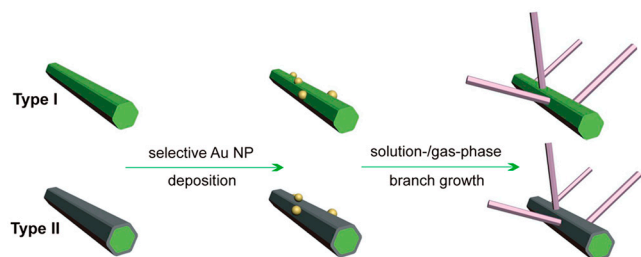


Fig. 1. Schematic illustrating the general synthesis of branched NW heterostructures. Following the synthesis of bare (type I) or core/shell (type II) NWs, Au-NPs are selectively deposited onto the respective backbone surfaces and then used as seeds or catalysts to define the nucleation and growth of branch NWs on the backbones. Branch NWs are synthesized using established aqueous solution (metal branches) and vapor-phase (semiconductor branches) methods.

SiO₂ (Fig. S1D) surfaces. Second, the resulting Au-NPs were used as seeds or catalysts to define the nucleation and growth of branch NWs on the backbones using either an aqueous solution-based method for metal branches and vapor-phase approaches for semiconductor branches.

We first examined the growth of metal and semiconductor branch NWs for type I structures. Gold metal branch NWs were grown using a reported surfactant mediated methodology (29) in aqueous solution (see *Materials and Methods*). A typical SEM image of Si/Au branched NW structures (Fig. 2A) shows that Au branches grown in this manner are uniform with an average diameter of 31 ± 4 nm and average length of 620 ± 100 nm. The overall yield of branches, which was determined with respect to the total number of Au-NP nucleation catalysts, was greater than 40% for these reaction conditions. The average aspect ratio of these Au branches, 20 ± 4 , could be further improved by reducing the Au-reactant concentration and/or increasing the surfactant

concentration, where the highest value obtained in our studies was *ca.* 50 (see *Materials and Methods*).

We further examined the Si/Au-branch NW junction structures in more detail using TEM and selected area electron diffraction (SAED). Low-resolution TEM images of Si/Au branched NW junctions (e.g., Fig. S2A) show that Au NW branches have approximately curved ends that contact the Si-NW backbone surfaces at the central region of the Au-branch NWs. A HRTEM image of the Si/Au junction (Fig. 2B) shows the single-crystalline structure of Si-NW backbone and more complex structure for the Au branch NW. Specifically, the Au branch exhibits modulations in the electron density in the central region of the NW parallel to the direction of branch axis, which are indicative of a twinned structure (29). Indeed, SAED patterns acquired to further illuminate the nature of these features (Fig. 2C) can be indexed as a superposition of $\langle 112 \rangle$ and $\langle 100 \rangle$ zones for face-centered cubic Au ($a = 0.408$ nm) (29), where the branch NW has overall fivefold twin symmetry (Fig. 2C, *Inset*). These results and model are consistent with the structure described previously by Murphy and coworkers (29).

We have also synthesized a variety of semiconductor branch NWs by vapor-phase growth, where the Au-NPs function as catalysts in a VLS process (1–3, 30) for branch elongation. SEM images of Si/Ge (Fig. 2D), Si/GaAs (Fig. 2E), and Si/GaP (Fig. 2F) backbone/branch NW structures show the uniform semiconductor branch growth from Si-NW backbones with a yield >70%. Moreover, our general approach can be extended to the growth of other III–V and II–VI semiconductor branches, including InP, InAs, ZnS, ZnSe, CdS, and CdSe (see *Materials and Methods*).

TEM images of Si/Ge (Fig. S2B), Si/GaAs (Fig. S2C), and Si/InP (Fig. S2D) show that the interfaces between backbone and branch NWs are clean and abrupt. In addition, energy dispersive X-ray mapping of Si/CdS (Fig. S2F) demonstrates the spatially controlled distributions of Si, Cd, and S in the backbone and branch. We note that the Si backbone is free of CdS homogeneous shell coating or islands formation due to the well-controlled nanocluster-catalyzed (30) branch synthesis. In addition, HRTEM studies were carried out to further characterize the Si/semiconductor branched junctions. The HRTEM images of the junctions of Si/Ge (Fig. 2G), Si/GaAs (Fig. 2H), and Si/InP (Fig. S2E) backbone/branch NWs show single-crystalline structures for all backbones and branches. These data also suggest that the backbone/branch interfaces remain structurally coherent in one or more crystallographic directions despite the large lattice mismatches for the bulk crystals (31): 4.2% for Si/Ge, 4.1% for Si/GaAs, and 8.1% for Si/InP).

To further understand strain relaxation in these branched NW structures, we carried out stress field simulations (see *Materials and Methods*). The simulation result for a Si/GaAs backbone/branch NW structure (Fig. 2I) shows that stresses are significant only in regions near the junctions (especially the junction boundary), of dimensions comparable to $1/4$ branch width, and produce deformations of negligible magnitude at distances longer than the diameter of branch from the junction region. The possibility of efficient strain relaxation in branched NW heterostructures could significantly expand our choices for backbone and branch materials, which can enable unique device concepts with enhanced properties.

We have also explored a variety of type II branched NW structures because it represents another important category of structural/functional integration, where metal or semiconductor branches can be grown on Si/SiO₂ core/shell NW backbones following the same approaches described above. SEM images of Si/SiO₂/Au (Fig. 3A) and Si/SiO₂/Ge (Fig. 3C) branched NWs exhibit morphologies similar to their respective type I analogs. The HRTEM images of both Si/SiO₂/Au (Fig. 3B) and Si/SiO₂/Ge (Fig. 3D) branched junctions show clearly an

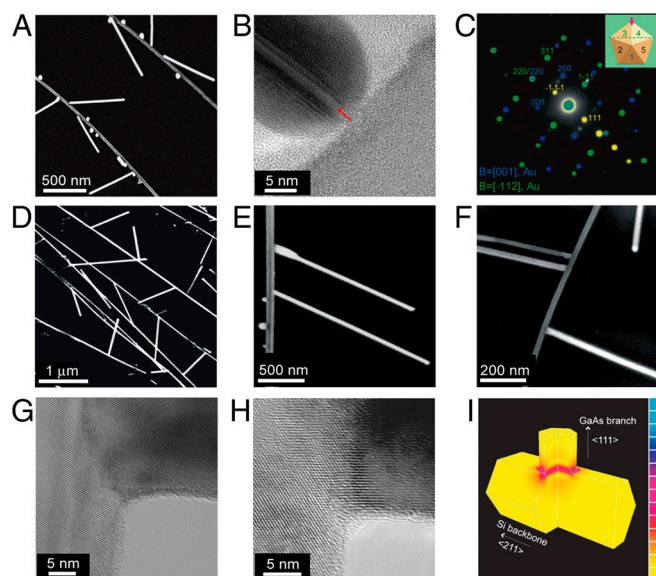


Fig. 2. Structural characterization of type I branched NW heterostructures. (A) SEM image of Si/Au branched NWs. (B) HRTEM image of Si/Au branched junction; red arrow highlights twin plane. (C) SAED pattern of the junction region shown in B, where blue and green spots originate from $\langle 100 \rangle_{\text{Au}}$ $\langle 112 \rangle_{\text{Au}}$ zone diffraction, and yellow spots are from the crystalline Si backbone. (*Inset*) Cross-sectional model of the penta-twinned Au branch consisting of five twinned subunits. Red arrow marks the incident beam direction. (D–F) SEM images of Si/Ge (D), Si/GaAs (E), and Si/GaP (F) branched NWs. (G and H) HRTEM images of Si/Ge (G) and Si/GaAs (H) branched junctions. (I) Simulated von Mises stress field at Si/GaAs branched junction. The scale bar range is from 3.1×10^6 to 1.6×10^{10} Pa.

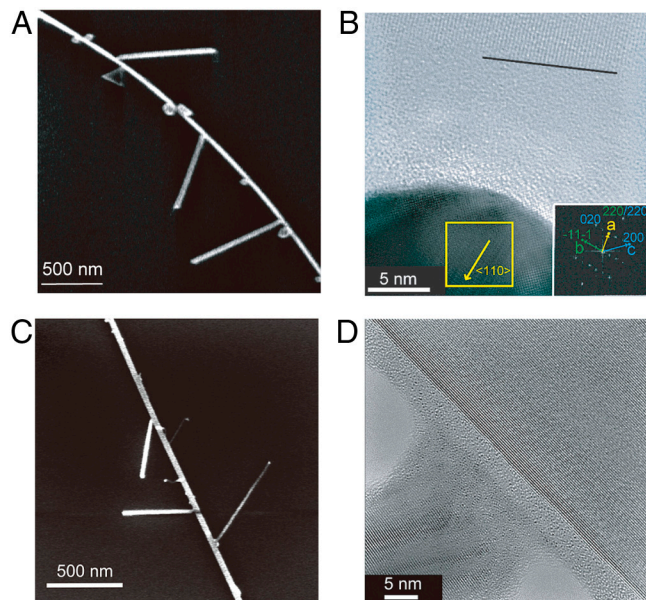


Fig. 3. Structural characterization of type II branched NW heterostructures. (A) SEM image of Si/SiO₂/Au branched NWs. (B) HRTEM image of Si/SiO₂/Au junction. The black line marks the SiO₂/Si interface. (Lower Right Inset) FFT pattern from the yellow square region, indexed as a superposition of [001] (blue) and [-112] (green) zone patterns. The marked yellow spot in the FFT pattern is one of the associated double diffraction reflections, where $a = b + c$. (C and D) SEM (C) and HRTEM (D) images of Si/SiO₂/Ge branched NW.

amorphous layer sandwiched between crystalline Si-backbone and branch NWs, which is consistent with our design for type II structures. Analysis of the Au branch last close to the junction (Fig. 3B, Inset) shows the superposition of $\langle 112 \rangle$ and $\langle 100 \rangle$ zone patterns and indicates the Au branch grows along the $\langle 110 \rangle$ direction, the same as in Si/Au branched NWs. We note that the SiO₂ shell on these Si-NW backbones can be readily extended to other types of functional materials conformally deposited by atomic layer deposition (32) and has the potential to significantly expand the scope of functionalities defined at the branched junctions.

We have fabricated and measured single-branch/backbone NW devices to examine the potential for encoding of functional device properties such as p-n diodes and field effect transistors (FETs) by synthesis (see *Materials and Methods*; Fig. S3). For example, p-n diodes should be encoded at the junction of p-Si-NW backbone and n-type semiconductor branch, where we have synthesized and studied structures with n-Ge, n-GaAs, and n-CdSe branches. Two-terminal electrical transport measurements recorded on p-Si/n-Ge, p-Si/n-GaAs, and p-Si/n-CdSe backbone/branch NW structures (Fig. 4A) all exhibit clear current rectification with threshold voltages of approximately 1.0 V, consistent with expectations for p-n diode (31). More detailed characterization of the Si/GaAs p-n diode (Fig. 4B) yields a room temperature ideality factor, n , of 2.4. Although the n value indicates surface recombination in the diode (33) and suggests that further optimization could be achieved in the future, the present results nevertheless demonstrate our capability to independently define the doping profile of backbone and branch NWs necessary for encoding device function.

We have also examined the potential for encoding nanoscale FETs in type II branched NWs, where p-Si-NW backbone serves as the active semiconductor channel, the SiO₂ shell layer as the gate dielectric, and heavily doped n-Ge or Au-branch NWs as nanoscale gate electrodes. Source and drain contacts were defined on p-Si-NW backbone, and an additional contact was made at the end of n-Ge or Au branch as voltage input for the

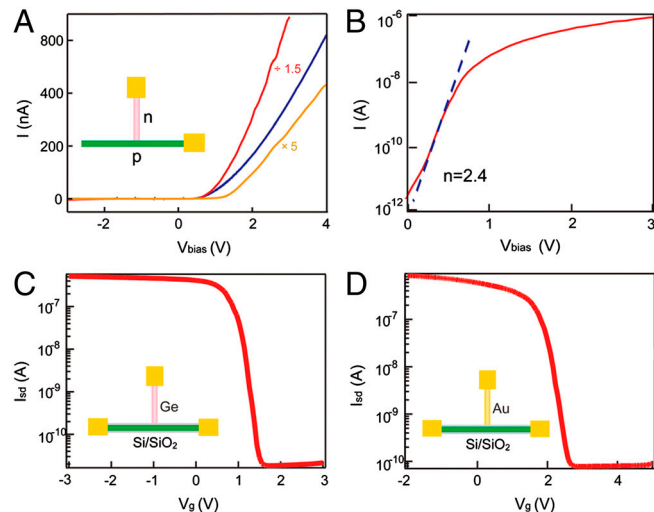


Fig. 4. Single-branch input devices. (A) Two-terminal I - V characteristics of p-n diodes encoded at p-Si/n-Ge (blue), p-Si/n-GaAs (red), and p-Si/n-CdSe (orange) branched junctions. (B) I - V curve of the same p-Si/n-GaAs diode on semilog scale; the slope (blue dashed line) yields an ideality factor $n = 2.4$. (C and D) I - V_g curves of nanoscale FETs encoded at p-Si/SiO₂/n-Ge (C) and p-Si/SiO₂/Au (D) branched junctions, respectively. A source-drain voltage of 0.5 V was used in the measurement.

gate electrode (Fig. 4C, Inset, and D, Inset and Fig. S3B and C). Current (I_{sd}) vs. branch-gate voltage (V_g) data recorded on p-Si/SiO₂/n-Ge (Fig. 4C) and p-Si/SiO₂/Au (Fig. 4D) branched NW FETs at a source-drain voltage of 0.5 V show a characteristic depletion mode FET behavior (31), with a turnoff current < 100 pA and on/off ratio $> 10^4$. The calculated subthreshold slopes for these two nanoscale FET devices are 120 and 150 mV/decade, respectively. The subthreshold values, which indicate good gate coupling, are especially notable given that the gate lengths for the n-Ge and Au-branch devices are only 30 and 35 nm, respectively.

In addition, we have investigated additional functional properties for synthetically encoded branch/backbone NW structures as well as the incorporation of multiple functional branches. First, we have characterized the photonic properties of p-Si/n-GaAs backbone/branch heterostructures, where the direct-band-gap GaAs branch can yield light emission in a forward biased diode (34). Significantly, electroluminescence (EL) data recorded from a p-Si/n-GaAs device (Fig. 5A) exhibits highly localized emission from the branch junction in forward bias, thus making these point-like, nanoscale active emitters (nanoLEDs). The EL spectrum (Fig. 5A, Lower) exhibits a peak maximum at 860 nm, corresponding to the GaAs band-edge emission. We note that the localized emission from the branch junctions was robust; that is, repeated on/off cycles did not affect the emission properties, and studies of over 20 p-Si/n-GaAs nanoLEDs yielded similar results.

We have exploited the reproducibility and robustness of the p-Si/n-GaAs nanoLEDs to study an addressable array consisting of three n-GaAs NW branches on p-Si-NW backbone (Fig. 5B). When a forward bias was applied to turn on one (Fig. 5B, Upper Right), two (Fig. 5B, Lower Left), or three (Fig. 5B, Lower Right) nanoLEDs sequentially, EL measurements demonstrate localized and addressable emission only from the junctions in forward bias. Moreover, we have assembled and characterized seven robust nanoLEDs within a $100 \times 100 \mu\text{m}^2$ area (Fig. S4), thus demonstrating the potential of this bottom-up approach for larger-scale integration of these unique photonic devices.

In addition, the concept of synthetically encoding multiple functional branch devices has been used to investigate their potential as logic gates. A two branch input FET configured from

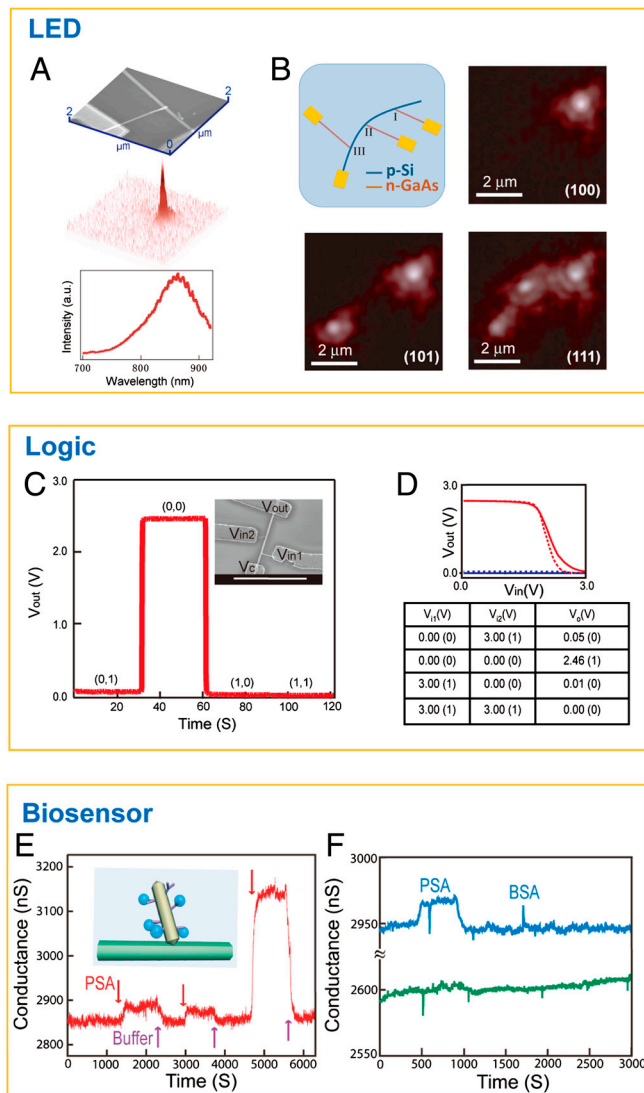


Fig. 5. Multibranch input devices. (A and B) p-Si/n-GaAs branched nanoLEDs. (A) Three-dimensional EL intensity plot (Middle), SEM image (Top), and EL spectrum (Bottom) of a single p-Si/n-GaAs branched nanoLED. (B) Schematic (Upper Left) of an LED array consisting of three p-Si/n-GaAs nanoLEDs, and EL images when a forward bias of 10 V was applied to sequentially turn on one (Upper Right), two (Lower Left), or three (Lower Right) branch junctions. (C) The output voltage vs. the four possible logic address level inputs: (0,1), (0,0), (1,0), and (1,1). (Inset) SEM image of the branched device. Scale bar, 2 μm . (D) The output–input (V_o – V_i) relation and experimental truth table for the NOR gate. The solid and dashed red (blue) lines show V_o – V_{i1} and V_o – V_{i2} when the other input is 0 (1). (E and F) Biological sensor based on Si/Au branched NW FETs. (E) Conductance vs. time curve recorded on a p-Si/Au branched NW sensor with alternate delivery of PSA (4 ng/mL, 80 pg/mL, 200 ng/mL) and pure buffer solutions. The red and purple arrows mark the delivery of protein and buffer solutions into the sensing channel, respectively. (Inset) Schematic of Si/Au branched NW sensor. (F) Conductance vs. time data recorded on Si/Au branched NW sensor with alternating delivery of 4 ng/mL of PSA and 4 $\mu\text{g/mL}$ of BSA solutions (blue curve), and on bare Si-NW device (modified as the Au branches) with delivery of 4 $\mu\text{g/mL}$ of PSA solution (green curve).

a type II Si/SiO₂/Ge branched NW structure (Fig. 5C) shows that when either one or both of the inputs were high (3 V) the p-Si-NW backbone FET output was low or off, but when both inputs were low (0 V), the FET output was high. More complete characterization of the input–output characteristics (Fig. 5D) are all consistent with two-input NOR logic gate (35). Similarly, we

have also demonstrated OR and AND gates from the integration of p-Si/n-Ge branch diodes (Fig. S5). Overall, these results suggest that the branched and hyperbranched (13) NW structures represent a potentially powerful approach for developing complex logic circuits with some analogy to highly branched and interconnected neuronal systems.

Finally, we investigated the branched NW devices as nanoelectronic sensors for detection of biological molecules (36), where the Au branches can act as “antenna” for analyte after modification with receptors. In contrast to previous studies that modified oxide surfaces of the nanowire and substrate (37, 38), we selectively modified Au branches with antibodies using reactive thiols (see *Materials and Methods*). Conductance vs. time data recorded from a monoclonal antibody modified p-Si/Au-branch NW FET as prostate specific antigen (PSA) and buffer solutions are delivered to the device (Fig. 5E) demonstrate concentration-dependent binding and unbinding of PSA with a detection limit of 80 pg/mL for signal-to-noise ratio of >3. Control experiments (Fig. 5F) using BSA and unbranched Si-NW FETs further demonstrate the excellent selectivity of Si/Au-branch NW sensor.

Conclusions

In summary, we report a rational, multistep approach for the general synthesis of branched nanowire heterostructures and demonstrate the encoding of electronic and optoelectronic functions at branched junctions through controlled synthesis. Single-crystalline semiconductors, including groups IV, III–V, and II–VI, and metal branches have been selectively grown on core or core/shell NW backbones via vapor- and solution-phase methods. With precise control over composition and doping, we demonstrate reliable p-n diode, LED, and FET device characteristics encoded at the branch junctions. Furthermore, we have demonstrated the potential to create more complicated structures and functional device-based backbone/multibranch NW structures, including addressable nanoLED arrays, logic circuits, and biological sensors. Our work highlights the power and potential of synthetically encoding functionalities at branch junctions, and more generally, bottom-up synthesis for the development of increasingly complex functional systems in the future.

Materials and Methods

Backbone NW Synthesis. Si-NW backbones were synthesized using nanocluster-catalyzed chemical vapor deposition method reported previously (39). Si/SiO₂ core-shell NWs were prepared by oxidation of Si NWs in pure O₂ (flow rate: 50 sccm; pressure: 40 torr) at 700 °C for 1–3 h; the resulting oxide layer thickness was 2–5 nm, respectively.

Selective Deposition of Au Nanoparticles. Au-NPs were deposited on bare Si NWs by galvanic surface reduction (40). First, Si NWs were etched in 5% hydrogen fluoride solution for 1 min to produce hydrogen-terminated surface, and then resulting Si NWs were immersed in HAuCl₄ solution ($1 - 5 \times 10^{-5}$ M) for 5–10 min. The HAuCl₄ solution concentration and reaction time was varied to control the Au-NP density and size, with higher HAuCl₄ and longer reaction time resulting in larger and denser Au-NPs. Au-NPs were deposited on the SiO₂ surfaces of Si/SiO₂ core/shell NWs in a two-step process. First, the Si/SiO₂ NWs were immersed in 0.1% polylysine solution (molecular weight: 150 k–300 k, Ted Pella) and rinsed thoroughly with deionized water. Second, the polylysine modified NWs were placed in the solution of citrate stabilized Au-NPs (15 nm, 1.4×10^{10} /mL, Ted Pella) for 5 min, followed by gentle rinse with deionized water.

Synthesis of Si/Au and Si/SiO₂/Au branched NWs. Si or Si/SiO₂ NWs with deposited Au-NPs were dispersed on SiO₂ surfaces of Si substrates (600-nm oxide, n-type 0.005 Ω -cm, Nova Electronic Materials) from isopropanol solutions, dried with N₂, and then annealed at 200 °C for 10 min. Au branched NWs were then grown by immersing the respective substrates with dispersed NWs in a solution containing HAuCl₄ ($2 \times 10^{-4} - 1 \times 10^{-3}$ M), ascorbic acid ($4 \times 10^{-4} - 2 \times 10^{-3}$ M), and cetyl trimethylammonium bromide (CTAB) (0.025–0.1 M) (29) for 12–24 h in the dark. A Au-NW aspect ratio up to 50 can be achieved under optimal growth conditions with 1×10^{-3} M HAuCl₄, 2×10^{-3} M ascorbic acid, and 0.1 M CTAB.

Synthesis of Si/semiconductor and Si/SiO₂/semiconductor branched NWs. Si or Si/SiO₂ NWs with deposited Au-NPs were dispersed on SiO₂ surface of heavily Si substrates as above and then immediately placed into the appropriate NW gas phase growth system to prepare branched semiconductor NWs. Ge branches were grown at 290 °C, 200 torr for 15 min, with the flow of 10 sccm GeH₄ (10%), 10 sccm PH₃ (1,000 ppm in H₂), and 200 sccm H₂ as described previously (41). The growth of other III-V and II-VI branches was achieved by thermal evaporation and vapor transport method (42). Powders with the same composition were put into the center of the quartz tube, which was heated to 650–780 °C, while the branch growth temperature was approximately 400–600 °C. 30 sccm of H₂ was used as the carrier gas, and pressure was kept at 40 torr.

Device Fabrication and Measurement. Single- and multiple-branch input devices were fabricated on SiO₂ surface of Si substrates (50-nm thermal oxide, n-type 0.005 Ω-cm, Nova Electronic Materials) using electron beam lithography (43) followed by thermal evaporation of metals. Ti/Pd (5/50 nm) contacts were used for both Si and Ge NWs; Ti/Al/Pd/Au (20/80/20/30 nm) contacts were used for other III-V and II-VI semiconductor NWs. Current-voltage (*I*-*V*) data were recorded using an Agilent semiconductor parameter analyzer (Model 4156C) with contacts to devices made using a probe station (Desert Cryogenics, Model TTP4). EL from branched NW structures was characterized with a homebuilt microluminescence instrument (44). Arrays of Si/Au-NP NW devices were defined by photolithography (37). Ti/Pd (5/50 nm) metal contacts were deposited by thermal evaporation and then passivated by subsequent deposition of 50-nm thick Si₃N₄ coating (37). The completed device chip was subject to Au-branch growth as described above.

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The Au branches were modified in two steps. First, the devices were reacted with a 10 mg/mL solution of DMSO (Sigma-Aldrich) for approximately 4 h, followed by extensive rinsing with DMSO. Anti-PSA (Ab1, clone ER-PR8, NeoMarkers) was then coupled to the succinimidyl(NHS)-terminated Au branches surfaces by reaction of 10–20 μg/mL antibody in a pH 8.4, 10 mM phosphate buffer solution for a period of 2–4 h. Unreacted NHS groups were subsequently passivated by reaction with ethanolamine under similar conditions. PSA and BSA protein samples in 1 μM phosphate buffer solution (pH, 7.4) were flowed under a flow rate of 0.30–0.60 mL/h through the microfluidic channel while monitoring the branch nanowire device properties as described in detail elsewhere (37).

Stress Field Simulation. Stress field simulations were carried out using finite element method (ABAQUS software, version, 6.5-1). To simulate the stress in Si/GaAs branched structure, we took the axis of GaAs branch and Si backbone as (111) and (211), respectively, and the following material constants are used: modulus of elasticity, $c_{11(\text{GaAs})} = 1.18 \times 10^{11}$ Pa, $c_{12(\text{GaAs})} = 0.538 \times 10^{11}$ Pa, $c_{44(\text{GaAs})} = 0.594 \times 10^{11}$ Pa, $c_{11(\text{Si})} = 1.662 \times 10^{11}$ Pa, $c_{12(\text{Si})} = 0.664 \times 10^{11}$ Pa, $c_{44(\text{Si})} = 0.798 \times 10^{11}$ Pa; lattice constant, $a_{(\text{Si})} = 0.543$ nm, $a_{(\text{GaAs})} = 0.565$ nm; backbone to branch width ratio, 2:1.

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