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## An Integrated Power-Efficient Active Rectifier With Offset-Controlled High Speed Comparators for Inductively Powered Applications

Hyung-Min Lee[Student Member, IEEE] and Maysam Ghovanloo[Senior Member, IEEE]  
GT-Bionics Lab, School of Electrical and Computer Engineering, Georgia Institute of Technology,  
Atlanta, GA 30308 USA

Maysam Ghovanloo: mgh@gatech.edu

### Abstract

We present an active full-wave rectifier with offset-controlled high speed comparators in standard CMOS that provides high power conversion efficiency (PCE) in high frequency (HF) range for inductively powered devices. This rectifier provides much lower dropout voltage and far better PCE compared to the passive on-chip or off-chip rectifiers. The built-in offset-control functions in the comparators compensate for both turn-on and turn-off delays in the main rectifying switches, thus maximizing the forward current delivered to the load and minimizing the back current to improve the PCE. We have fabricated this active rectifier in a 0.5- $\mu\text{m}$  3M2P standard CMOS process, occupying 0.18 mm<sup>2</sup> of chip area. With 3.8 V peak ac input at 13.56 MHz, the rectifier provides 3.12 V dc output to a 500  $\Omega$  load, resulting in the PCE of 80.2%, which is the highest measured at this frequency. In addition, overvoltage protection (OVP) as safety measure and built-in back telemetry capabilities have been incorporated in our design using detuning and load shift keying (LSK) techniques, respectively, and tested.

### Index Terms

Active rectifier; back telemetry; high speed comparators; implantable microelectronic devices; inductive power transmission; load shift keying; offset control; RFID

### I. Introduction

Implantable microelectronic devices (IMD) powered by internal batteries suffer from their large volume, limited lifetime, replacement hardship, and cost. Therefore, they are only suitable for medical treatments with ultra low power requirements, such as pacing the heart, which have extended battery lifetimes in the range of several years [1]. On the other hand, there are treatments, such as neuroprostheses like cochlear and retinal implants, which require orders of magnitude higher currents for stimulation or recording regardless of the circuit efficiency [2]. There are also applications such as radio frequency identification (RFID), in which the size and cost of neither primary nor secondary (i.e., rechargeable) batteries are justified [3]. To address these limitations, wireless power transmission techniques using inductive links have been utilized to supply size-, cost-, and power-constrained devices and applications.

Inductively powered systems in general consist of three main components: reader, inductive link, and transponder, as shown in Fig. 1. On the reader side, which is also the power transmitter, a power amplifier drives the primary coil,  $L_1$ , at the power carrier frequency,  $f_c$ . This signal is induced on to the secondary coil,  $L_2$ , through the inductive link, and generates an ac voltage across the transponder resonance circuit,  $L_2$  and  $C_2$ . Following the  $L_2C_2$  tank, there is always a rectifier to convert the ac signal to dc ( $V_{REC}$ ) for supplying the rest of the transponder. The efficiency and performance of this rectifier, which is the focus of this article, is key to the overall power efficiency of the system, because all the usable received power passes through it. Since the dc voltage varies significantly with the coils' relative distance,  $d$ , and alignment, a low dropout regulator often follows the rectifier for providing a constant supply voltage,  $V_{DD}$ , to the IMD or RFID load.

Considering the power flow from the external energy source (i.e., the battery) to the load,  $R_{LR}$ , the total power conversion efficiency (PCE) can be calculated from

$$\eta_{total} = \eta_{PA} \times \eta_{link} \times \eta_{rectifier} \times \eta_{regulator} \quad (1)$$

where  $\eta_{PA}$ ,  $\eta_{link}$ ,  $\eta_{rectifier}$ , and  $\eta_{regulator}$  are the efficiencies of the power amplifier, inductive link, rectifier, and regulator, respectively. Achieving higher PCE ( $\eta_{total}$ ) is very important in inductively powered applications because it allows IMDs to operate with smaller received power from a larger distance. Lower received power also reduces the risk of tissue damage from overheating [2]. In the IMD applications,  $\eta_{link}$  is limited due to the size constraint of the secondary coil [4]. The regulator, on the other hand, already has a high  $\eta_{regulator}$  because of its low dropout topology. Therefore, improving the rectifier PCE ( $\eta_{rectifier}$ ) is a key factor for safe IMD operation.

Passive rectifiers using diodes or diode-connected transistors have been used in the past for inductively powered applications [5]–[9]. However, PN junction diodes induce large forward voltage drops and power dissipation. Schottky diodes have low dropout voltages [10]. However, they have a high leakage current, they are not available in most standard CMOS processes, and may need extra fabrication steps. Their reverse breakdown voltages may not be high enough either. Several  $V_{Th}$  cancellation techniques have been proposed to reduce the passive diode voltage drop [11]–[14]. However, these are sensitive to process variations and still unable to provide high PCE. Therefore, active synchronous rectifiers using comparator controlled rectifying switches are currently considered the most promising solutions for increasing the PCE in ASICs [15]–[24]. In these rectifiers, voltage drop across the main rectifying switches is much lower than the diode voltage drop, dissipating less power within the rectifier. We previously reported power efficient active rectifiers using phase lead in [16] and [24]. The maximum operating frequency of those rectifiers, however, was limited to 1–2 MHz. Active rectifiers need significantly faster comparators to drive their switches at the right times for higher carrier frequencies, such as 13.56 MHz in the Industrial, Scientific, and Medical (ISM) band, and maximize the forward current flow, while minimizing the reverse currents.

In this paper, we propose an integrated power efficient active rectifier with offset-controlled high speed comparators for inductively powered applications. Comparators are equipped with offset control functions to compensate for both turn-on and turn-off delays, optimizing the power transfer from the secondary coil to the load (regulator). Section II presents the operating principles and the PCE analysis of our new active rectifier architecture. Section III describes the concept, implementation, and effects of the proposed offset-control functions on the high speed comparators. The simulation and measurement results are depicted in Section IV, followed by conclusions in Section V.

## II. Active Rectifier Architecture

### A. Operating Principle and Implementation

The new full-wave active rectifier employs a pair of high-speed comparators ( $CMP_1$  and  $CMP_2$ ) to drive the main rectifying elements ( $P_1$  and  $P_2$ ) in Fig. 2. Ideally, the input voltage of the rectifier,  $V_{IN} = V_{IN1} - V_{IN2}$ , has a sinusoidal waveform. Hence,  $P_1$  and  $P_2$  turn on alternatively depending on the polarity and amplitude of  $V_{IN}$ .

When  $V_{IN} > V_{ThN}$  (the NMOS threshold voltage) and  $|V_{IN}| < V_{REC}$ , the positive feedback operation of the cross-coupled NMOS pair ( $N_1$  and  $N_2$ ) connects  $V_{IN2}$  to  $V_{SS}$  through  $N_2$  and turns off  $N_1$ . In this case,  $CMP_2$  output goes high because  $V_{REC} > V_{SS}$ , and  $P_2$  is turned off.  $P_1$  also remains off as long as  $|V_{IN}| < V_{REC}$ . When  $|V_{IN}| > V_{REC}$ ,  $CMP_1$  output goes low and turns  $P_1$  on. Therefore, current flows from  $V_{IN1}$  to  $V_{REC}$ , and charges the rectifier's resistive/capacitive load ( $R_L C_L$ ). In the next half cycle, when  $V_{IN} < -V_{ThN}$ ,  $V_{IN1}$  is connected to  $V_{SS}$  through  $N_1$ ,  $N_2$  turns off, and both  $P_1$  and  $P_2$  are also initially off for the period of  $|V_{IN}| < V_{REC}$ . Then, after  $|V_{IN}| > V_{REC}$ ,  $CMP_2$  turns  $P_2$  on and current flows from  $V_{IN2}$  to  $V_{REC}$  to charge the resistive/capacitive load again.

To avoid latch-up and substrate leakage problems among  $P_1$  and  $P_2$ , potentials at their separated N-well body terminals ( $V_{B1}$  and  $V_{B2}$ ) need to be the highest potentials on-chip. We adopted the dynamic body bias control technique from [6] and [25] by utilizing auxiliary PMOS transistors,  $P_3$  to  $P_6$ . With this method,  $V_{B1}$  and  $V_{B2}$  are automatically connected to the highest potential between the input voltages,  $V_{IN1}$  and  $V_{IN2}$ , and the output voltage,  $V_{REC}$ , of the rectifier.

### B. Back Telemetry and Overvoltage Protection

To add back telemetry capability, which is desired to inform the reader about the status of the IMD, deliver measured biosignals, or close the power control loop [26], [27], we have employed the load shift keying (LSK) scheme by shorting the secondary coil,  $L_2$ , with the short-coil (SC) data signal [9]. A pair of NMOS switches,  $N_3$  and  $N_4$ , has been added in parallel to the cross-coupled  $N_1$  and  $N_2$ , respectively. When the data signal is high, the input nodes of the rectifier are shorted together, leading to increased secondary quality factor,  $Q_2$ , and increased voltage across the primary coil,  $L_1$ . Back telemetry data from the transponder to the reader is detected by sensing these variations across the external LSK sensing block in Fig. 1.

$V_{IN}$  highly depends on the coils mutual coupling,  $M$ , which is in turn highly dependent on the coils separation,  $d$ , and alignment [4]. Loading variations also change  $Q_2$  and affect  $V_{IN}$  even when  $M$  is constant. Unexpected variations in  $M$  and  $R_{LR}$  may cause  $V_{REC}$  to exceed the safe voltage limits of the application or fabrication process and result in transistor breakdown. To prevent this problem, we have added an overvoltage protection (OVP) circuit to the rectifier by comparing a quarter of  $V_{REC}$  with a constant reference voltage. When  $V_{IN}$  exceeds a certain level, the comparator output goes high and a detuning capacitor ( $C_{ovp}$ ) is added in parallel across the secondary tank circuit, as shown in Fig. 1, to reduce  $V_{IN}$  by detuning it. The advantage of this method over current leakage based techniques [10] is that no extra heat is dissipated within the ASIC and IMD as a result of this protective safety measure.

### C. PCE Analysis and Considerations

PCE depends on the size of the rectifying PMOS and the cross-coupled NMOS pairs because these transistors are in the main current path. For example, when  $V_{IN1} - V_{IN2} > V_{REC}$ ,  $P_1$  and  $N_2$  turn on and open a current path to the load, as shown in Fig. 3. In this case,

the total lost power,  $P_{\text{Loss,total}}$ , will be dominated by the switching loss of  $P_1$  ( $P_{\text{Loss},C_{gp}}$ ),  $R_{\text{on}}$  loss of  $P_1$  ( $P_{\text{Loss},R_{onp}}$ ), and  $R_{\text{on}}$  loss of  $N_2$  ( $P_{\text{Loss},R_{onn}}$ ). Since the gate of  $N_2$  is always connected to the input node of the rectifier, there is negligible switching loss for charging and discharging the gate capacitance of  $N_2$ . Therefore,  $P_{\text{Loss,total}}$  can be approximated by

$$\begin{aligned} P_{\text{Loss,total}} &= P_{\text{Loss},C_{gp}} + P_{\text{Loss},R_{onp}} + P_{\text{Loss},R_{onn}} \\ &= C_{gp} V_{\text{REC}}^2 2f_c + I_p^2 R_{onp} D_{\text{eff}} + I_n^2 R_{onn} D_{\text{eff}} \\ &= W_p C_{gp}^* V_{\text{REC}}^2 2f_c + \left( \frac{V_{\text{REC}}}{R_L D_{\text{eff}}} \right)^2 \times D_{\text{eff}} (R_{onp} + R_{onn}) \end{aligned} \quad (2)$$

where  $C_{gp}^*$  is the gate capacitance per unit width of  $P_1$ ,  $f_c$  is the carrier frequency (13.56 MHz),  $D_{\text{eff}}$  is the effective duty cycle including comparator delay, and  $W_p$  is the width of  $P_1$ .

In this design, we have assumed  $W_n = W_p$  for the sake of simplicity. However, we have also proven in [24] that the optimal size ratio of the PMOS and NMOS transistors can be found from

$$\left( \frac{W_p}{W_n} \right)_{\text{opt}} = \sqrt{\frac{K_n \cdot (V_{\text{REC}} - V_{ThN})}{K_p \cdot (V_{\text{REC}} - |V_{ThP}|)}} \quad (3)$$

where  $K_p = \mu_p C_{\text{ox}}$  and  $K_n = \mu_n C_{\text{ox}}$  are the PMOS and NMOS transconductances, respectively. One should note that even though larger transistor size decreases the  $R_{\text{on}}$  loss, it increases the switching loss and comparator delays due to the larger gate capacitance. Therefore, the main rectifying transistors have an optimal size for minimum power dissipation depending on  $f_c$  and  $R_L$ , which should also comply with the total chip area that is allocated to the rectifier [24].

$T_{PHL}$  and  $T_{PLH}$ , the turn-on and turn-off delays of  $\text{CMP}_{1,2}$ , affect the rectifier PCE because these delays hinder  $P_{1,2}$  switches from turning on and off at proper times and cause back current. Our model considers the size of the rectifying transistors and comparator delays to estimate the maximum PCE. In the Appendix, we have defined  $W_p$ ,  $R_{onp} + R_{onn}$ , and  $D_{\text{eff}}$  as functions of the switching duty cycle ( $D$ ),  $T_{PHL}$ , and  $T_{PLH}$ , and differentiated (2) with respect to  $D$  to minimize  $P_{\text{Loss,total}}$ . With the power loss from (2), we can estimate the maximum PCE of the rectifier

$$\eta_{\text{rectifier}} = \frac{P_{\text{Load}}}{P_{\text{Load}} + P_{\text{Loss,total}} + 2P_{\text{Comparator}}} \quad (4)$$

where  $P_{\text{Load}}$  is the output power, and  $P_{\text{comparator}}$  is the total power consumption of each comparator excluding the charging and discharging power consumption of  $P_{1,2}$  gates, which has already been considered in  $P_{\text{Loss,total}}$ .

Fig. 4 shows the calculated rectifier PCE versus  $W_p$  for various comparator delays, using parameters from the ON Semi 0.5- $\mu\text{m}$  standard CMOS process. In this calculation, we assume that  $P_{\text{Load}} = 20$  mW,  $V_{\text{REC}} = 3.2$  V,  $R_L = 500$   $\Omega$ , and  $P_{\text{comparator}} = 0.1$  mW, which are based on the simulation results. It can be seen that with  $W_p = 2100$   $\mu\text{m}$  and  $T_{PHL} = T_{PLH}$

= 0 ns, the rectifier achieves the highest PCE of 92%. This is the theoretical upper limit for the PCE that can be obtained by choosing optimized transistor width and eliminating the effect of comparators' delay by utilizing offset-controlled high speed comparators that are described in Section III.

### III. Offset-Controlled High Speed Comparators

#### A. Concept of the Offset-Control Function

In order to drive the large rectifying PMOS transistors at high operating frequency of 13.56 MHz, high speed comparators with low power consumption and high driving capability are required. Typically, the comparator operating speed is limited by its propagation delay,  $T_P$ , which is how quickly the output responds to a change at the input. In this rectifier application, the comparator propagation delay adversely affects the PCE. Due to  $T_{PHL}$ , the comparators turn  $P_{1,2}$  on too late and reduce the input power that could otherwise be transferred to the load during this delay. Moreover, due to  $T_{PLH}$ , comparators lag in turning  $P_{1,2}$  off, and current can instantaneously flow from  $C_L$  back to the secondary coil when  $V_{IN} < V_{REC}$ .

Since it is not possible to reduce  $T_P$  to zero, in order to overcome such limitations, we have utilized offset control function in the high speed comparators used in this rectifier. Fig. 5 shows the block diagram of this comparator, which consists of a common-gate type comparator (CG Cmp), two offset-control blocks (Offset<sub>F</sub> and Offset<sub>R</sub>), and current-starved (CS) inverters. Offset-control blocks inject a programmable offset current,  $OS_F$  and  $OS_R$ , to the inputs of the CG comparator alternately depending on the state of the  $V_{OUT}$  feedback signals,  $FB_F$  and  $FB_R$ . Therefore,  $V_{OUT}$  expedites the falling or rising transition by sensing them ahead of time.

Segment-(a) in Fig. 6 exhibits a falling  $V_{OUT}$  transition, occurring when  $|V_{IN}| = |V_{IN1} - V_{IN2}| > V_{REC}$ . At this point, the CG comparator output,  $V_{OUT}$ , falls to turn on  $P_1$  (or  $P_2$ ).  $FB_F$  is low during this period, and only the Offset<sub>F</sub> block operates to inject offset current to the negative input of the CG comparator. With the help of Offset<sub>F</sub>,  $V_{OUT}$  can be forced to fall even before  $|V_{IN}|$  exceeds  $V_{REC}$  at the end of segment-a, compensating for the comparators' turn-on delay. It is important, however, to note that Offset<sub>F</sub> has to be turned off after the  $V_{OUT}$  falling transition so that it does not affect the following  $V_{OUT}$  rising transition. Otherwise, Offset<sub>F</sub> can delay the rising  $V_{OUT}$  transition, which is counterproductive. This is why in Fig. 5 the Offset<sub>F</sub> block receives a feedback signal from  $V_{OUT}$  and properly turns off after every falling transition of  $V_{OUT}$ .

On the other hand, during the  $V_{OUT}$  rising transition in segment-(b), when  $|V_{IN}| < V_{REC}$ ,  $FB_R$  that has gone low after  $V_{OUT}$  falling, turns on the Offset<sub>R</sub> block. The Offset<sub>R</sub> block injects offset current to the positive input of the CG comparator and can force  $V_{OUT}$  to start rising even before  $|V_{IN}|$  falls below  $V_{REC}$ . This helps  $P_1$  (or  $P_2$ ) to turn off at a proper time and prevents the back current.

If the Offset<sub>R</sub> block turns on just after  $V_{OUT}$  starts to fall, this instantaneous negative feedback mechanism hinders  $V_{OUT}$  from falling down fully and causes  $V_{OUT}$  to fluctuate. To avoid this problem, we have added two current-starved inverters in the feedback loop to add a delay between  $V_{OUT}$ ,  $FB_F$ , and  $FB_R$  transitions, thus assuring stable comparator feedback operation. This delay does not need to be precise as long as it is less than one carrier cycle period. It results in a short period, segment-(c), during which both Offset<sub>F</sub> and Offset<sub>R</sub> blocks are on.

## B. Circuit Implementation

Fig. 7 shows the schematic diagram of the high speed comparator with two offset-control functions,  $\text{Offset}_F$  and  $\text{Offset}_R$ . Without considering offset-control blocks and CS inverters, it basically works as a simple common-gate comparator with start-up capability [15]. Two input voltages,  $V_{\text{REC}}$  and  $V_{\text{IN1}}$ , are applied to the sources of input transistors,  $P_7$  and  $P_8$ , respectively. When  $V_{\text{IN1}} > V_{\text{REC}}$ , the current flowing through  $P_8$  becomes larger than that of  $P_7$ . Therefore, the gate voltage of the output inverter,  $V_A$ , rapidly increases, and  $V_{\text{OUT}}$  falls to turn  $P_1$  on. The  $\text{Offset}_F$  and  $\text{Offset}_R$  blocks are implemented by using current sources,  $P_{13}\text{--}P_{14}$  and  $P_{10}\text{--}P_{11}$ , within the comparator, MUXs, and the control switches,  $P_{15}$  and  $P_{12}$ . These blocks inject offset currents to the comparator inputs alternatively, inducing the desired timing. For example, when  $V_{\text{OUT}}$  is high,  $P_{15}$  turns on, and an offset current flows into the comparator positive input branch ( $V_{\text{REC}}$ ) through  $OS_F$ , causing  $V_A$  to increase. Therefore,  $V_{\text{OUT}}$  starts to fall earlier before  $V_{\text{IN1}}$  exceeds  $V_{\text{REC}}$ . The offset current is programmable by using 2-bit off-chip control signals per offset-control block, CTL0:1 and CTL2:3, in order to adjust the rectifier timing in response to process variations.

## C. Effects of Offset-Control Functions on PCE

Simulation results depicting the relationship between the PCE and offset-control functions are shown in Fig. 8. To understand the effects of the offset-control functions better, we have overlapped the rectifier input/output voltages, input current, and input power waveforms while adjusting  $V_{\text{IN}}$  amplitude to achieve a constant  $V_{\text{OUT}} = 3.2$  V for  $R_L = 500$   $\Omega$ . Fig. 8(a) shows that with no comparator offset-control function in place, the back current resulting from the turn-off delay severely degrades the PCE. This back current can be prevented by using the  $\text{Offset}_R$  function, as shown in Fig. 8(b). Even though  $\text{Offset}_R$  improves the PCE significantly, the input power to the rectifier is still being reduced due to the comparators' turn-on delay,  $T_{\text{PHL}}$ . Therefore, there is room to further improve the rectifier PCE as well as voltage conversion efficiency (VCE) by using both  $\text{Offset}_F$  and  $\text{Offset}_R$  functions to compensate for  $T_{\text{PHL}}$  and  $T_{\text{PLH}}$  delays, respectively. Fig. 8(c) clearly shows that with both functions in place  $V_{\text{OUT}}$  transitions happen at the right times, and the PCE is maximized.

Since the offset-control blocks consume additional power to provide the offset currents, the power overhead for employing these functions needs to be considered. Fig. 9 shows the simulated comparator power consumption versus  $V_{\text{REC}}$  and its break down between the two blocks. When  $V_{\text{REC}}$  increases, the power consumption of the CG comparator, curve-(b) also increases, contributing a large portion of the comparator power consumption, curve-(a). This is because both the static current of the CG comparator and the shoot-through current of the output inverter increase with  $V_{\text{REC}}$ . Moreover, since the comparator offsets have been tuned for  $V_{\text{REC}} = 3.12$  V, power consumption becomes more severe at higher  $V_{\text{REC}}$ . On the other hand, curve-(c), the offset-control blocks' power consumption shows a mild increase when  $V_{\text{REC}}$  increases. It is because the offset-control blocks consume only dynamic power for a short period. For  $V_{\text{REC}} = 3.12$  V, the entire high speed comparator consumes 135  $\mu\text{W}$ , 40  $\mu\text{W}$  of which is the power consumption of the offset-control blocks. The entire comparator power consumption is little affected by the load conditions as long as  $V_{\text{REC}}$  is fixed.

## D. Startup Capability

Since no supply voltage is available before the active rectifier starts its operation, it is necessary for the rectifier to have self startup capability. Our high speed comparator, shown in Fig. 7, has a common-gate input stage, in which the two comparator input voltages,  $V_{\text{IN1}}$  and  $V_{\text{REC}}$ , are also the positive supply voltages. Hence the rectifier sinusoidal input voltage,  $V_{\text{IN1,2}}$ , guarantees that the rectifier reliably starts up even before  $V_{\text{REC}}$  is sufficiently charged up. For example, when  $V_{\text{REC}} = 0$  V, the input voltage of the output inverter,  $V_A$ , follows  $V_{\text{IN1}}$  through  $P_8$ , since  $N_6$  is turned off. Therefore, when  $V_{\text{IN1}} > V_{\text{ThN7}}$ ,  $V_{\text{OUT}}$  of the

comparator will be connected to  $V_{SS}$  through  $N_7$  leading the rectifying PMOS to turn on and charge  $V_{REC}$ .

Since the comparator bias current is generated by  $P_7$ - $P_9$ - $N_5$  branch, it properly turns on when  $V_{REC} > V_{ThP7} + V_{ThN5}$ . On the other hand, when  $0 < V_{REC} < V_{ThP7} + V_{ThN5}$ , the comparator still turns on the rectifying PMOS for conducting current to  $V_{REC}$ , as explained above, but it does not turn them off at the right time, resulting in back current. Now, if  $V_{IN,peak}$  is high enough ( $> 2.9$  V in our design), then it will be sufficient for charging  $V_{REC}$  to surpass the  $V_{ThP7} + V_{ThN5}$  level even in the presence of the back current. While  $V_{REC}$  is being charged, the gate voltage of  $N_{5,6}$  also increases, and  $V_A$  decreases to turn off the rectifying PMOS during  $V_{IN1} < V_{REC}$ . Moreover, the comparator operation and the rectifier PCE move towards their optimal points as  $V_{REC}$  increases toward the target value of 3.12 V. Therefore, once  $V_{REC}$  exceeds  $V_{ThP7} + V_{ThN5}$ , it can easily charge up to 3.12 V. Fig. 10 shows simulated waveforms for the rectifier self startup process, which guarantees that  $V_{REC}$  is charged up to 3.12 V when  $V_{IN,peak} = 3.4$  V (3.8 V in measurements). In this design, for an input voltage of  $V_{IN,peak} = 2.9$  V (3.2 V in meas.), the suboptimal operation of the rectifier results in  $V_{REC} = 2.5$  V.

## IV. Simulation and Measurement Results

The active rectifier was fabricated in the ON Semiconductor 0.5- $\mu\text{m}$  3M2P standard CMOS process (minimum transistor length of 0.6  $\mu\text{m}$ ) for its relatively high voltage handling capability. Fig. 11 shows the chip micrograph, which includes the active rectifier, overvoltage protection circuit, and the low dropout regulator, occupying 0.4  $\text{mm}^2$  of the Si area with  $W_p/L_p = W_n/L_n = 2100 \mu\text{m}/0.6 \mu\text{m}$ . Since each comparator offset-control function can be enabled or disabled by external control lines, we were able to evaluate the rectifier performance with and without the comparator offset functions.

### A. Measured Waveforms and Parasitic Effects

Fig. 12 shows the lumped model of the circuit used in the rectifier measurements with emphasis on the inductive and capacitive parasitic components, which combined with the measurement instrument (oscilloscope) parasitic, cause distortion in the measured waveforms at this relatively high operating frequency ( $f_c = 13.56$  MHz). For instance, when the rectifier starts conducting, there is a sudden drop in  $V_{IN1} - V_{IN2}$ , and when it stops conducting, the stored energy in the interconnect inductors cause a sudden voltage hike across the rectifier inputs. Therefore, it is important to note that the voltages measured across the coil or load,  $V_{XY}$ , are not exactly the same as those measured on the rectifier packaged IC pins,  $V_{xy}^*$  (LQFP176). For example,  $L_{bond}$ , the parasitic inductance of the wirebond, and  $L_{wire}$ , the parasitic inductance of the external interconnects, cause the rectifier input voltage at the package,  $V_{IN1}^* - V_{IN2}^*$ , to be distorted and have a peak voltage higher than the sinusoidal input voltages at the secondary coil,  $V_{IN1} - V_{IN2}$ .

Moreover, the instantaneous input current flows into the rectifier through the parasitic inductors only during the rectifier turn-on, which is much shorter than one operating cycle (see Fig. 8(c)). Therefore, the frequency components, which affect the parasitic inductors and distort the voltage waveforms, are effectively much higher than the carrier frequency at 13.56 MHz. Unfortunately, this effect has not been considered in the recent literature on active rectifiers, and consequently, depending on how the measurements are done, the reported results on the rectifier efficiency might have been optimistic.

Fig. 13 shows the active rectifier measured input and output voltage waveforms. In these measurements we refrained from directly probing  $V_{OUT}$  because it could load and affect the

comparator performance. Instead,  $C_L$  was reduced from  $10\ \mu\text{F}$  to  $100\ \text{pF}$  to better show the effects of offset-control functions. For all measurements and simulations in this section, we enabled the  $\text{Offset}_R$  to prevent the back currents. When the  $\text{Offset}_F$  function was enabled,  $V_{\text{REC}}$  started to increase  $\sim 5\ \text{ns}$  earlier than without  $\text{Offset}_F$ . This comparison, which is consistent with the simulation results in Fig. 8, shows that the comparators turn the rectifier on faster to deliver current for a longer time period. Therefore, the  $\text{Offset}_F$  function not only improves the PCE but also reduces the rectifier dropout voltage,  $V_{\text{drop}}$ , which is defined as the difference between  $V_{\text{IN1,Peak}}^*$  and  $V_{\text{REC}}$ . There is also a small phase shift between the ripple on  $V_{\text{REC}}$  and  $V_{\text{IN1,2}}^*$  due to the parasitic components.

## B. PCE and Dropout Voltage Measurements

We measured the PCE and  $V_{\text{drop}}$  by sweeping 1)  $V_{\text{REC}}$ ; 2)  $R_L$  connected directly across the rectifier, substituting the regulator; and 3)  $f_c$ . In order to measure the rectifier input current, we connected a small resistor,  $R_{\text{sense}} = 10\ \Omega$ , in series with the rectifier input as a current sensor and differentially measured the voltage across it. The rectifier input power was calculated offline by integrating the instantaneous product of the input current and voltage samples. The output power for the PCE was obtained by measuring the  $V_{\text{REC,RMS}}$ . The peak input voltage,  $V_{\text{IN,Peak}}$ , can be expressed as the sum of  $V_{\text{REC}}$  and  $V_{\text{drop}}$ .

Fig. 14 shows the measured and simulated PCE and  $V_{\text{drop}}$  versus  $V_{\text{REC}}$  with  $C_L = 10\ \mu\text{F}$ ,  $R_L = 500\ \Omega$ , and  $f_c = 13.56\ \text{MHz}$ . All simulated results in this section are postlayout and include the estimated parasitic components of the LQFP176 package (see Fig. 12). Fig. 14(a) shows that for  $V_{\text{REC}} = 3.12\ \text{V}$ , the maximum PCE with both offset-control functions was measured to be 80.2% (curve-b), which was slightly lower than the maximum postlayout simulated PCE of 84.5% (curve-a) and schematic simulated PCE of 87% due to the effects of parasitics and the current sensing resistor. The measured PCE without  $\text{Offset}_F$  (curve-c) is  $\sim 10\%$  lower than the PCE with  $\text{Offset}_F$ . When  $V_{\text{REC}}$  was higher or lower than  $3.12\ \text{V}$ , the PCE gradually decreased because the comparator offsets were only adjusted for  $V_{\text{REC}} = 3.1\text{--}3.2\ \text{V}$ . For other  $V_{\text{REC}}$  values, the comparator offsets can be easily readjusted using CTL0:3 in Fig. 2.

In Fig. 14(b), the measured  $V_{\text{drop}}$  with  $\text{Offset}_F$  (curve-b) shows  $0.7\ \text{V}$  dropout, which is  $0.4\ \text{V}$  higher than the simulated  $V_{\text{drop}}$  with  $\text{Offset}_F$  (curve-a). This is due to the interconnect inductances increasing  $V_{\text{IN1,Peak}}^*$  as explained earlier. For example,  $V_{\text{IN1,Peak}}^*$  was measured  $\sim 250\ \text{mV}$  higher than  $V_{\text{IN1,Peak}}$  in Fig. 12 after shorting  $R_{\text{sense}}$ . By including these parasitic inductors in our simulations ( $L_{\text{bond}} + L_{\text{wire}} = 25\ \text{nH}$ ), we were able to verify the cause of  $V_{\text{drop}}$  variations by producing results (curve-d) that were closer to the measured  $V_{\text{drop}}$  (curve-b).  $V_{\text{drop}}$  is also affected by the output current,  $I_{\text{REC}}$ , and PCE. In Fig. 14(b), a higher  $V_{\text{REC}}$  with fixed  $R_L$  requires higher  $I_{\text{REC}}$  through the rectifier, which generates a larger voltage drop across the rectifying transistors, increasing  $V_{\text{drop}}$ . Furthermore, a rectifier with lower PCE requires more current from the coil to reach a certain  $V_{\text{REC}}$ , which also increases  $V_{\text{drop}}$ . Overall, measured and simulated results clearly showed that  $V_{\text{drop}}$  is reduced by using both offset-control functions.

Fig. 15(a) shows the measured and simulated PCE versus  $R_L$  with  $C_L = 10\ \mu\text{F}$ ,  $V_{\text{REC}} = 3.12\ \text{V}$ , and  $f_c = 13.56\ \text{MHz}$ . As  $R_L$  increases, the rectifier output power for the same  $V_{\text{REC}}$  decreases. Therefore, the rectifier internal power dissipation for switch losses,  $P_{\text{Loss,total}}$ , and comparators,  $P_{\text{comparator}}$ , become more significant in (4) and reduce the PCE. The measured and simulated  $V_{\text{drop}}$  versus  $R_L$  in Fig. 15(b) shows that  $V_{\text{drop}}$  decreases by increasing  $R_L$ . It is because larger  $R_L$  requires smaller  $I_{\text{REC}}$ , leading to smaller voltage drop across the rectifying transistors.



Fig. 16(a) shows the measured and simulated PCE versus  $f_c$  with  $C_L = 10 \mu\text{F}$ ,  $V_{\text{REC}} = 3.12 \text{ V}$ , and  $R_L = 500 \Omega$ . The transistor dimensions and comparator offsets of our rectifier were optimized for operating at 13.56 MHz. Therefore, the PCE decreases at higher frequencies due to the comparator delays. At lower frequencies, the PCE also decreases a little bit since the fixed comparator offset turns off the rectifier earlier. Fig. 16(b) shows the measured and simulated  $V_{\text{drop}}$  versus  $f_c$ . Even though  $I_{\text{REC}}$  is fixed in these experiments, the PCE variation by frequency also affects  $V_{\text{drop}}$ . Therefore, lower PCE at higher frequencies leads to higher  $V_{\text{drop}}$ .

### C. Back Telemetry Measurements

To demonstrate the built-in back telemetry capability of our active full-wave rectifier, we applied a random stream of serial data bits at 500 kbps and  $0.2 \mu\text{s}$  pulse width (10% duty cycle) to the rectifier short-coil (SC) input terminal (see Fig. 2). A pair of planar spiral coils with  $d = 4 \text{ cm}$  were used similar to the setup described in [26] (see Fig. 1 and Table II). The LSK back telemetry data was recovered using a commercial RFID reader ASIC (TRF7960) from Texas Instruments (Dallas, TX). In Fig. 17, measured waveforms from top show the data signal applied to SC, voltages across the load ( $R_L C_L = 500 \Omega || 10 \mu\text{F}$ ), secondary coil ( $V_{\text{IN}1}$ ), primary coil ( $V_{L1}$ ), and recovered serial data bit stream at TRF7960 output, which has  $\sim 1.2 \mu\text{s}$  delay with respect to SC. Shorting  $L_2$  with SC = High in Fig. 1 results in a sudden drop in  $V_{\text{IN}1}$  and increased current in  $L_1$ , which also increases the voltage across  $L_1$  [9]. Current and voltage variations in  $L_1$  are detected by the RFID reader and amplitude shift keying (ASK) demodulated to recover the LSK back telemetry data. It can be seen in Fig. 17 that  $V_{\text{REC}}$  remains constant during the LSK operation because of the large  $C_L$  ( $10 \mu\text{F}$ ) and small SC duty cycle (10%).

### D. Overvoltage Protection Measurements

The OVP circuit is activated when  $V_{\text{REC}}$  increases above a certain threshold voltage,  $V_{\text{threshold}} = 4.4 \text{ V}$ , which is determined by comparing  $0.25 V_{\text{REC}}$  with a reference voltage,  $V_{\text{REF}} = 1.1 \text{ V}$ , generated by the regulator. The comparator in Fig. 1 connects  $C_{\text{ovp}}$  to  $V_{\text{ss}}$  to deviate the resonance frequency of  $L_2 C_2$  from 13.56 MHz and decrease  $V_{\text{IN}1,2}$  as well as  $V_{\text{REC}}$ . Once  $V_{\text{REC}}$  is reduced,  $C_{\text{ovp}}$  is disconnected and the  $L_2 C_2$  can return back to 13.56 MHz, unless  $V_{\text{REC}} > V_{\text{threshold}}$  condition is persistent. This closed-loop mechanism regulates  $V_{\text{REC}}$  around  $V_{\text{threshold}}$  as long as the input voltage is too high without dissipating extra heat within the rectifier. However, the amount of frequency deviation depends on  $C_{\text{ovp}}$  value. To cope with larger input voltages, larger  $C_{\text{ovp}}$  is required. Fig. 18 shows the measured  $V_{\text{REC}}$  versus  $V_{L1}$  for two  $C_{\text{ovp}}$  values. It can be seen that with the frequency deviation resulted from  $C_{\text{ovp}} = 40 \text{ pF}$ , the rectifier can be protected against  $V_{L1}$  up to  $\sim 60 \text{ V}$ , while  $C_{\text{ovp}} = 120 \text{ pF}$  can protect the rectifier against  $V_{L1}$  up to  $\sim 68 \text{ V}$ . In practice,  $V_{L1}$  is often constant and a sudden reduction in  $d$  or  $I_{\text{REC}}$  activates the OVP circuit.

### E. Performance Summary and Comparison

Table I shows the full-wave rectifier benchmarking table, comparing our work with previously reported rectifiers. It can be seen that despite its relatively large feature length process and size, the active rectifier reported here, to the best of our knowledge, provides the highest measured PCE = 80.2% ever reported at 13.56 MHz, thanks to its high speed comparators that are equipped with offset-control functions for both rising and falling edges. With an input peak voltage of 3.8 V, this rectifier can deliver more than 20 mW at  $V_{\text{REC}} = 3.12 \text{ V}$ , which is required for high power IMDs such as the implantable multichannel wireless neural recording and stimulating system that is being developed in our lab [26]. By shortening the connection between  $L_2$  and the rectifier input port when they are both embedded in an IMD and thus reducing the parasitic components shown in Fig. 12, we expect the rectifier PCE to move closer to the simulated level of 87%. Further, migrating to

a smaller feature length process is expected to further improve the PCE and bandwidth by lowering the threshold voltages and comparator delays. Table II summarizes some additional specifications of the rectifier and LDO that are not listed in Table I.

## V. Conclusions

An integrated power-efficient full-wave active rectifier equipped with offset-controlled high speed comparators has been presented for inductively powered applications, such as RFID and IMD. The main switches in this rectifier are driven by a pair of comparators, which keep them closed precisely when  $V_{IN1,2} > V_{REC}$ , while compensating for both turn-on and turn-off propagation delays of the comparators by a pair of programmable offsets. As a result, the rectifier conducts for the maximum possible period of time and delivers maximum forward current to the load, while minimizing the back current.

In addition, the sizes of the rectifying transistors were optimized for minimizing their  $R_{on}$  and switching losses at the rectifier operating frequency. We have reported the highest measured PCE of 80.2% with 3.12 V dc output across a 500  $\Omega$  load from a 3.8 V ac input at 13.56 MHz. The rectifier's built-in LSK back telemetry capability can be utilized for communication, such as establishing a closed loop wireless power transmission system to adjust the transmitted power for a constant rectifier output voltage [27]. The rectifier has also been equipped with a detuning-based overvoltage protection circuit, which is a necessary safety feature for situations in which the rectifier input signal has grown too large as a result of the coils being too close or the load current being too small.

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## Biographies



**Hyung-Min Lee** (S'06) received the B.S. degree in electrical engineering (*summa cum laude*) from Korea University, Seoul, in 2006, and the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2008. Since 2009, he has been with the GT-Bionics lab in the Department of Electrical and Computer Engineering at the Georgia Institute of Technology, Atlanta, where he is working toward the Ph.D. degree.

His research interests include analog/mixed-signal integrated circuits and power management integrated circuits for biomedical implantable systems.

Mr. Lee has received the Silver Prize in the 16th Human-Tech Thesis Prize from Samsung Electronics, Korea, and the Commendation Award in the 4th Outstanding Student Research Award from TSMC, Taiwan, both in 2010.



**Maysam Ghovanloo** (S'00–M'04–SM'10) was born in 1973 in Tehran, Iran. He received the B.S. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1994, the M.S. degree in biomedical engineering from the Amirkabir University of Technology, Tehran, in 1997, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 2003 and 2004, respectively.

From 2004 to 2007, he was an Assistant Professor in the Department of Electrical and Computer Engineering at North Carolina State University, Raleigh. He joined the faculty of the Georgia Institute of Technology, Atlanta, in 2007, where he is currently an Assistant Professor and the founding director of the Georgia Tech Bionics Laboratory in the School of Electrical and Computer Engineering. He has authored or coauthored more than 80 conference and journal publications.

Dr. Ghovanloo is an Associate Editor of the *IEEE Transactions on Circuits and Systems—Part II: Express Briefs* and the *IEEE Transactions on Biomedical Circuits and Systems*. He has received awards in the 40th and 41st Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC) Student Design Contests. He has organized special sessions and was a member of Technical Review Committees for several major conferences, such as ISSCC and ISCAS, in the areas of biomedical circuits, sensors, and systems. He is a member of the Tau Beta Pi, the Sigma Xi, and the IEEE Solid-State

Circuits Society, the IEEE Circuits and Systems Society, and the IEEE Engineering in Medicine and Biology Society.

## Appendix

In this section we derive (2) and (4) for PCE analysis using simplified rectifier waveforms, shown in Fig. 19.  $D$  is the rectifier switching duty cycle,  $D_{\text{charge}}$  is the charging duty cycle,  $T = 1/2f_c$  is the period of the full-wave rectified signal, and  $T_{\text{PHL}}$  and  $T_{\text{PLH}}$  are the delays in high-to-low and low-to-high transitions of the comparator output ( $V_{\text{OUT}}$ ), respectively. In this model, we assume: 1)  $V_{\text{IN}}$  is sinusoidal, 2)  $R_L$  is constant, 3)  $C_L$  is large enough to maintain  $V_{\text{REC}}$  almost constant despite the rectifier operation, and 4) the rising and falling times of the comparator output are negligible compared to  $T$  (or they have been included in  $T_{\text{PHL}}$  and  $T_{\text{PLH}}$ ). The rectifier turns on (i.e., conducts) from  $T_a$  to  $T_d = DT$  and turns off from  $T_d$  to  $T_e = T - DT$ . The assumption is that the additional charge that is stored in  $C_L$  during  $DT$  maintains  $V_{\text{REC}}$  constant while the rectifier is supplying  $R_L$  for the entire period of  $T$ . Therefore,

$$\begin{aligned} \int_{T_a}^{T_d} I_{\text{in}}(t) dt &= \int_{T_a}^{T_d} \left( \frac{V_{\text{IN}}(t) - V_{\text{REC}}}{R_{\text{onp}} + R_{\text{onn}}} \right) dt \\ &= \int_{T_a}^{T_e} \left( \frac{V_{\text{REC}}}{R_L} \right) dt = \frac{V_{\text{REC}}}{R_L} T \end{aligned} \quad (5)$$

where  $T_a = (T - DT + T_{\text{PHL}} + T_{\text{PLH}})/2$ ,  $T_d = (T + DT + T_{\text{PHL}} + T_{\text{PLH}})/2$ , and  $T_e = (3T - DT + T_{\text{PHL}} + T_{\text{PLH}})/2$  are indicated on Fig. 19. The sinusoidal input voltage,  $V_{\text{IN}}$ , can be expressed as

$$\begin{aligned} V_{\text{IN}}(t) &= V_{\text{IN,peak}} \sin\left(\frac{\pi}{T}t\right) \\ &= \frac{V_{\text{REC}}}{\sin\left(\frac{\pi}{T}(T_a - T_{\text{PHL}})\right)} \sin\left(\frac{\pi}{T}t\right). \end{aligned} \quad (6)$$

Using (6) in (5),  $R_{\text{onp}} + R_{\text{onn}}$  can be expressed as a function of  $D$

$$R_{\text{onp}} + R_{\text{onn}} = R_L \left( \frac{\frac{1}{\pi} (\cos(T_a \frac{\pi}{T}) - \cos(T_d \frac{\pi}{T}))}{\sin\left(\frac{\pi}{T}(T_a - T_{\text{PHL}})\right)} - D \right). \quad (7)$$

If  $T_{\text{PLH}} = 0$ ,  $D_{\text{charge}}$  would be the same as  $D$  because the rectifier only supplies  $R_L C_L$  during its conducting period. However, with  $T_{\text{PLH}} > 0$ , the back current can discharge  $C_L$  when  $V_{\text{REC}} > |V_{\text{IN}}|$ . In Fig. 19, the back current from  $T_c$  to  $T_d(D_2T)$  discharges  $C_L$  as much as the forward current from  $T_b$  to  $T_c(D_1T)$  charges  $C_L$ . Therefore,  $D_{\text{charge}}$  can be derived as a function of  $D$  by obtaining  $T_b$

$$\begin{cases} I_{\text{in}} = I_{C_L, \text{charge}} + I_{R_L} & T_b < t < T_c \\ I_{\text{in}} = I_{C_L, \text{discharge}} + I_{R_L} & T_c < t < T_d \end{cases} \quad (8)$$

$$\int_{T_b}^{T_c} I_{C_L, \text{charge}}(t) dt + \int_{T_c}^{T_d} I_{C_L, \text{discharge}}(t) dt = \int_{T_b}^{T_d} \left( \frac{V_{\text{IN}}(t) - V_{\text{REC}}}{R_{\text{onp}} + R_{\text{onn}}} - \frac{V_{\text{REC}}}{R_L} \right) dt = 0. \quad (9)$$

By solving (5)–(9) for  $T_b$  using MATLAB,  $-D_{\text{charge}}$  can be expressed as

$$D_{\text{charge}} = D - \left( \frac{T_d - T_b}{T} \right). \quad (10)$$

Note that even though the input current from  $T_b$  to  $T_d$  does not affect  $V_{\text{REC}}$ ,  $-R_{\text{on}}$  power losses still occur during this period ( $D_1T + D_2T$ ). Therefore, the  $R_{\text{on}}$  loss term with  $D_{\text{eff}}$  in (2) can be represented as

$$\begin{aligned} P_{\text{Loss}, R_{\text{onp}}} + P_{\text{Loss}, R_{\text{onn}}} &= \left( \frac{V_{\text{REC}}}{R_L D_{\text{eff}}} \right)^2 D_{\text{eff}} (R_{\text{onp}} + R_{\text{onn}}) \\ &= \left( \frac{V_{\text{REC}}}{R_L D_{\text{charge}}} \right)^2 D_{\text{charge}} + \left( \frac{1}{D_1 T} \int_{T_b}^{T_c} I_{\text{in}}(t) dt \right)^2 D_1 + \left( \frac{1}{D_2 T} \int_{T_c}^{T_d} I_{\text{in}}(t) dt \right)^2 D_2 (R_{\text{onp}} + R_{\text{onn}}) \end{aligned} \quad (11)$$

where the first, second, and third terms of the right-hand side equation correspond to the  $R_{\text{on}}$  loss during  $D_{\text{charge}}T$ ,  $D_1T$ , and  $D_2T$ , respectively. If  $T_{\text{PLH}} = 0$ , the second and third terms will be eliminated because  $T_b = T_c = T_d$ . Therefore, using (5)–(11), the  $R_{\text{on}}$  loss in (2) can be expressed as a function of  $D$ .

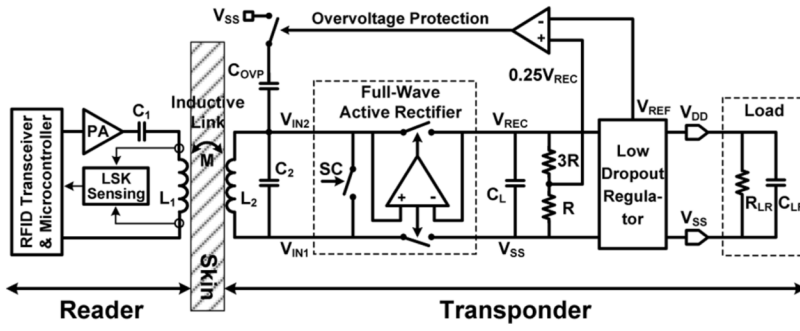
$R_{\text{onp}} + R_{\text{onn}}$  can also be represented as a function of  $W_p = W_n$

$$R_{\text{onp}} + R_{\text{onn}} = \frac{1}{W_p} \left( \frac{L_{\text{min}}}{k_p (V_{\text{REC}} - |V_{\text{Thp}}|)} + \frac{L_{\text{min}}}{k_n (V_{\text{REC}} - V_{\text{Thn}})} \right) \quad (12)$$

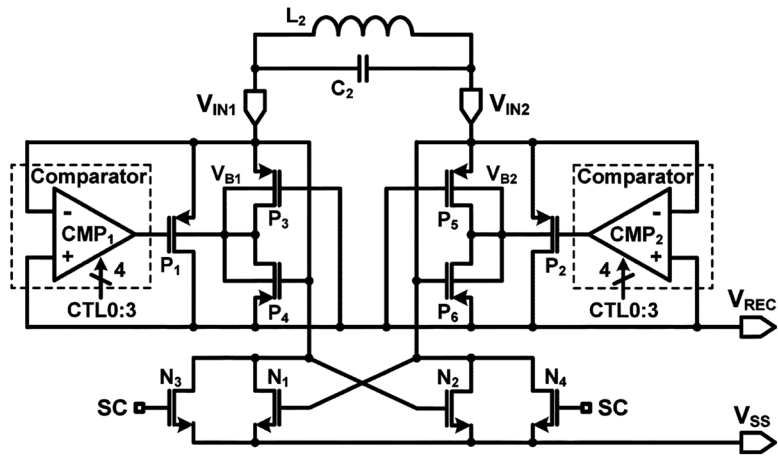
where  $L_{\text{min}}$  is the length of the PMOS and NMOS transistors. By substituting  $W_p$  with (12), the switching loss term,  $P_{\text{Loss}, C_{\text{gp}}}$ , in (2) can be expressed as a function of  $D$

$$P_{\text{Loss}, C_{\text{gp}}} = W_p C_{\text{gp}}^* V_{\text{REC}}^2 2f_c = C_{\text{gp}}^* V_{\text{REC}}^2 2f_c \times \frac{1}{R_{\text{onp}} + R_{\text{onn}}} \times \left( \frac{L_{\text{min}}}{k_p (V_{\text{REC}} - |V_{\text{Thp}}|)} + \frac{L_{\text{min}}}{k_n (V_{\text{REC}} - V_{\text{Thn}})} \right). \quad (13)$$

Therefore, by substituting (11) and (13) in (2) and differentiating it with respect to  $D$ , we can obtain the optimized  $D$  for minimum power loss inside the rectifier. Using the optimal  $D$ , the optimal  $W_p$  can be derived from (7) and (12), and the maximum PCE can be calculated from (4) by minimizing the power loss in (2).

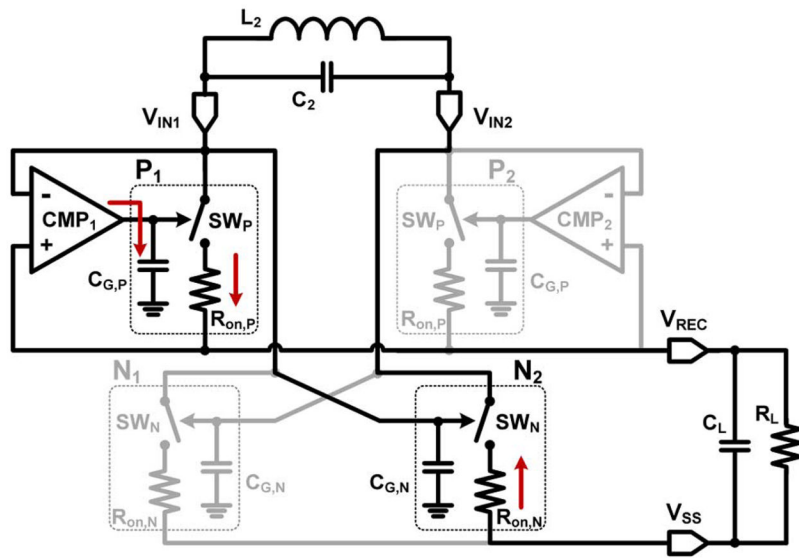


**Fig. 1.** Block diagram of an inductively powered implantable microelectronic device (IMD) with emphasis on the power transmission/conditioning circuitry.

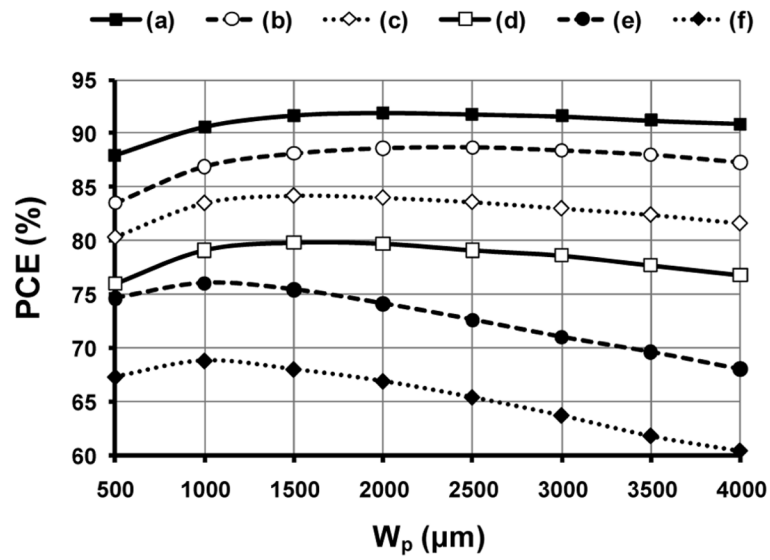


**Fig. 2.** Schematic diagram of our active rectifier including offset-controlled high speed comparators, dynamic body biasing, and load shift keying (LSK) back telemetry functions.

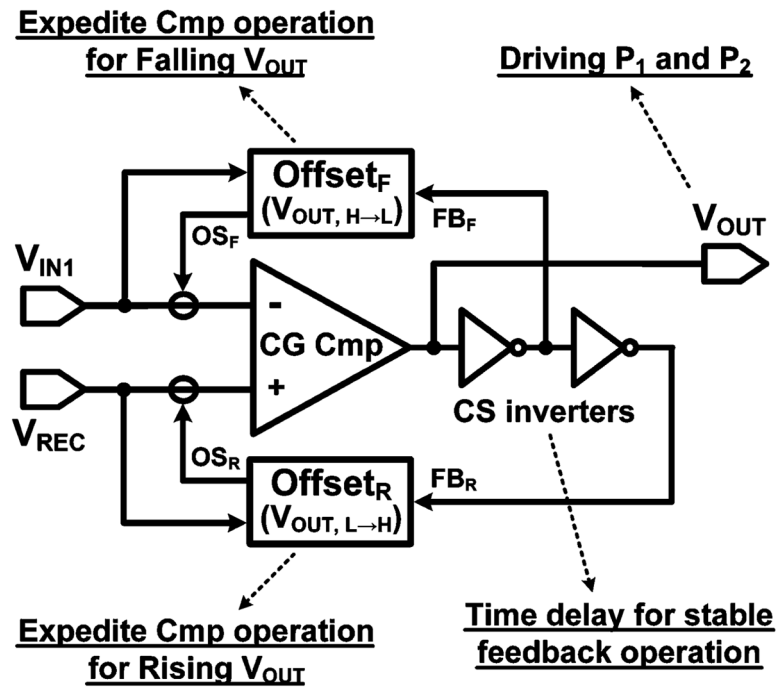




**Fig. 3.** Simplified schematic diagram of the active rectifier depicting the current path and power dissipating components when  $V_{IN1} - V_{IN2} > V_{REC}$ .



**Fig. 4.** Calculated rectifier power conversion efficiency (PCE) versus  $W_p$  depending on the comparator delays when  $V_{\text{REC}} = 3.2$  V and  $R_L = 500$   $\Omega$ . Curve-a:  $T_{\text{PHL}} = 0$  ns and  $T_{\text{PLH}} = 0$  ns; Curve-b:  $T_{\text{PHL}} = 5$  ns and  $T_{\text{PLH}} = 0$  ns; Curve-c:  $T_{\text{PHL}} = 0$  ns and  $T_{\text{PLH}} = 3$  ns; Curve-d:  $T_{\text{PHL}} = 3$  ns and  $T_{\text{PLH}} = 3$  ns; Curve-e:  $T_{\text{PHL}} = 0$  ns and  $T_{\text{PLH}} = 4$  ns; and Curve-f:  $T_{\text{PHL}} = 4$  ns and  $T_{\text{PLH}} = 4$  ns.



**Fig. 5.** Block diagram of the high speed comparator employing offset control functions for both falling and rising  $V_{OUT}$  transitions.

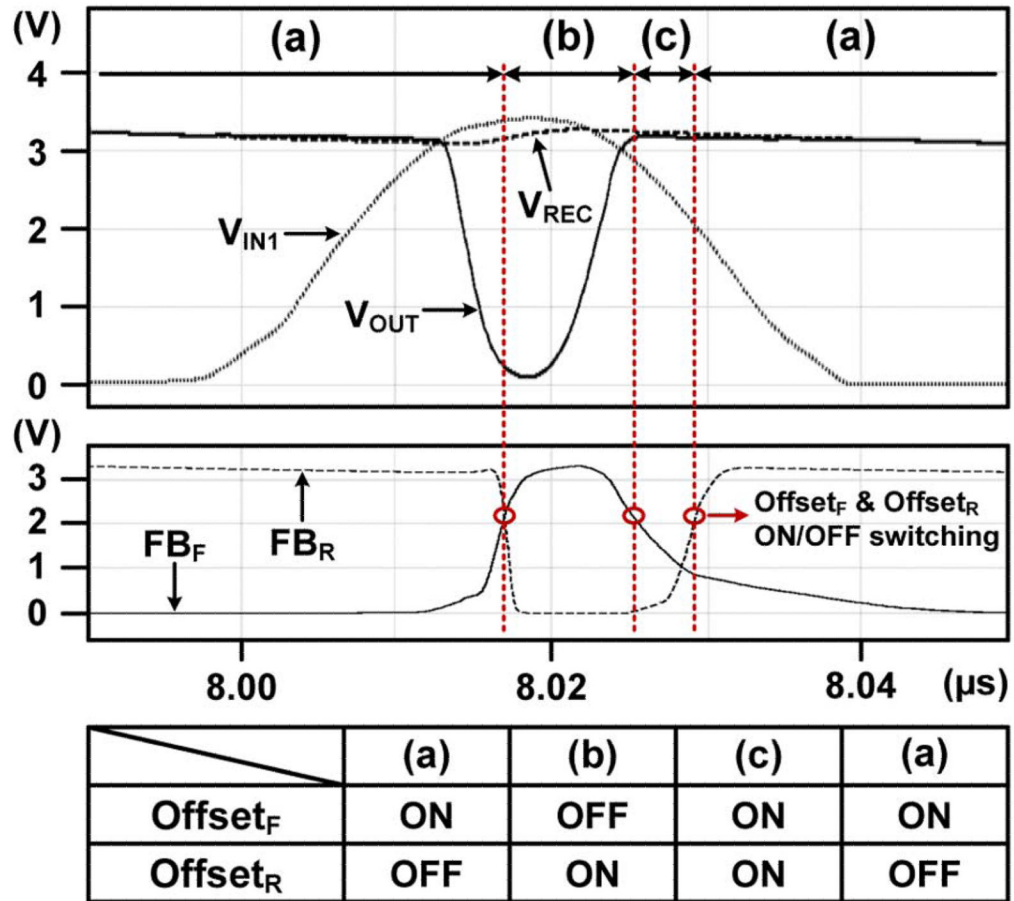
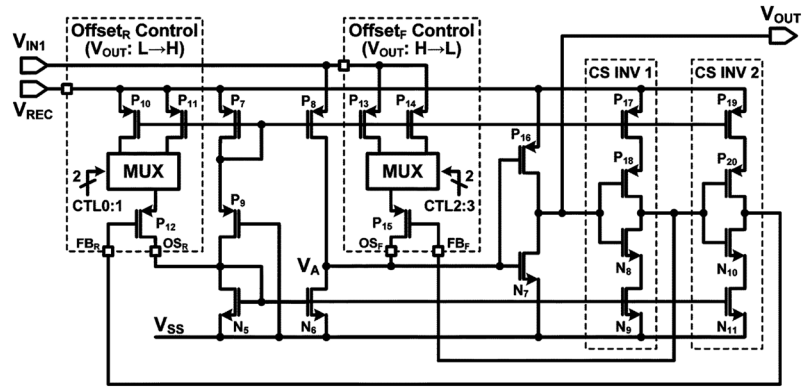
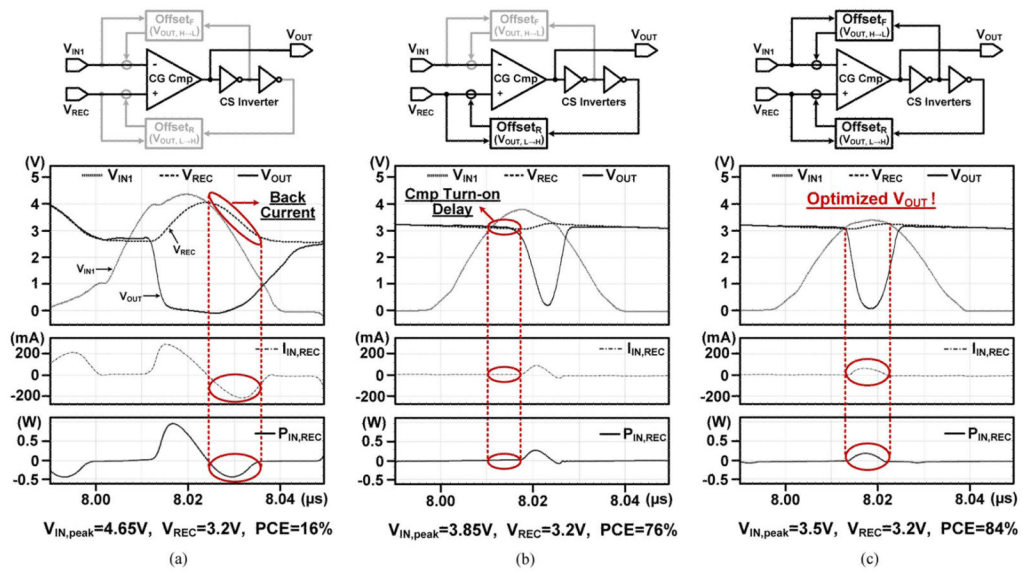


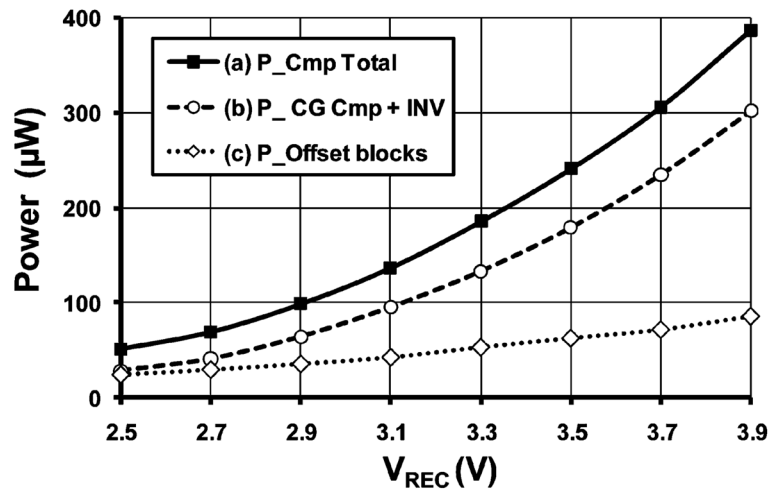
Fig. 6. Simulated waveforms and timing diagram showing the operation of the offset-control blocks in the high speed comparators.



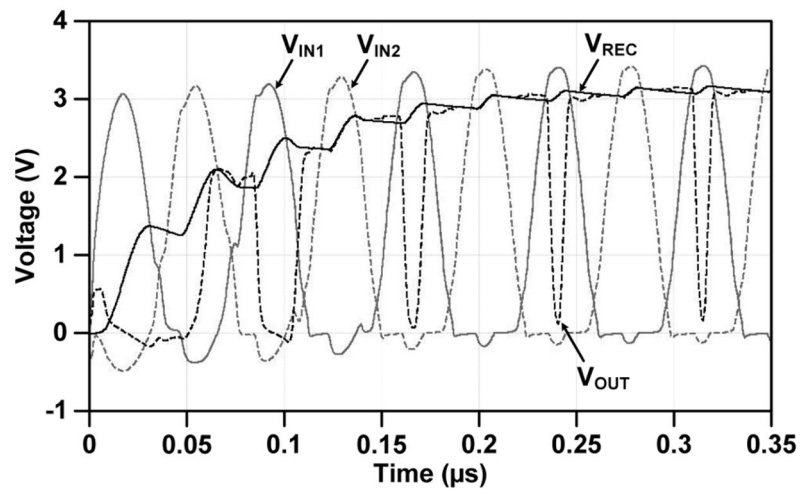
**Fig. 7.** Schematic diagram of the high speed comparator with two offset-control functions,  $Offset_F$  for the  $V_{OUT}$  falling edge and  $Offset_R$  for the  $V_{OUT}$  rising edge.



**Fig. 8.** Simulation results of the active rectifier showing waveforms of the input/output voltages, input current, and input power with  $V_{REC} = 3.2 \text{ V}$  and  $R_L = 500 \Omega$ , (a) without any offset-control function, (b) with only  $Offset_R$  function, and (c) with both  $Offset_F$  and  $Offset_R$  functions.

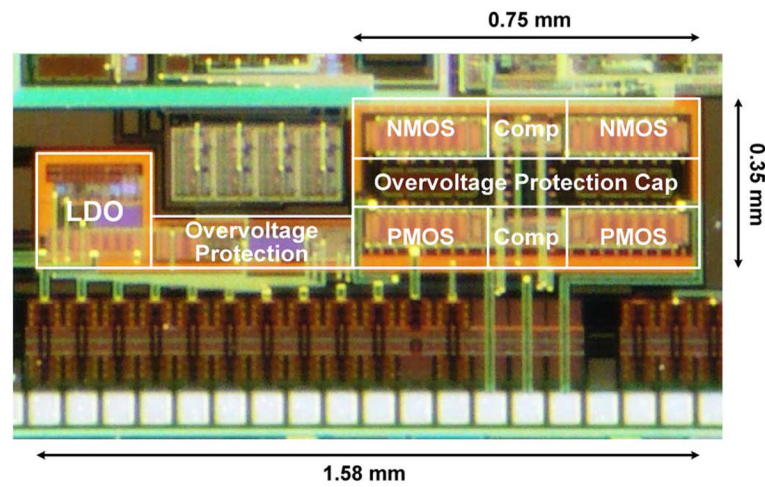


**Fig. 9.** Simulated power consumption of the comparator versus  $V_{REC}$  showing power overheads for employing the offset-control functions ( $f_c = 13.56$  MHz,  $R_L = 500 \Omega$ , and  $C_L = 10 \mu\text{F}$ ). Curve (a) shows the total power consumption of the high speed comparator, (b) is the power consumption of the CG comparator and CS inverters, and (c) indicates the consumption of the offset-control blocks.

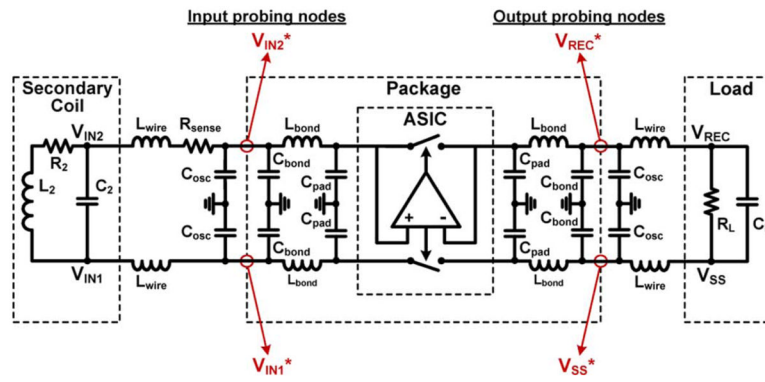


**Fig. 10.** Simulated waveforms for self startup operation of the active rectifier ( $f_c = 13.56$  MHz,  $V_{IN,peak} = 3.4$  V,  $V_{REC} = 3.12$  V,  $R_L = 500$   $\Omega$ , and  $C_L = 2.5$  nF).





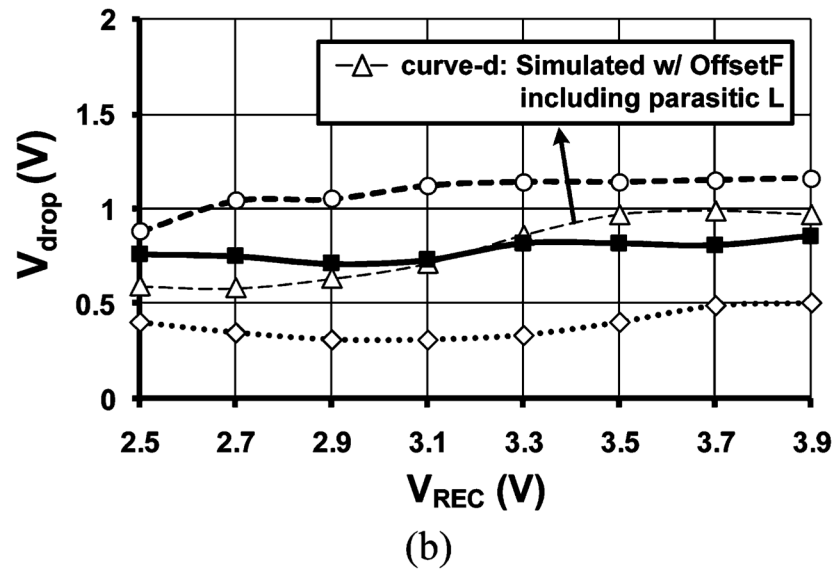
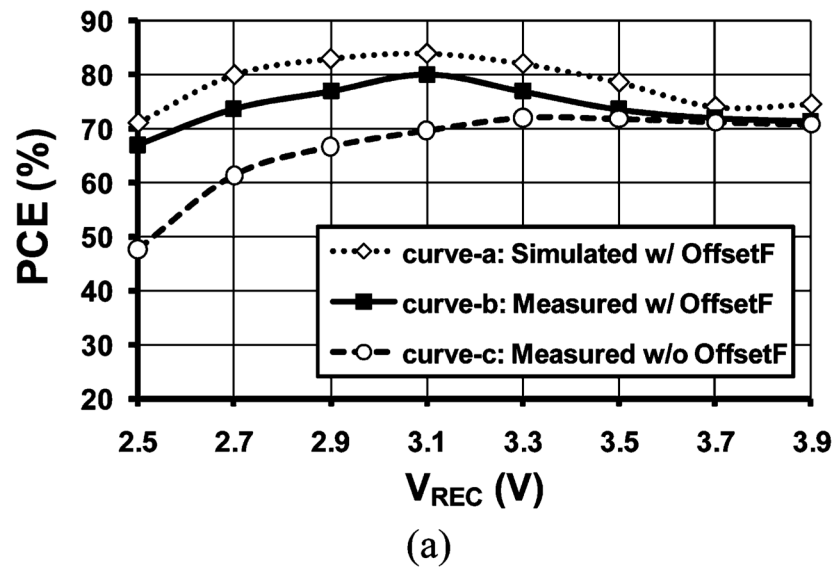
**Fig. 11.** Fabricated chip micrograph and its floor plan, including the active rectifier, overvoltage protection circuit, and low dropout regulator.



**Fig. 12.**

Lumped model of the circuit used in active rectifier simulations, showing capacitive and inductive parasitic components of the wire-bond and external interconnects. It is important to note that because of these parasitics, voltages measured on the coil or load,  $V_{XY}$ , are not exactly the same as those measured on the asic package (lqfp176),  $V_{XY}^*$ .





**Fig. 14.** Measured and simulated (a) PCE and (b)  $V_{drop}$  versus  $V_{REC}$  when  $R_L = 500 \Omega$ ,  $C_L = 10 \mu\text{F}$ , and  $f_c = 13.56 \text{ MHz}$ .

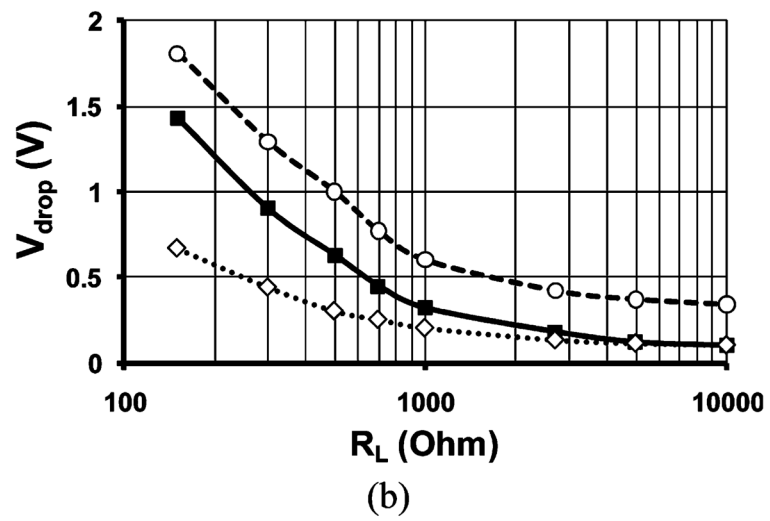
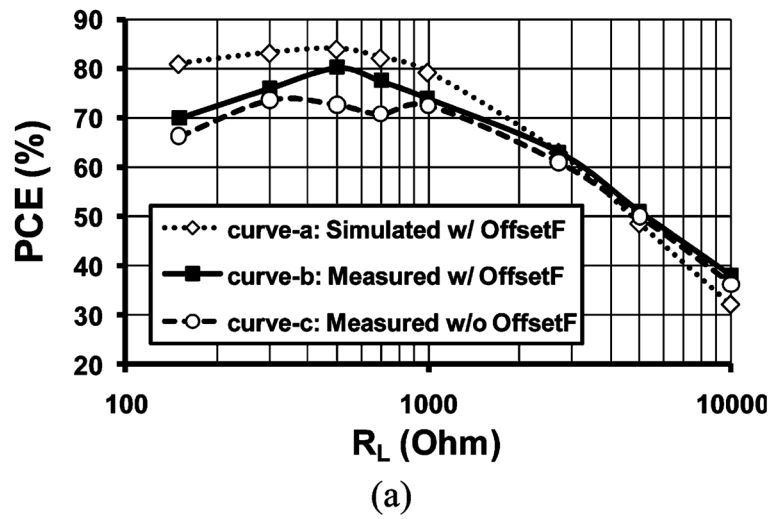
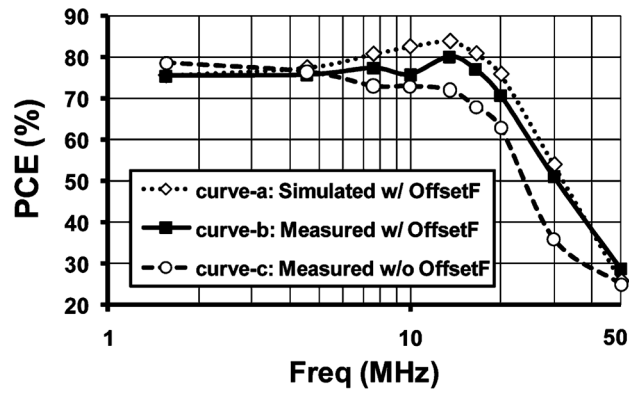
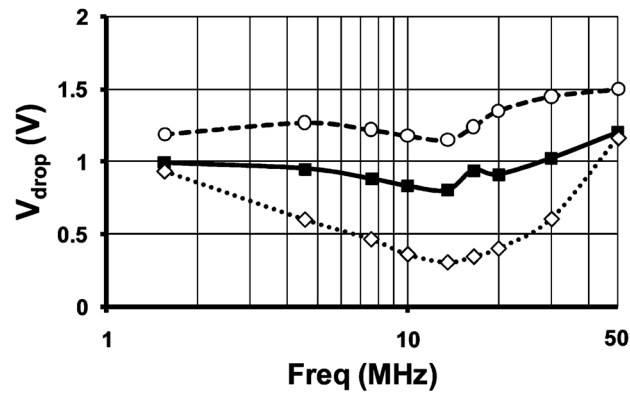


Fig. 15. Measured and simulated (a) PCE and (b)  $V_{drop}$  versus  $R_L$  with  $V_{REC} = 3.12$  V,  $C_L = 10 \mu\text{F}$ , and  $f_c = 13.56$  MHz.

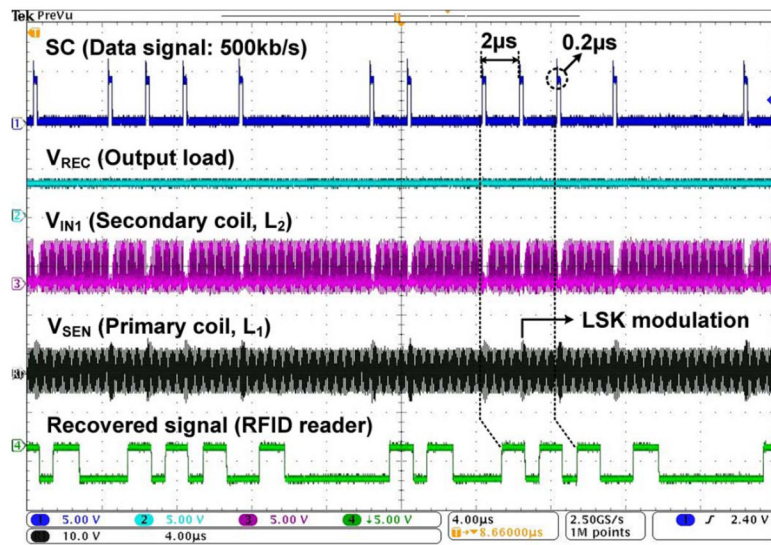


(a)

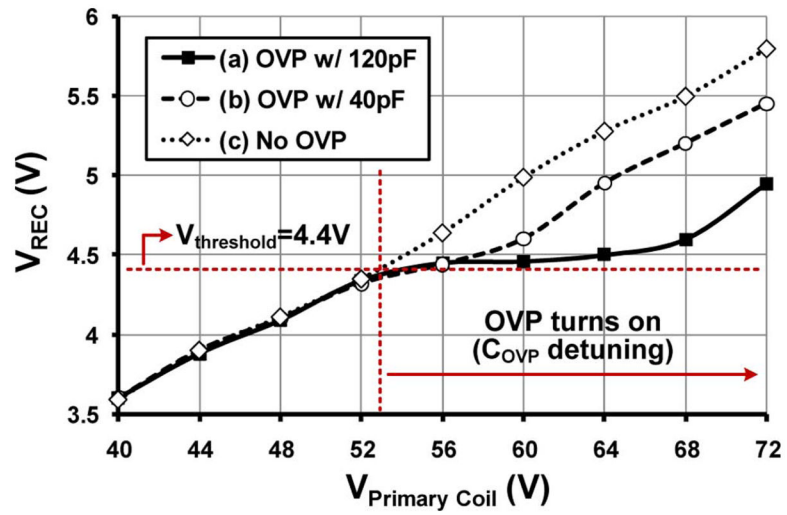


(b)

**Fig. 16.** Measured and simulated (a) PCE and (b)  $V_{\text{drop}}$  versus  $f_c$  with  $V_{\text{REC}} = 3.12$  V,  $C_L = 10$   $\mu\text{F}$ , and  $R_L = 500$   $\Omega$ .



**Fig. 17.** Measured waveforms showing the active rectifier's built-in LSK back telemetry capability through its short-coil (SC) input terminal (data signal = 500 kbps with 10% duty cycle,  $R_L = 500 \Omega$ , and  $C_L = 10 \mu\text{F}$ ). Data was recovered across the primary coil using a commercial RFID reader ASIC (TRF7960, Texas Instruments, Dallas, TX).



**Fig. 18.** Measured  $V_{REC}$  versus primary coil voltage,  $V_{L1}$ , with overvoltage protection (OVP) circuit in Fig. 1 using  $C_{OVP} = 120$  pF (curve-a),  $C_{OVP} = 40$  pF (curve-b), and without overvoltage protection (curve-c) when  $R_L C_L = 500\Omega || 10\mu F$ .





TABLE I

Full-Wave Rectifier Benchmarking

Publication	[28]	2006 [15]	2007 [10]	2008 [16]	2009 [14]	2009 [17]	2009 [18]	This work
Technology	Discrete (1N4148)	0.35 $\mu\text{m}$ CMOS	0.5 $\mu\text{m}$ (Schottky)	0.5 $\mu\text{m}$ CMOS	0.18 $\mu\text{m}$ CMOS	0.18 $\mu\text{m}$ CMOS	0.35 $\mu\text{m}$ CMOS	0.5 $\mu\text{m}$ CMOS
$V_{IN, peak}$ (V)	6	3.5	5	5	0.8	1.25	2.4	3.8
$V_{REC}$ (V)	4.3	3.22	4.2	4.36	1.8	0.96	2.08	3.12
$R_L$ (k $\Omega$ )	1.3	1.8	2.8	1	270	2	0.1	0.5
$f_c$ (MHz)	13.56	13.56	4	0.1~2	13.56	10	0.2~1.5	13.56
Area (mm <sup>2</sup> )	3.08	0.0055	N/A	0.4	0.83	0.86	0.4	0.18
PCE(%)	Simulation	87	N/A	90.4	N/A	N/A	87	87
	Measurement	50	75	84.8	54.9	76	N/A	80.2

TABLE II

## Additional Active Rectifier and LDO Specifications

$V_{ThN}/V_{ThP}$	0.78 V/0.92 V
Nominal rectifier output power	20 mW
Minimum rectifier input voltage	3.2 V (2.9 V <sup>*</sup> )
Ripple rejection capacitor ( $C_L$ )	10 $\mu$ F(ESR=80m $\Omega$ )
Output ripple	80 mV <sub>pp</sub>
Comparator power consumption	135 $\mu$ W <sup>*</sup>
Comparator turn-on delay with Offset <sub>F</sub>	0.75 ~ 1.5 ns <sup>*</sup>
Comparator turn-off delay with Offset <sub>R</sub>	-0.7 ~ 0.5 ns <sup>*</sup>
Primary coil diameter/inductance ( $L_1$ )	16.8 cm/0.88 $\mu$ H
Secondary coil diameter/inductance ( $L_2$ )	3.0 cm/0.41 $\mu$ H
LDO/BGR current consumption	17 $\mu$ A <sup>*</sup> /7 $\mu$ A <sup>*</sup>
LDO output/dropout voltage	3V/150mV
Size of rectifying switches ( $W_p/L_p = W_n/L_n$ )	2100 $\mu$ m/0.6 $\mu$ m
Total area on chip	0.4 mm <sup>2</sup>

<sup>\*</sup> From simulation