High-frequency self-aligned graphene transistors with transferred gate stacks

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Graphene has attracted enormous attention for radio-frequency transistor applications because of its exceptional high carrier mobility, high carrier saturation velocity, and large critical current density. Herein we report a new approach for the scalable fabrication of high-performance graphene transistors with transferred gate stacks. Specifically, arrays of gate stacks are first patterned on a sacrificial substrate, and then transferred onto arbitrary substrates with graphene on top. A self-aligned process, enabled by the unique structure of the transferred gate stacks, is then used to position precisely the source and drain electrodes with minimized access resistance or parasitic capacitance. This process has therefore enabled scalable fabrication of self-aligned graphene transistors with unprecedented performance including a record-high cut-off frequency up to 427 GHz. Our study defines a unique pathway to large-scale fabrication of high-performance graphene transistors, and holds significant potential for future application of graphene-based devices in ultra–high-frequency circuits.

cut-off frequency | transfer gate

Graphene is of considerable interest as a potential new electronic material (1–10). In particular, it has attracted enormous attention for radio-frequency transistor applications owing to its exceptional high carrier mobility, high carrier saturation velocity, and large current density (11–17). However, the fabrication of high-performance graphene transistors is a significant challenge because conventional steps in the device-fabrication process often introduce undesired damage into graphene lattice, degrading its electronic performance or resulting in nonideal device geometry with excessive parasitic capacitance or serial resistance (18–20). The recent development of self-aligned graphene transistors with nanowire gates can address these challenges, and has enabled graphene transistors with the highest intrinsic cutoff frequency—up to 300 GHz (14). Moving forward to the terahertz regime requires high-quality graphene material, damage-free dielectric integration strategy, and self-aligned device layout. The strategy of physical assembling nanowire gate is promising for addressing the latter two problems. On the other hand, the scalability of this approach is complicated by the requirement of unconventional nanowire-assembly processes. Instead of fighting with the difficulty of nanowire assembly, here we report a scalable approach to high-performance graphene transistors by transferring lithographically patterned gate stacks onto graphene as the self-aligned top gate to demonstrate the highest cutoff frequency (up to 427 GHz).

Results and Discussion

Fig. 1 illustrates our approach to fabrication of the self-aligned graphene transistors with transferred gate stacks. A 50-nm gold thin film is first deposited on a Si/SiO_2 substrate by e-beam evaporation. This gold film is served as the sacrificial substrate in the transferring process. Subsequently, we build the (Al_2O_3/Ti/Au) gate stacks on top of the gold film by standard atomic layer deposition (ALD), lithography, and reactive ion etching (RIE) processes (Fig. 1*A* and *B*). The gate sidewall spacer is formed by depositing a thin-layer Al_2O_3 film using ALD approach (Fig. 1*C*), followed by an anisotropic RIE process to etch away unwanted Al_2O_3 film on the top surface of the gate metal and the substrate (Fig. 1*D*). Because of the limited affinity between the sacrificial Au film and the SiO_2 underneath, the fabricated gate stacks are easily peeled off by thermal release tape. Additionally, to facilitate peeling off and releasing, a thin layer of polymer that has glass transition temperature close to the thermal tape–releasing temperature is spin-cast before peeling off the gate stacks. Therefore, the patterned top-gate stacks are sandwiched between the gold layer and the polymer layer for peeling off from the Si wafer (Fig. 1*E*). After Au etching, the gate stacks can be readily transferred onto desired graphene substrate through a thermal releasing process (Fig. 1*F*). Compared to other releasing methods, such as lateral undercut etching of the sacrificial layer underneath, mechanical peeling is much faster and has lower chemical degradation or contamination to the releasing structure. Moreover, the flexible nature of our approach is compatible with roll-to-roll transfer process, demonstrating high potential for printable electronics (21). The chemical vapor deposition (CVD) graphene is grown on copper foil and transferred onto arbitrary substrates, such as silicon, glass, and plastic (22, 23) (see *SI Methods* and Fig. S1). After transferring the gate stacks, external source, drain, and gate connections are formed by conventional lithography and metallization process. Finally, a thin layer of Pd/Au (5 nm/10 nm) is used to form the self-aligned source and drain electrodes, which are separated by the gate spacer dielectrics (Fig. 1*H* and *I*).

The described fabrication approach is intrinsically scalable, and compatible to various substrates, such as silicon, glass, and plastics. As shown in Fig. 2, arrays of self-aligned graphene transistors with uniform device geometry and spacing are demonstrated on glass (Fig. 2*A*) and 300-nm Si/SiO_2 substrate (Fig. 2*B*). Fig. 2*C* shows a SEM image of the top view of an individual self-aligned graphene transistor. The cross-sectional transmission electron microscope (TEM) image shows that the self-aligned source and drain electrodes are well-separated and precisely positioned next to the gate spacer dielectrics (Fig. 2*D*). Because the device performance is essentially determined by the structure of the individual gate stack and the self-aligned source drain electrodes, the relatively large gap between external source drain lead electrodes may not affect the device performance, but rather makes the device more tolerant to the transfer-induced misalignment and distortion of the gate stacks arrangement.

The conventional dielectric integration approach can often introduce substantial defects into graphene lattice and degrade its

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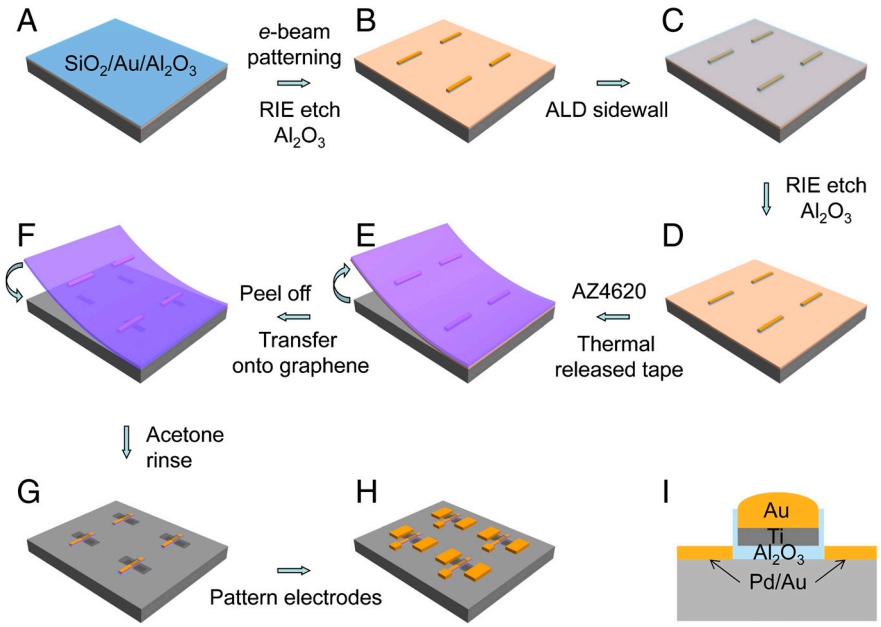

Fig. 1. Schematic illustration of the fabrication of self-aligned graphene transistors with transferred gate stacks. (*A*) A 50-nm gold film is first deposited on a Si/SiO_2 substrate by e-beam evaporation followed by a standard ALD of Al_2O_3 film. (*B*) RIE process is employed to pattern the dielectric strips after standard lithography and metallization process. (*C*) The gate sidewall spacer is formed by depositing a thin-layer Al_2O_3 film using ALD approach. (*D*) An anisotropic RIE process is used to etch away unwanted Al_2O_3 film on the top surface of the gate metal and the substrate. (*E*) A layer of polymer that has glass transition temperature close to the thermal tape–releasing temperature is spin-cast before applying thermal releasing tape and peeling off the gate stacking. (*F*) The patterned top-gate stacks are peeled from the Si wafer. After etching away the gold film, the gate stacks can be readily transferred onto desired graphene substrate through a thermal releasing process. (*G*) Polymer is removed by an acetone rinse, leaving only the gate stacks on top of graphene strips. (*H*) The external source, drain, and top-gate electrodes are fabricated using e-beam lithography, followed by deposition of 5-nm/10-nm Pd/Au metal film to form the self-aligned source and drain electrodes. (*I*) The cross-sectional view of the self-aligned device.

electronic performance (e.g., carrier mobility). To investigate the impact of our transferring method on graphene carrier mobility, we have studied the electrical performance and carrier mobility distribution of more than 20 graphene transistors (in the back-gate configuration) before and after dielectric integration. Here, the CVD-grown graphene is patterned by photolithography with a channel length of approximately 8 μm and a channel width of approximately 8 μm. The effective mobility values are extracted from the drain source current (I_{ds}) versus the back-gated voltage (V_{BG}) (I_{ds}–V_{BG}) curve. Importantly, a histogram of the mobility value shows that the CVD-grown graphene exhibits a similar mobility distribution in the range of 1,000–2,000 $cm^2/V{\cdot}s$ before and after the transfer dielectric integration process (Fig. 3*A*). These studies clearly demonstrate our transfer gate approach does not lead to an obvious degradation of the electronic performance of the graphene.

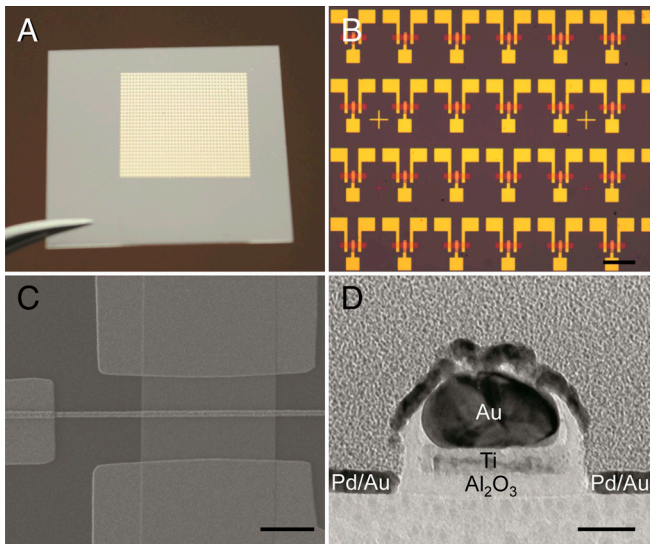

Fig. 2. The self-aligned graphene transistor. (*A*) Photo image of large-scale self-aligned devices with transferred gate stacks on glass substrate. (*B*) Optical image of self-aligned graphene transistors on 300-nm SiO_2/Si substrate. Scale bar, 100 μm. (*C*) SEM image of a graphene transistor with transferred gate stack. Scale bar, 2 μm. (*D*) Cross-sectional TEM image of the overall device layout. Scale bar, 30 nm.

Fig. 3*B–F* depicts the room-temperature electrical transport characteristics of the self-aligned graphene transistors. Before characterizing the transistor properties of our self-aligned devices, gate leakage current (I_{gs}) from the gate stack to the underlying graphene is measured from −4-V to 4-V gate voltage, which indicates the gate leakage current is negligible during the measurement (Fig. S2). Fig. 3*B* shows the I_{ds}–V_{ds} output characteristic of a 300-nm channel-length self-aligned graphene transistor at various gate voltages. The maximum scaled on-current of 1.73 $mA\,\mu m^{-1}$ can be achieved at $V_{ds} = -1V$ with slight current saturation. The current saturation is desirable for the power gain performance in radio-frequency (rf) graphene transistors (10).

The I_{ds}–V_{TG} curve of the same device is measured at different drain bias from 100 mV to 600 mV, with the top-gate voltage sweeps from 0 V to 3 V (Fig. 3*C*). It shows a typical characteristic of *p*-type doping with the Dirac points located at positive top-gate voltage, and can be attributed to oxygen doping that occurred during the growth or transfer processes (10). Overall, the hole-transport branch can switch from saturation current to Dirac point within 2 V of top-gate voltage sweeping, indicating a strong top-gate capacitance coupling. In general, these top-gated self-aligned graphene transistors exhibit a very small I_{ds}–V_{TG} hysteresis of approximately 0.1 V or less, demonstrating the relatively clean nature of the graphene–dielectric interface (Fig. S3). A suppression of electron transport branch is observed in the I_{ds}–V_{TG} transfer curves. This electron-hole asymmetry commonly originates from the misalignment between the work function of con-

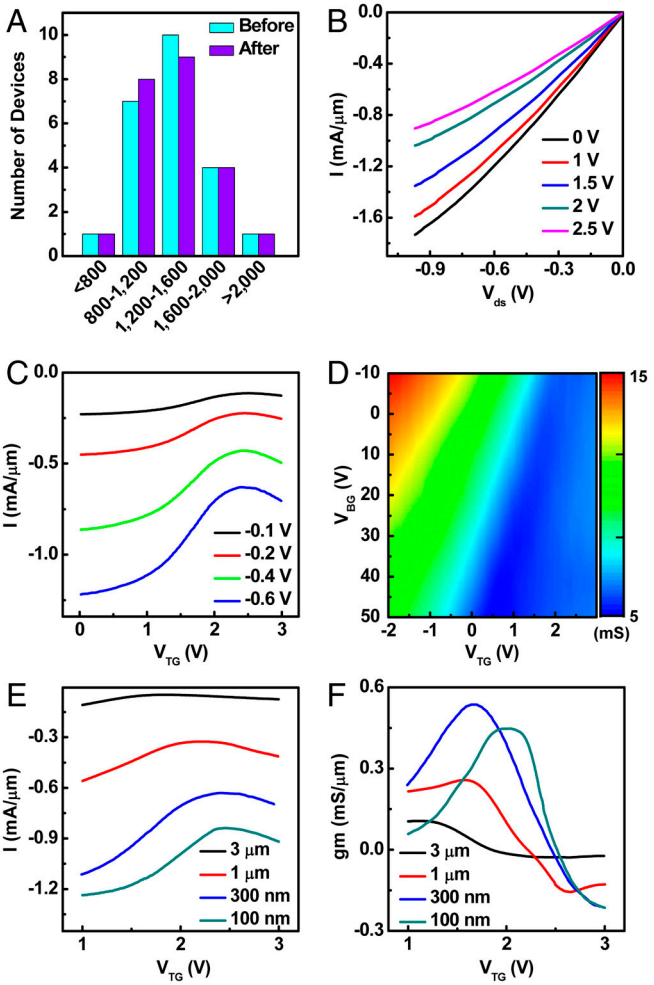

Fig. 3. Room-temperature dc electrical characteristics of the CVD graphene transistors with transferred gate stacks. (*A*) The distribution of device mobility before and after the dielectric transfer process. (*B*) I_{ds}–V_{ds} output characteristics at various gate voltages (V_{TG} = 0, 1, 1.5, 2.0, and 2.5 V) for a 300-nm channel-length self-aligned device. (*C*) The transfer characteristics at different bias voltage for the 300-nm channel-length self-aligned device (V_{ds} = −0.1, −0.2, −0.4, and −0.6 V). (*D*) Two-dimensional plot of the device conductance for varying V_{BG} and V_{TG} biases for the self-aligned graphene device. (*E*) Transfer characteristics of self-aligned graphene transistors at V_{ds} = −0.6 V with channel lengths of 3 μm, 1 μm, 300 nm, and 100 nm. The channel width is 5 μm for all devices. (*F*) The corresponding transconductance of the devices shown in Fig. 3*E* at V_{ds} = −0.6 V.

tact electrodes and the neutrality point of the graphene channel (24). A trend of negative shift of Dirac point is observed with increasing drain voltage. This can be explained by the fact that the Dirac point will shift by $1/2\Delta V_{ds}$ with a change of bias voltage ΔV_{ds}, caused by the relative potential between the gate and drain (25, 26).

In order to characterize the gate capacitance, the conductance of one graphene transistor with 300-nm channel length and 22-nm dielectric thickness is measured as a function of both top-gate voltage (V_{TG}) and back-gate voltage (V_{BG}) (Fig. 3*D*). The ratio between the top-gate and back-gate capacitance is extracted from the slope of the linear shift trajectory of the Dirac point as a function of both the top-gate and back-gate voltage, which gives a value for C_{TG}/C_{BG} of about 29. For 300-nm SiO_2, the back-gate capacitance is $C_{BG} = 11.5\ \mathrm{nF\,cm^{-2}}$; therefore, the estimated top-gate capacitance is $C_{TG} = 334\ \mathrm{nF\,cm^{-2}}$ (27), which is consistent with the result obtained from geometry-based finite-element calculations ($C_{TG} = 359\ \mathrm{nF\,cm^{-2}}$) (Fig. S4).

Fig. 3*E* shows the I_{ds}–V_{TG} transfer curves of several devices with variable self-aligned gate length ranging from 3 μm to 100 nm. With decreasing channel length, a general trend of positive shift of Dirac point and decrease of on/off ratio is observed, which can be explained by short-channel effect (25): In short-channel device, the off-state energy barrier is strongly affected by drain voltage, and thus increases the off-state current and requires higher gate voltage to turn off the channel. Fig. 3*F* shows the extracted transconductance, $g_m = |dI_{ds}/dV_{TG}|$, for devices with different channel length. The peak transconductance at bias of 600 mV increases from 0.11 mS/μm (L = 3 μm) to 0.53 mS/μm (L = 300 nm). However, a further shrinkage of channel length to 100 nm leads to a reduction of transconductance to 0.45 mS/μm, which may be explained by the short-channel effect with less effective gate modulation when the channel length is becoming comparable with the gate dielectric thickness (25). Moreover, the occurrence of Klein tunneling in ultra–short-channel device makes the short-channel effect worse (28–31).

The above discussion clearly demonstrates that our self-aligned graphene transistors with transferred gate stacks exhibit excellent dc performance. To further determine the cutoff frequency (f_T) of our devices, we carried out the on-chip microwave measurements with an Agilent 8361A network analyzer in the range of 50 MHz–30 GHz. The graphene transistors for rf measurement are fabricated on glass substrate in order to minimize the parasitic pad capacitance. To assess accurately the intrinsic f_T value, careful de-embedding procedures are performed using the exact pad layout as "open," "short," and "through" structures on the same chip. The de-embedded S parameters constitute a complete set of coefficients to describe intrinsic input and output behavior of graphene transistors.

Fig. 4*A* shows the small-signal current gain $|h21|$ extracted from the measured S parameters at V_{TG} = 1.5 V and V_{ds} = 0.6 V in a 220-nm channel-length graphene transistor. The curve shows a typical $1/f$ frequency dependence expected for an ideal field-effect transistor. The linear fit yields a f_T value of 57 GHz

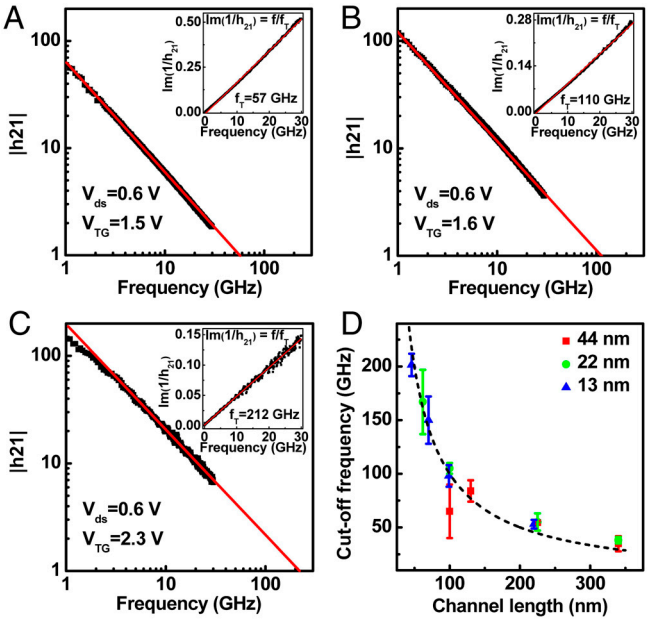

Fig. 4. Radio-frequency performance of self-aligned CVD graphene transistors. (*A*–*C*) Small-signal current gain $|h21|$ versus frequency for three devices with a channel length of (*A*) 220 nm, (*B*) 100 nm, and (*C*) 46 nm at room temperature. The cutoff frequencies are 57 GHz, 110 GHz, and 212 GHz, respectively, at a dc bias of 0.6 V. (*Inset*) Linear fitting using Gummel's method, showing extraction of cutoff frequencies identical to the value obtained in the main panel for each device. (*D*) Peak f_T as a function of gate length from over 40 devices with three different dielectric thicknesses.

for this particular device (Fig. 4*A*), which is also verified by using Gummel's approach (Fig. 4*A*, *Inset*). To further probe the limit of the frequency response, we have fabricated graphene transistors with smaller channel lengths. Fig. 4*B* and *C* show the result extracted from another two self-aligned graphene transistors with 100-nm and 46-nm channel length. The cutoff frequency is $f_T =$ 110 GHz and $f_T = 212$ GHz, respectively. After the rf measurement, we have carefully analyzed the S parameters for all three devices. The device component values (including gate-source capacitance, gate-drain capacitance, transconductance, source resistance, and drain resistance) derived from the rf measurements are consistent with those obtained from the dc measurements and finite element simulations (Table S1), demonstrating the validity of the rf measurements and the de-embedding procedures.

In addition to f_T, maximum oscillation frequency (f_{MAX}), defined as the frequency at which the power gain is equal to one, is another important parameter for rf characteristics. The power-gain performance plot shows a device with 220-nm channel length exhibits a high f_{MAX} of 29 GHz, and a 46-nm device shows a value of 8 GHz (Fig. S5). Because f_{MAX} highly depends on f_T, gate resistance, and source drain conductance, it does not always scale with channel length. The f_{MAX} value of the devices can be further improved by increasing graphene quality, reducing gate resistance, and increasing source drain current saturation.

To investigate further the reproducibility of our approach and examine the length-scaling relationship, we examined more than 40 graphene transistors of variable channel lengths (L) and dielectrics thicknesses. In general, the peak cutoff frequencies follow $1/L$ dependence, which is consistent with previous studies (16). Although $1/L^2$ dependence was observed in longer-channel devices (32), the dominance by contact resistance and degradation of transconductance in short-channel transistors leads to $1/L$ dependence of the cutoff frequency (16). For devices with dielectric thickness of 44 nm, the cutoff frequency falls beneath the $1/L$ trend when the channel length shrinks to 100 nm. This phenomenon can be attributed to the short-channel effect (25), in which the gate modulation is less effective when the channel length is reduced to be nearly comparable with gate dielectric thickness. This short-channel effect can be improved by using thinner dielectric thickness (e.g., 22 nm and 13 nm) (Fig. 4*D*).

The cutoff frequency of our self-aligned devices shows a significant improvement over previously reported CVD graphene transistors of comparable channel length (e.g., f_T of approximately 212 GHz for a 46-nm device in our approach vs. 155 GHz for a 40-nm device reported previously). Nonetheless, the performance of these devices is still far from those obtained from peeled graphene (14, 16), which suggests that the ultimate performance of our devices here is limited by the quality of CVD graphene rather than the fabrication process. To demonstrate that our approach is applicable for higher-performance devices, we have studied the self-aligned transistors on peeled graphene. The devices are fabricated on highly resistive Si substrate with 300-nm SiO_2 because of the difficulty in visualizing the peeled graphene on glass substrate. To assess accurately the intrinsic f_T value, careful de-embedding procedures are performed using the identical pad layout as "open," "short," and "through," structures on the same chip, following a previously established approach (14). Importantly, electrical characterization shows graphene transistors with substantially higher cutoff frequency can be obtained in this way. The I_{ds}–V_{TG} transfer of a 67-nm device shows that a maximum scaled on-current of 3.56 mA/μm and a peak scaled transconductance of 1.33 mS/μm is obtained at $V_{ds} = 1$ V (Fig. 5*A*). Fig. 5*B* shows the small-signal current gain $|h21|$ of a 67-nm channel-length graphene transistor with a typical $1/f$ frequency dependence and an extracted f_T value of 427 GHz at $V_{ds} = 1.1$ V (Fig. 5*B*, *Inset*). Additionally, an f_T value of 169 GHz can be obtained at $V_{ds} = 0.4$ V, indicating a linear trend of f_T value with source drain voltage. The 427-GHz f_T value represents the highest f_T value reported for any graphene transistors to date. We believe the rf performance of our device can be further improved by minimizing the contact resistance or decreasing the gate dielectric thickness to improve gate coupling.

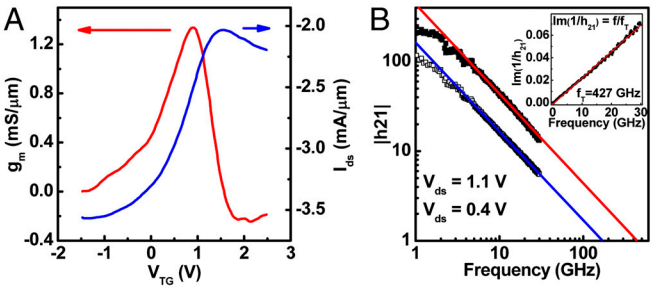

Fig. 5. Room-temperature dc and rf characteristics of the self-aligned peeled graphene transistor with transferred gate stacks. (*A*) The transfer characteristics and corresponding transconductance at a dc bias voltage of 1 V for the 67-nm channel-length self-aligned peeled graphene device. (*B*) Small-signal current gain |*h*21| versus frequency for the 67-nm peeled graphene device under two different dc bias voltages. The cutoff frequency is 427 GHz for 1.1-V bias (solid block) and 169 GHz for 0.4-V bias (open block). (*Inset*) Extraction of f_T by Gummel's method.

Conclusions

In summary, we have developed a scalable method to fabricate self-aligned graphene transistors on glass with transferred gate stacks. With a damage-free transfer process and self-aligned device structure, the fabricated graphene transistors exhibit the highest cutoff frequency to date (427 GHz). By processing conventional lithography, deposition, and etching steps on a sacrificial substrate before integrating with large-area CVD-grown graphene, this approach defines a pathway to scalable fabrication of high-speed self-aligned graphene transistor arrays on arbitrary substrate.

Methods

The detailed description of the device-fabrication process is described here and in *SI Text*. Both the dc and rf transport studies are conducted with a probe station at room temperature (25 °C) under ambient conditions. The on-chip microwave measurements are carried out in the 50-MHz–30-GHz range using an Agilent 8361A network analyzer. The scattering parameters measurements are de-embedded using specific "short" and "open" structures with identical layouts to exclude the effects of the parasitic capacitance, resistance, and inductance associated with the pads and connections. The "through" calibration was done with the exact pad layout (with the gate shorted to the drain), and the "load" calibration was done with the standard calibration pad.

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