



A stable solution-processed polymer semiconductor with record high-mobility for printed transistors

SUBJECT AREAS:
MATERIALS CHEMISTRY
POLYMER CHEMISTRY
APPLIED PHYSICS
ELECTRONIC DEVICES

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Received
20 August 2012

Accepted
21 September 2012

Published
18 October 2012

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Microelectronic circuits/arrays produced via high-speed printing instead of traditional photolithographic processes offer an appealing approach to creating the long-sought after, low-cost, large-area flexible electronics. Foremost among critical enablers to propel this paradigm shift in manufacturing is a stable, solution-processable, high-performance semiconductor for printing functionally capable thin-film transistors — fundamental building blocks of microelectronics. We report herein the processing and optimisation of solution-processable polymer semiconductors for thin-film transistors, demonstrating very high field-effect mobility, high on/off ratio, and excellent shelf-life and operating stabilities under ambient conditions. Exceptionally high-gain inverters and functional ring oscillator devices on flexible substrates have been demonstrated. This optimised polymer semiconductor represents a significant progress in semiconductor development, dispelling prevalent skepticism surrounding practical usability of organic semiconductors for high-performance microelectronic devices, opening up application opportunities hitherto functionally or economically inaccessible with silicon technologies, and providing an excellent structural framework for fundamental studies of charge transport in organic systems.

Solution-processable or printable organic semiconductors have been extensively explored for use in printing organic thin-film transistor (OTFT) arrays and circuits for novel electronic applications^{1–9}. The expectation lies in ultra low-cost fabrication of large-area semiconductor devices via high-throughput printing to impart significant manufacturing economic advantage^{8,9}. This would enable a new generation of low-cost, large-area flexible electronics otherwise unachievable with traditional silicon technologies^{7–9}. Great strides have been made over the last decade in the development of printable organic semiconductors^{10–19} with field-effect transistor (FET) mobility in some cases exceeding those of hydrogenated amorphous silicon semiconductors (α -Si:H; mobility $\sim 0.5–1.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$; on/off ratio $\sim 10^6–10^8$)⁶, but major technical difficulties persist and hamper technology translation to commercialization. Specifically, organic single crystals^{10–14} with FET mobility over $10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are beset with either high air sensitivity or complex and elaborate processing conditions, etc. to be suitable for ambient high-speed printing. On the other hand, polymer semiconductors that can be solution-processed or printed suffer from a number of difficulties including air sensitivity, insufficient mobility, poor FET characteristics, and short lifetime limitations^{15–19}. Most recently, advances in materials design have led to achievement of FET mobility to $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and beyond for solution-processed polymer semiconductors^{20–28}. However, the mobility of printed semiconductors (e.g. via inkjet printing), from our experience, has often been a factor of two or more lower, and the current mobility is thus not sufficient for broad-based, high-value applications (e.g. radiofrequency identification tags, switching backplanes for video displays, etc.). Accordingly, solution-processable semiconductors with consistent FET mobility in greater excess of $2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and current on/off ratio of at least 10^6 in addition to other desirable FET properties, processing, operational, and lifetime stabilities would be required for transitioning printed electronics from laboratory to marketplace.

In an effort to drive mobility of solution-processed polymer semiconductors to significantly beyond the current levels, we had focused our investigation on conjugated alternating electron donor–acceptor (D–A) polymers. A conjugated alternating D–A polymer offers the feasibility of creating a ground-state partial charge-transfer state

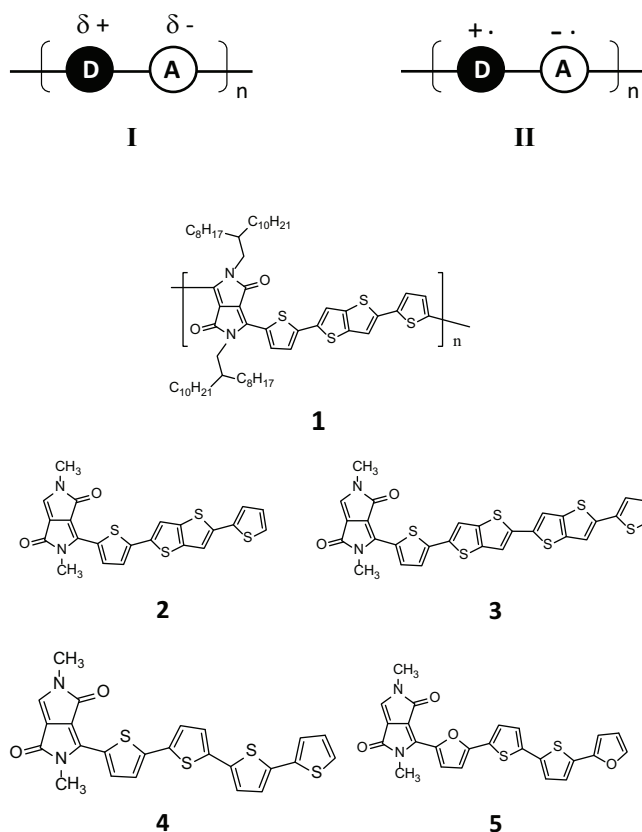


Figure 1 | Schematic ground-state partial charge-transfer State I, biradical anion-cation State II and structures of polymer 1 and D-A model monomers for computational analysis.

as schematically described by I (Fig. 1). This is reminiscent of n- and p-doping of silicon to achieve effective n- and p-type semiconductor properties with appropriate donor and acceptor dopants. A weakly polarized state I would help induce and promote charge injection at the electrode/semiconductor interface, and facilitate charge carrier transport in the semiconductor after charge injection, thus greatly boosting effective charge transport efficiency (see Supplementary, Fig. S1).

The charge transport efficacy of a conjugated alternating D–A polymer would be dictated by, among other factors such as intrinsic charge transport capabilities of donor and acceptor moieties, molecular ordering, etc., the extent of ground-state charge transfer. The latter can be modulated by the relative donor and acceptor strengths and nature of π -conjugation within the polymer framework. To maintain semiconductor properties, the donor and acceptor strengths need to be properly adjusted to prevent extensive ground-state charge transfer to the biradical anion-cation or intramolecular polaron-pair state II (Fig. 1) where formal charge separation occurs. State II would be a conducting state much like the intermolecular charge-transfer complexes, TCNQ–TTF²⁹ and PEDOT/PSS³⁰, to name a few.

Conjugated D–A polymers are fundamentally ambipolar transport semiconductors with the majority carriers being determined by the relative strengths of their donor and acceptor components, i.e. stronger donor leads to predominantly hole transport while stronger acceptor, electron transport. Thus, a suitable molecular set-up for creating state I would be a D–A polymer with a strong donor and a comparatively weak acceptor or vice versus for creating respectively a p-channel or n-channel semiconductor. In addition, a polymer with a relatively planar backbone structure, which promotes closer π – π stacking of polymer chains, would be ideal as tighter π – π stacking

would be conducive to charge transport by hopping³¹. In line with these considerations, we had studied conjugated alternating D–A polymers of a relatively strong donor moiety, dithienylthieno[3,2-b]thiophene (DTT) and a comparatively weaker acceptor moiety, N-alkyl diketopyrrolo-pyrrole (DPP) for p-type semiconductor design. There have been many recent reports on conjugated DPP-based D–A polymer semiconductors having a wide range of mobility from a low of 0.1 cm² V⁻¹ s⁻¹ to a high of approaching 2 cm² V⁻¹ s⁻¹, with most being around 1 cm² V⁻¹ s⁻¹^{22–28}. Through synthesis and processing optimizations, we found that, a simple DPP-DTT-based conjugated polymer, **1** (see Fig. 1), could be rendered to exhibit extremely high hole mobility to over 10 cm² V⁻¹ s⁻¹, together with high current on/off ratio of $\geq 10^6$ and drain current on the order of mA — a world record for a stable, solution-processed polymer semiconductor. The observed mobility was at least an order of magnitude higher than the values of about 1 cm² V⁻¹ s⁻¹ recently reported^{23,25}, and one to two orders of magnitude higher than those of α -Si:H⁶. More importantly, excellent FET performance consistency and ambient, cyclic and lifetime stabilities for over one year have been demonstrated by semiconductor **1**. Experimental high-gain PMOS-like inverters and functional PMOS-oscillator devices have been successfully fabricated on flexible substrates. These latest advances in ambient stable, solution-processed semiconductor development would open up application opportunities never before considered possible (e.g. ultra low-cost identification tags and smart labels, pixel driver backplanes for large-area OLED, etc.). High-mobility semiconductor **1** will also serve as a strategic model compound for theoretical studies to challenge current understanding of phonon-assisted charge transport in organic systems.

Results

Our confidence in **1** as a high-mobility semiconductor was driven and supported by molecular modeling and simulation studies. We found that the guidance provided by proper modeling studies was particularly important in organic semiconductor development as their FET performance vary significantly even for the same molecular structure, depending on such variables as synthetic and processing conditions (synthetic methodology, purification process, molecular weight, etc.) and fabrication methodologies.

Modeling and simulation studies. Four DPP-based D–A monomer units, namely **2** through **5** (Fig. 1), varying in their electron donor components were investigated as model compounds to gain insights into the charge transport properties of their polymeric forms (e.g. **1** from **2**) using nonadiabatic Marcus charge transfer theory^{32,33}. The rate of charge transport between neighboring molecules, Γ , is dictated by both reorganization energy (E) and coupling matrix element (U) as described by the following equation:

$$\Gamma = \frac{U^2}{h} \left(\frac{\pi}{Ek_B T} \right)^{1/2} \exp \left(- \frac{E}{4k_B T} \right) \quad (1)$$

where k_B is the Boltzmann constant and T is the temperature (298.15 K in this study). We first calculated the diffusion coefficient from the hopping rate between two interacting D–A molecules as expressed in Eq. (1), and used Einstein relation to convert the diffusion coefficient to drift mobility at 298.15 K (Supplementary Table S1). The electronic structure calculations of different charge states of D–A molecules were employed to calculate the reorganization energy, which is associated with structural adjustment needed for charge transport. The geometry changes upon charge perturbation in C–C bond lengths were all on the order of 0.031 Å, leading to smaller reorganization energy for more efficient charge transport. The coupling matrix was highly dependent on orbital overlap and decreased with increasing intermolecular π – π stacking distance between two interacting D–A molecules, especially in the region

Table 1 | Synthetic conditions and resulting molecular weights of **1**

Catalyst (stoichiometry)*	Reaction Temp [§] (°C)	M _n (g mol ⁻¹) [†]	M _w (g mol ⁻¹) [†]
Pd(Ph ₃ P) ₄ (4 mol % eq.)	120	29,000 (320,000) [‡]	91,000 (840,000) [‡]
Pd ₂ (dbda) ₃ / P(tolyl) ₃ (2/8 mol % eq.)	120	71,000	344,000
Pd ₂ (dbda) ₃ / P(tolyl) ₃ (2/8 mol % eq.)	130	110,000	501,000

*Catalyst stoichiometry against monomers.

[§]Reaction conducted in chlorobenzene.[†]Molecular weight numbers obtained using high-temperature GPC at 160 °C with 1,2,4-trichlorobenzene as eluent.[‡]Molecular weight numbers obtained using room-temperature GPC with THF as eluent.

where π - π distance was larger than 3.30 Å (Supplementary Fig. S2a). This is because the orbitals of molecules couple more effectively when they are closer to each other. For **2**, when the π - π distance was shorter than 3.30 Å, the coupling matrix element reached the highest level of 0.273 eV. To compare the coupling strengths among four D-A compounds, **2** through **5**, we used their respective optimized π - π staking distances as presented in Table S1. Among the four model systems, **2** showed the highest coupling element matrix of 0.193 eV, leading to the highest drift mobility rate of 2.299 cm² V⁻¹ s⁻¹ for hole transport. On the other hand, **4**, with similar reorganization energy as **2**, exhibited the lowest drift mobility rate of 0.245 cm² V⁻¹ s⁻¹ as a result of having a lower coupling matrix. Considering the close reorganization energy values for these four systems, the calculated drift mobility rate of **2** (2.299 cm² V⁻¹ s⁻¹), **3** (1.717 cm² V⁻¹ s⁻¹), **4** (0.245 cm² V⁻¹ s⁻¹) and **5** (1.037 cm² V⁻¹ s⁻¹) thus follows the same descending trend as the coupling matrix, i.e. **2** > **3** > **5** > **4**. These values corresponded reasonably well with the reported mobility of 1.46 ± 0.46 cm² V⁻¹ s⁻¹, 0.5–1.5 cm² V⁻¹ s⁻¹ and 0.2–0.97 cm² V⁻¹ s⁻¹ respectively for the polymers of **3**²⁷, **5**²⁸, and **4**^{25,24} except for the polymer of **2**, which was reported to have mobility significantly lower (0.95 cm² V⁻¹ s⁻¹, due to low molecular weight)²³. Furthermore, due to the interplay between reorganization energy and coupling strength in determining the mobility rate, our studies suggested that for **2**, as high as 6 cm² V⁻¹ s⁻¹ (Supplementary Fig. S2b) could be obtained if the π - π stacking distance was reduced to ~3.3 Å — a π - π stacking distance that is much shorter than the normal value of ~3.7–3.9 Å generally observed for solution-processed polycrystalline polymer semiconductors. Our modeling studies thus suggested **1** as a polymeric form of **2** could potentially provide much higher carrier mobility than what have been reported if close π - π stacking could be achieved in its molecular packing.

Synthesis, processing and optimization of semiconductor 1. One plausible approach to tightening the π - π stacking of a relatively rigid and planar D-A polymer such as **1** was to increase its molecular weight. Increased molecular weight had also been linked to improved charge transport arising from better intergrain connectivity^{20,34,35}. Polymer **1** had been synthesized before, invariably at low molecular weights due to its relatively low solubility in the reaction media²³.

Our synthetic effort was directed at achieving very high molecular weight of **1** by optimizing the catalyst system and reaction conditions for the Stille coupling polymerization of 3,6-bis(5-bromothiophen-2-yl)-2,5-bis(2-octyl-1-dodecyl)pyrrolo[3,4-c]pyrrole-1,4-dione with 2,5-bis(trimethyl-stannyl)thieno[3,2-*b*]-thiophene. We had found that the reaction conditions, particularly the catalyst, reaction medium and reaction temperature had a profound effect on molecular weight of **1**. Specifically, we found that chlorobenzene was a particularly good reaction medium as it had excellent solvency for the sparingly soluble polythiophene polymers. In addition, changing the catalyst from the common bis(triphenylphosphine)palladium(II) dichloride or tetrakis(triphenylphosphine)palladium(II) to a catalyst system comprising tris(dibenzylideneacetone)-dipalladium [Pd₂(dbda)₃] and tri(*o*-tolyl)phosphine in appropriate catalytic stoichiometry and employing higher reaction temperatures were particularly efficient in boosting the molecular weight of **1** (Table 1).

Physical characterization. Relatively low-molecular weight (i.e. $M_n < 30,000$) samples of **1** were soluble in common organic solvents such as toluene, chloroform and THF, while very high-molecular weight samples (i.e. $M_n > 70,000$) exhibited solubility only in chlorinated solvents such as chloroform and chlorobenzene (as high as 5 mg/ml). At room temperature, **1** displayed a great tendency to aggregate in solution. Thus, the molecular weight of **1** as obtained by room-temperature gel permeation chromatography (GPC) would provide a misleadingly high value as the measurements reflected only the aggregated forms composed of several polymer chains. This was found to be true with previously reported high molecular weights for **1**^{23,24}. To illustrate this point, we found that the molecular weight values of **1** obtained by room-temperature GPC using THF as eluent ($M_n/M_w = 320,000/840,000$) were about one order of magnitude lower ($M_n/M_w = 29,000/91,000$) when measured by high-temperature GPC using 1,2,4-trichlorobenzene as eluent (Table 1).

The highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) levels of **1** as determined by cyclic voltammetry (Supplementary Fig. S3a) gave respectively -5.2 eV and -3.5 eV from vacuum with a bandgap of 1.7 eV. UV-vis spectra of chloroform solution **1** (Supplementary Fig. S3b) gave λ_{max} of 822 nm. A spin-cast film (from chloroform solution, 5 mg/ml) of **1** annealed at 120 °C exhibited λ_{max} similar to that of solution absorption, but with an additional strong absorption peak at λ of 748 nm, suggesting highly ordered molecular organization in the solid state.

Tapping-mode atomic force microscopy (AFM) of a thin film of high-molecular weight sample ($M_n/M_w = 110,000/501,000$) of **1** showed large fibrous crystalline domain structures having dimensions of 30–40 nm in width and more than 1 μ m in length (Supplementary Fig. S4). This was corroborated by the grazing incidence X-ray diffraction (GIXRD) results (Supplementary Fig. S5) showing high crystallinity. The out-of-plane (Q_z) diffraction exhibited a progression of peaks at $Q_z = 0.34 \text{ \AA}^{-1}$ ($2\theta = 4.80^\circ$), demonstrating an interlayer spacing of 18.4 Å. This is in excellent agreement with the calculated intermolecular polymer chain packing distance of approximately 18.5 Å for **1** with the longest chains fully extended from the backbone in a lamellar-like structure. The in-plane diffraction (Q_{xy}) displayed a diffraction peak at $Q_{xy} = 1.83 \text{ \AA}^{-1}$ ($2\theta = 25.95^\circ$), demonstrating a very close π - π stacking distance of 3.43 Å. The out-of plane diffraction peaks increased significantly with increasing molecular weight (Fig. 2), film thickness ~100 nm), attesting to a much higher crystallinity in the higher molecular weight films.

Further evidence of tighter π - π stacking was obtained through high-resolution transmission electron microscopy (TEM) analysis of the same high-molecular weight sample of **1**. Thin films of **1** were first deposited on Si wafer and then delaminated from the substrate and transferred onto a TEM grid coated with a layer of lacey carbon film. TEM analysis was carried out on an FEI Titan 80/300 Scanning/TEM equipped with an EDX detector and a Gatan Image Filter (GIF). There was random dispersion of highly crystalline domains in the polymer film, and most of these crystalline domains were not

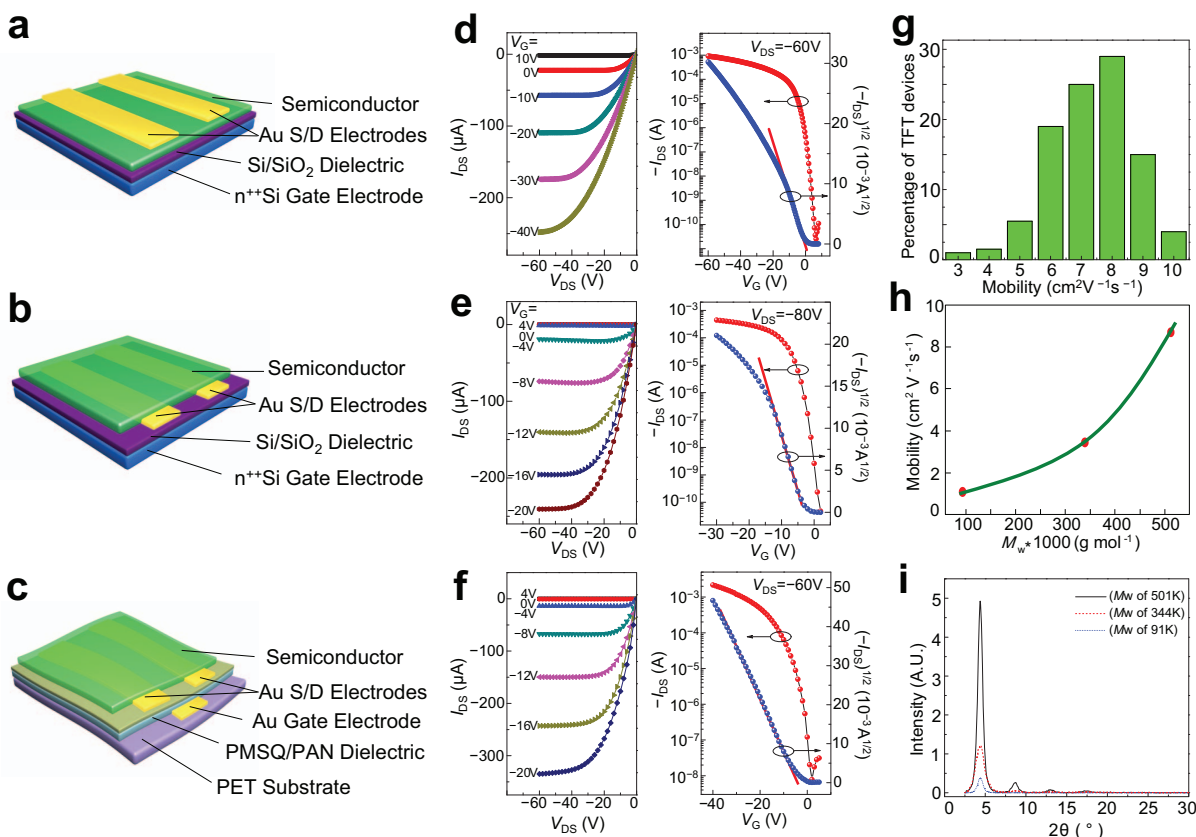


Figure 2 | Illustrative OTFTs with channel semiconductor 1 and their FET characteristics in ambient conditions: (a) and (b) are respectively schematic BGTC and BGBC devices on Si wafer while (c) is a schematic BGBC device on flexible PET substrate. For devices (a) and (b), the Si/SiO₂ surfaces were first modified with alkyl silyl self-assembled monolayers (SAMs) from octyltrichlorosilane and octadecyltrichlorosilane respectively before semiconductor was deposited by spin coating. The heavily n-doped Si wafer substrate served as a common gate electrode for these devices while vacuum deposited gold (Au) features served as the source/drain electrodes. For device (c), vacuum deposited Au gate and source/drain electrodes were separated by a spin-cast PMSQ/PAN dielectric layer modified with octadecylsilyl SAM, and the semiconductor was deposited by spin coating directly on source/drain electrodes on the dielectric surface. (d), (e), and (f) are the respective output curves and transfer characteristics of devices (a), (b) and (c). The mobility distribution for over 200 devices of (a) and (b) is summarized in (g), showing mobility ranging from 3 cm² V⁻¹ s⁻¹ to about 10 cm² V⁻¹ s⁻¹. The dependence of average saturated mobility of five representative devices on semiconductor weight-average molecular weight (M_w) is depicted in (h). Increased crystallinity of a thin film (~100 nm) of semiconductor 1 as a function of increasing M_w is reflected by increased intensity of XRD diffractions as shown in (i).

oriented along major zone axis during TEM observation. To avoid causing damage to the fragile polymer film, the acceleration voltage was lowered down to 200 kV and we did not focus the beam or tune the sample to a major zone axis. The magnification of high-resolution TEM images was carefully calibrated by a standard Si sample. The lattice distances in HRTEM images were calculated using the fast Fourier transform (FFT) of the obtained image, with an error of 1% (0.003 nm). We had taken more than 40 high-resolution images and shown the regions with clear planar structures. The FFT of a typical example (Supplementary Fig. S6c) revealed that the electron beam was parallel to the π - π stacking domains and a clear lamellar structure was present with a spacing of 0.336 nm. The streaks along the diffraction spots may be caused by the stacking faults of different lamellar domains. These TEM images (Fig. S6) clearly showed that in some highly crystalline areas, very close π - π stacking distance of 0.334 to 0.349 nm was achieved, in excellent agreement with our GIXRD finding of 3.43 Å for π - π stacking. No such close π - π stacking could be found in the thin films of lower-molecular weight samples.

OTFT fabrication and characterization. The FET characteristics of high-molecular weight 1 as channel semiconductor were investigated using a bottom-gate, top-contact (BGTC, Fig. 2a) and bottom-gate,

bottom-contact (BGBC, Fig. 2b) OTFT devices fabricated respectively on octyltrichlorosilane (OTS-8)- and octadecyltrichlorosilane (OTS-18)-treated Si/SiO₂ substrates. The gold (Au) source-drain electrodes were prepared by photolithography and semiconductor 1 was deposited from its chlorobenzene solution via spin-coating, blade coating or inkjet printing. OTFT devices on flexible PET (polyethylene terephthalate) substrate were also fabricated with a polymer bilayer dielectric composing of a top polymethylsilsesquioxane layer and a bottom polyacrylonitrile layer (PMSQ/PAN) via spin coating (Fig. 2c). Cross-linked PMSQ was chosen to provide resistance to potential solvent attack during subsequent semiconductor deposition. It also provided a hydroxy-functionalised surface for anchoring OTS surface modifying agents. PAN was utilized for its high dielectric breakdown voltage, low leakage current density, relatively high dielectric constant (high- κ , 6.27) and good solubility in the fabrication solvent. The fabrication and evaluation were conducted entirely under ambient conditions without taking precautionary measures to exclude atmospheric oxygen, moisture and light. Fig. 2d, e and f show representative transfer and output current-voltage plots. Very high hole mobility of up to 10.5 cm² V⁻¹ s⁻¹ in the saturation regime, sharp subthreshold slope of 1.0 V dec⁻¹, high on/off current ratio $\geq 10^6$, and high drain current of ~ mA were obtained. The mobility was extracted using the slope of square root of source/drain current (I_{DS})


Table 2 | Field-effect performance characteristics of OTFTs of different device configurations and dimensions with channel semiconductor 1 as measured under ambient conditions

OTFT Configuration [†]	Substrate	Deposition Process	Dielectric (nm)/SiO ₂ -modifying agent [‡]	W/L (μm/μm)	μ (cm ² V ⁻¹ s ⁻¹)	I _{on} /I _{off} (log ₁₀)	V _T (V)	S (Vdec ⁻¹)
BGTC	Silicon	Spin coating	SiO ₂ (200)/OTS-8	4000/100	5.5–8.2	7.0–8.0	0–4	0.8–1.0
BGTC	Silicon	Spin coating	SiO ₂ (200)/OTS-8	4000/125	5.5–9.0	7.0–8.0	0–4	0.8–1.0
BGBC	Silicon	Spin coating	SiO ₂ (300)/OTS-18	1400/30	3.5–8.0	6.0–8.0	-5–3	0.8–1.6
BGBC	Silicon	Spin coating	SiO ₂ (300)/OTS-18	1400/40	5.4–10.5	6.0–8.5	-6–4	0.7–1.4
BGBC	Silicon	Spin coating	SiO ₂ (300)/OTS-18	1400/50	5.2–10.5	6.0–8.5	-6–3	0.7–1.4
BGTC	Silicon	Blade coating	SiO ₂ (200)/OTS-8	4000/125	3.5–5.3	6.0–7.0	-1–1	1.0–1.2
BGTC	Silicon	Inkjet printing	SiO ₂ (200)/OTS-8	1400/125	1.5–3.5	5.5–6.0	-1–1	1.0–1.2
BGBC	PET	Spin coating	PAN/PMSQ (800/50)/OTS-18	7000/70	1.7–5.3	5.0–7.5	-6–2	1.3–2.0

[†]BGTC: bottom-gate, top-contact; BGBC: bottom-gate, bottom-contact.

[‡]OTS-8: surface modification with octyltrichlorosilane and OTS-18: surface modification with octadecyltrichlorosilane.

versus gate voltage (V_G) plot in the region of V_G from 0 to -15 V (red slope lines in Fig. 2d, e and f) in accordance with reported practices.^{24,34,35} Over two hundred devices were measured and the saturation mobility of $5.5\text{--}9.0\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ and $3.5\text{--}10.5\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ were obtained respectively for spin-coated BGTC and BGBC devices on OTS-modified Si/SiO₂ substrates depending on device dimension (Table 2 and Fig. 2g). The average mobility extracted from the saturation regime was about $7\text{--}8\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for these devices, while the mobility ranges for the linear regimes were $1.84\text{--}3.41\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ and $1.81\text{--}3.28\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ respectively at V_{DS} of -10 V and -5 V. The flexible BGBC devices on PET substrates also exhibited excellent performance with mobility of $1.7\text{--}5.3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ and current on/off ratio $> 10^5$. To the best of our knowledge, both the highest and average mobilities observed are the world records to date for polymer semiconductors. Other deposition techniques such as blade coating and inkjet printing afforded lower mobility ($\sim 1.5\text{--}5.3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$).

As expected, we found that high molecular weight was central to the achievement of extremely high FET mobility as reflected in Fig. 1h, showing variation of mobility from about $1\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for the low molecular weight sample (M_w/M_n : 91K/29K) to a high of about $8\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for the high molecular weight sample (M_w/M_n : 501K/110K).

Despite the remarkable FET performance of these OTFTs, we noticed that for some devices the $(I_{DS})^{1/2}\text{--}V_G$ plot showed some deviation from linearity in the high source/drain current regimes ($\sim 10^{-4}\text{--}10^{-3}\text{ A}$). This bending phenomenon had also been previously observed by many other groups^{24,34,35}. This was more pronounced in the larger-channel than smaller-channel devices. Fig. 3a shows that while smaller-channel devices (i.e. $L \leq 10\text{ }\mu\text{m}$) behaved normally, the larger-channel devices (i.e. $L \geq 20\text{ }\mu\text{m}$) exhibited some bending in $(I_{DS})^{1/2}\text{--}V_G$ plots under the same V_{DS} conditions. The studies of $(I_{DS})^{1/2}\text{--}V_G$ as a function of source/drain voltage (V_{DS}) for a $10\text{-}\mu\text{m}$ channel length device (Fig. 3b) revealed that the $(I_{DS})^{1/2}\text{--}V_G$ plot bending occurred at lower fields ($V_{DS} = -20$ V or -60 V) while at higher fields ($V_{DS} = -80$ to -100 V), near normal behaviour prevailed. The highest mobility extracted from our devices without significant bending was $5.3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$. Notwithstanding this anomalous behaviour, no discernable second-order curvatures in the output curves were observed. The width-normalised contact resistance for these devices was $-3.5\text{ k}\Omega\text{-cm}$ and $16\text{ k}\Omega\text{-cm}$ at V_G of -20 V and -10 V respectively. These are comparable to those calculated for $\alpha\text{-Si TFTs}$ ³⁰, and were negligibly insignificant as to cause the bending in the $(I_{DS})^{1/2}\text{--}V_G$ plot. As the problem could be alleviated or eliminated by increasing the source/drain field, it is possible that this was due to carrier supersaturation in the conduction channel at high source/drain current regimes leading to decreased carrier velocity. It may also be due to low-density shallow charge trapping in the semiconductor and/or interface. Further in-depth studies would be necessary to shed light on this apparent transport anomaly.

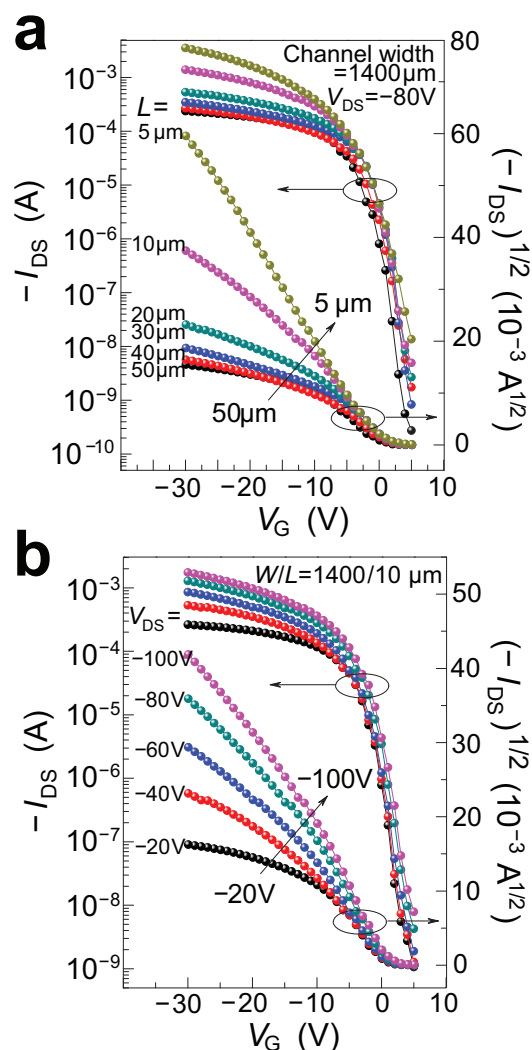


Figure 3 | FET performance characteristics of different-dimension OTFT devices with channel semiconductor 1. (a) Transfer characteristics of devices with different channel lengths at source/drain voltage (V_{DS}) of -80 V showing dependence of $(I_{DS})^{1/2}\text{--}V_G$ plot on channel length. (b) Transfer characteristics of a $10\text{-}\mu\text{m}$ device ($W = 1400\text{ }\mu\text{m}$) under different V_{DS} showing dependence of $(I_{DS})^{1/2}\text{--}V_G$ plot on source/drain field.

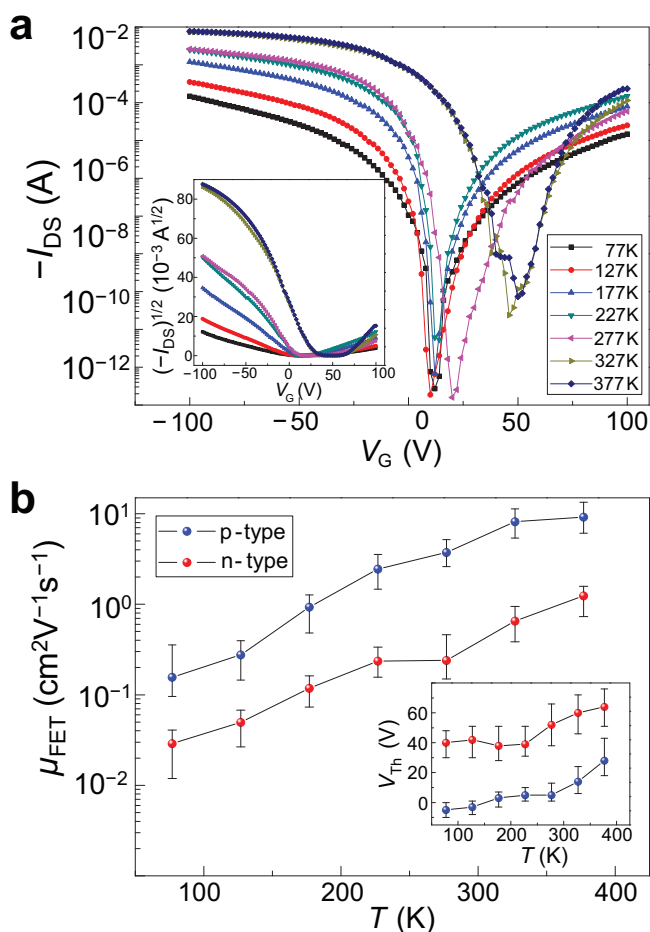


Figure 4 | Temperature effects on FET characteristics. (a) Plot of source-drain current (I_{DS}) as a function of gate voltage (V_G) at various temperatures (77 K to 373 K) with source-drain voltage $V_{DS} = -40$ V (inset is plot of square root of I_{DS} as a function of V_G at different temperatures and $V_{DS} = -40$ V). (b) Temperature dependence of electron and hole mobilities in vacuum (inset is the temperature dependence of threshold voltage, V_T). The lowest electron and hole mobilities at 77 K are respectively $0.011 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $0.096 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ while the highest electron and hole mobility at 373 K are respectively $1.58 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $13.41 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ ($W/L = 1400 \mu\text{m}/50 \mu\text{m}$).

Temperature-dependent and ambipolar FET characteristics. The temperature-dependence and ambipolar charge transport behaviours of **1** were investigated in vacuum at below 1×10^{-3} Pa. The results show that as the temperature increased, I_{DS} increased as well and the threshold voltage (V_T) drifted towards positive direction (Fig. 4a). A plot of $(I_{DS})^{1/2} - V_G$ clearly shows V_T drift and mobility increase (inset of Fig. 4a, b). Both hole and electron transport characteristics were observed in vacuum (Supplementary Fig. S7). The highest hole and electron mobilities at 373 K were respectively 13.5 and $1.58 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$. Ambipolar transport with balanced hole and electron mobility of $\sim 1.5 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ under nitrogen atmosphere had been reported for this polymer before³⁸. The activation energies for hole and electron conduction were estimated to be respectively 60 meV and 49 meV. Positive temperature coefficient of mobility ($d\mu/dT > 0$, Fig. 4b) was noted, demonstrating a hopping transport mechanism instead of band-like transport observed in highly organized crystalline semiconductors such as single crystals. This is particularly puzzling as most solution-processed organic semiconductors, except single-crystalline compounds such as rubrene, have exhibited mobility about an order of magnitude lower. The achievement of such a high mobility by a solution-processed polycrystalline polymer semiconductor via hopping mechanism is

unimaginable even for today. We consistently obtained the same results with repeated experiments, confirming the hopping transport mechanism for this polymer semiconductor. Accordingly, this semiconductor will be expected to stimulate further fundamental research interest in the understanding of charge transport in organic systems. Our modeling and experimental studies suggest that this may be linked to the ability of high-molecular weight **1** to achieve very close π - π stacking in molecular organization in the solid state^{36,37}.

Hysteresis, bias stress effects and device stability. Representative OTFT devices with high-molecular weight semiconductor **1** were subjected to hysteresis and bias stress tests. Only very slight hysteresis effect (Fig. 5a) was noted. There were essentially no bias stress effects as no changes in the transfer characteristics and no shifts in both of its turn-on and threshold voltages were observed (Fig. 5b) when the device was subject to negative gate bias stress for duration of up to 1080 s with $V_{DS} = -60$ V. The shelf-life stability of OTFTs was monitored using BGTC devices on OTS-8 treated Si/SiO₂ substrate. The devices were stored in ambient conditions without insulating the devices from exposure to atmospheric air, moisture and room light. The mobility and on/off ratio of five representative devices were measured periodically at different intervals over a period of over one year. Fig. 5c shows the mobility and on/off of the devices for 56 weeks. No apparent statistical variations in mobility and on/off ratio occurred, demonstrating excellent device stability under ambient conditions. The transfer characteristics of a newly fabricated TFT device and that of the device that had been standing in ambient conditions for 56 weeks as shown Fig. 5d are essentially similar, revealing no appreciable changes in its transfer behaviour over time. These results represent the first report of unprecedented shelf-life stability of a solution-processed OTFT with extremely high mobility and on/off ratio. In addition, the device also displayed excellent operating cyclic stability as it maintained its on- and off-currents very well when continuously turned on and off over a period of 3500 s (Fig. 5e).

Inverters and Circuits. To demonstrate the feasibility of using high-molecular weight semiconductor **1** in semiconductor devices, we fabricated inverter devices and PMOS-based ring oscillator circuits on flexible substrates using BGBC configuration (Fig. 2c). The fabrication involved thermal vacuum evaporation of Au gate on FET substrate before deposition of PAN (800 nm)/PMSQ (50 nm) bilayered dielectric via spin-coated. After surface modification of the dielectric with OTS-18 SAM, Au source/drain electrodes were vacuum evaporated, followed by spin coating of semiconductor **1**. We had found that a thin coating of Ag (~ 80 nm) prepared by thermal evaporation on the gate and source/drain electrode surfaces improved their conductivity and electrical connections. The resulting inverter device showed clear response when switching between logic '1' (30 V) and logic '0' (0 V) (Fig. 6a) and surprisingly, a maximum voltage gain of 92 for this PMOS-like device was obtained. Further integration of inverters yielded a five-stage ring oscillator with a switching frequency of about 1.2 kHz (Fig. 6c). This oscillating frequency is surprisingly low, given the extremely high mobility of the semiconductor. The unexpectedly low oscillating frequency was likely due to the large channel devices that we used as well as the relatively large parasitic capacitance arising from significant electrode overlapping. It is well known that the performance of an oscillator depends on transistor size and parasitic capacitance from electrode overlapping. In our oscillator devices (Fig. 6b), the overlapping of the source/drain electrodes with gate electrode was very large (larger than the channel length), leading to very high parasitic capacitance which seriously restricted the oscillator frequency. We believe that with smaller channel transistors and lesser electrode overlap, higher-frequency oscillator devices can be fabricated with our polymer semiconductor.

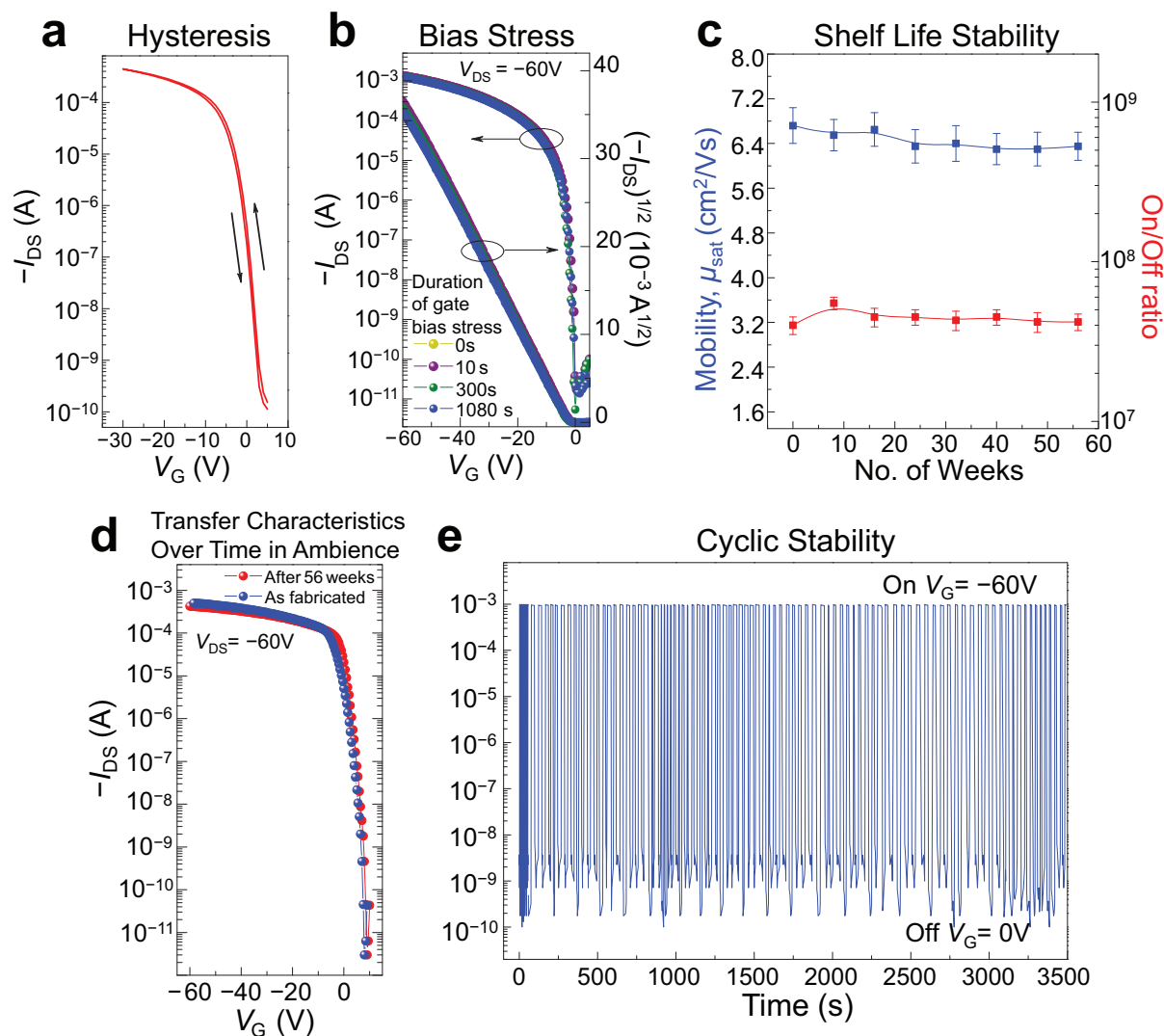


Figure 5 | Stability characteristics of OTFTs with polymer semiconductor 1. (a) Transfer characteristics of forward and backward V_G sweeps showing a slight hysteresis effect of a representative device. (b) Stability of transfer characteristics of a representative device under different bias stress conditions. (c) Shelf-life stability under ambient conditions, showing stability of mobility and on/off ratio obtained from five representative devices for over one year period. (d) The transfer characteristics of as-cast device and that of device after standing in ambient conditions for 56 weeks. (e) Cyclic stability of a representative device showing maintenance of on- and off-currents during continuous on/off cycles for 3500 s.

Discussion

We have developed a very high molecular-weight DPP-DTT-based polymer, **1**, which can be solution-processed into an ambient-stable, high-performance thin-film semiconductor for OTFT application. OTFT devices fabricated with this polymer semiconductor have exhibited very high mobility (up to $10.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and on/off ratio ($\geq 10^6$), together with excellent FET performance characteristics and exceptional device shelf-life and operational stabilities. The temperature-dependent characteristics of the transport behaviour of this polymer semiconductor unequivocally attest to a hopping mode transport mechanism with low activation energy. Very high-gain PMOS inverter devices and functional oscillator circuits have been fabricated from this polymer semiconductor, demonstrating its potential for broad-range, high-value technological applications. These results represent a significant achievement in organic semiconductor development and are expected to help propel technological translation of printed electronics from laboratory to marketplace. From the theoretical perspective, the ability of a polycrystalline polymer semiconductor to achieve a single crystal-like charge carrier transport points to the deficiency and limitations of existing theory of charge transport in organic systems. This high-mobility polymer

semiconductor will thus be of fundamental importance to organic semiconductor research and organic electronics.

Methods

Materials. PAN, purchased from Aldrich without further purification. PMSQ was synthesized according to previous reports.

Semiconductor polymer synthesis. An illustrative polymerization procedure for generating very high-molecular weight polymer **1** is as follows: To a Schlenk flask was added 3,6-bis(5-bromothiophen-2-yl)-2,5-bis(2-octyl-1-dodecyl)pyrrolo[3,4-c]pyrrole-1,4-dione (0.2 mmol), 2,5-bis(trimethylstannyl)thieno[3,2-b]thiophene (0.2 mmol), tri(*o*-totyl)phosphine (8 mol% equivalent), tris(dibenzylideneacetone)-dipalladium (2 mol% equivalent) and dry chlorobenzene (20 ml) under a nitrogen atmosphere. The flask was securely sealed and stirred for 72 h at 130°C . After cooling to room temperature, the reaction mixture was poured into a stirring mixture of methanol (100 ml) and concentrated hydrochloric acid (8 ml) and stirred for 16 h. The precipitated product was collected by filtration and subjected to consecutive Soxhlet extractions with ethanol, ethyl acetate, chloroform and chlorobenzene. The final chlorobenzene extraction was vacuum evaporated and dried under vacuum to afford electrically pure polymer **1** in 56% yields.

Fabrication of TFT devices, inverters and oscillators. A heavily n-doped Si wafer with a 200 or 300-nm SiO_2 surface layer (respective capacitance of 17.25 and $11 \text{ nF} \cdot \text{cm}^{-2}$) was employed as the substrate with Si wafer serving as a common gate electrode and SiO_2 as the dielectric. The high-crystallized OTS layers play a very

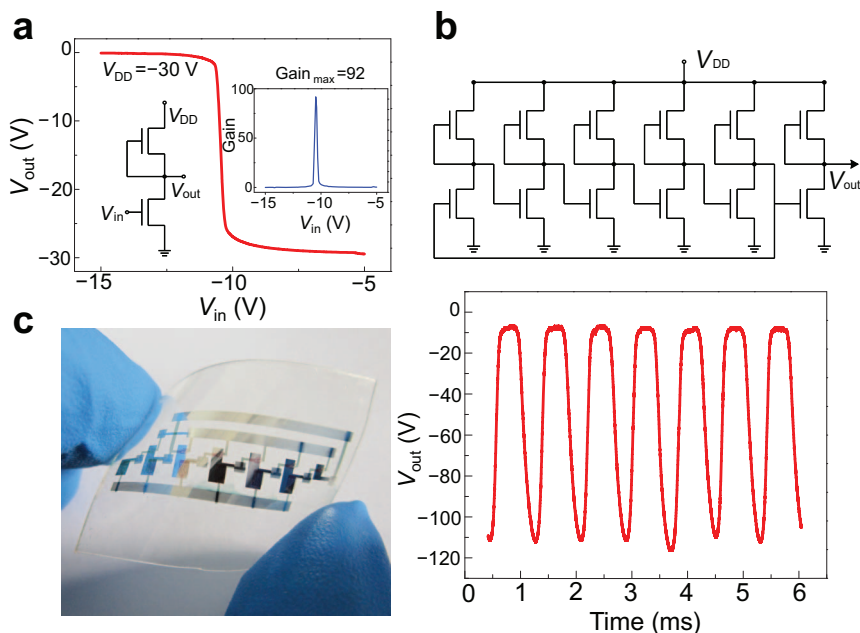


Figure 6 | Schematic representations and electrical characteristics of inverter and oscillator circuit built on OTFTs with channel semiconductor 1. Devices were fabricated on flexible PET substrate with thermal vacuum evaporated Au as gate electrodes. The bilayer dielectric (800 nm-PAN / 50 nm-PMSQ) was spin-coated and its surface modified with OTS-18 SAM. Subsequently, Au source/drain electrodes were deposited on the OTS-18-treated dielectric layer before channel semiconductor 1 was deposited by spin coating. The electrical connections of gate and source/drain electrodes were found to be enhanced by deposition of an 80 nm Ag layer. (a) Schematic electrical connection and characteristics of an illustrative inverter: $V_{DD} = -30$ V and the maximum gain ~ 92 . (b) Optical image of a flexible five-stage ring oscillator device. (c) Schematic electrical connection and electrical characteristics of an illustrative flexible five-stage ring oscillator: $V_{DD} = -130$ V and switching frequency ~ 1.2 KHz. Inserts of (a) and (b) are schematic electrical connections of inverter and oscillator devices.

important role in the high performance devices. For the OTS-8 SAM modification, the Si wafer surface was first cleaned by sonication in acetone for 5 min, and immersed in Piranha solution (7:3 mixture of sulfuric acid and 30% hydrogen peroxide) for 10 min. This was followed by rinsing with deionized water for several times before treating with a 0.1 M solution of octyltrichlorosilane (OTS-8) in toluene at 60°C for 20 min. After rinsing with toluene, it was blown dried with nitrogen to afford an OTS-8 SAM on the substrate surface. For the OTS-18 SAM modification, the silicon wafer (with/without Au bottom contact for BGTC/BGBC) was cleaned and treated with hot Piranha solution as before. It was then further subjected to sonication sequentially in ethanol and acetone for 6 min each, and then put in a culture disk with a drop of octadecyltrichlorosilane (OTS-18). The disk was then covered and heated in a vacuum oven at 120°C for 3 h resulting in the formation of an OTS-18 SAM on the surface. For BGTC devices, semiconductor 1 was spin coated from its dichlorobenzene solution (5 mg/ml) on the dielectric surface and annealed in a vacuum oven at 160°C for 30 min. The Au source/drain electrodes were then deposited via thermal vacuum evaporation on the semiconductor layer through a shadow mask bearing the source/drain electrode features of various dimensions. The BGBC devices were fabricated similarly except Au source/drain electrodes were deposited on the dielectric layer before spin coating the semiconductor solution and then annealed at 160°C on a hot plate in ambient conditions for 5 min. The fabrication of TFT, inverter, and oscillator devices on flexible PET substrates were performed under ambient conditions except Au electrode deposition. 80 nm Au gate electrodes were first deposited on the substrate via thermal vacuum evaporation. The substrate was then deposited with a PMSQ/PAN dielectric bilayer from sequential spin coating of a PAN solution in DMF (70 mg/ml) at 80°C and a 5% PMSQ solution in ethanol at 3000 r.p.m. The dielectric layers were annealed at 150°C for 60 min. Thereafter, the substrates were irradiated with ultraviolet ozone for 15 min, followed by dipping in octadecyltrichlorosilane solution in hexane (1:100 v/v mixture) for 1 min. Subsequently, Au source/drain electrodes were deposited on top of the dielectric surface before spin coating of semiconductor solution.

Device characterization. Characterization of fabricated OTFT devices was carried out using a Keithley 4200 Semiconductor Characterization System in ambient air. The field-effect mobility in the saturation regime was extracted using equation, $I_{DS} = (\mu WC_i/2L)(V_G - V_T)^2$ under the condition of $-V_{DS} > -(V_G - V_T)$. For mobility in the linear regime, equation, $I_{DS} = (\mu WC_i/L)(V_G - V_T - V_{DS}/2)$ was utilized under the condition of $-V_{DS} \ll -(V_G - V_T)$, where I_{DS} is the source-drain current, μ is the field-effect mobility, W is the channel width, L is the channel length, C_i is the capacitance per unit area of gate dielectric layer, and V_G , V_T and V_{DS} are the gate, threshold and source-drain voltages respectively. Atomic force microscopy (AFM) images were obtained on a Nanoscope V AFM (Digital Instruments) in tapping mode.

Molecular weights were determined with GPC at 160°C on a PL-220 system using three PLgel Olexis columns and 1,2,4-trichlorobenzene as eluent. A flow rate of 1 mL min^{-1} was used.

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Acknowledgements

Beijing Synchrotron Radiation Facility (BSRF) is gratefully acknowledged for the grazing incidence X-ray diffraction measurements. This work was partially supported by funding from Exploit Technologies Pte Ltd. of Agency for Science, Technology and Research of Singapore, National Natural Science Foundation of China, Major State Basic Research Development Program, and Chinese Academy of Sciences.

Author Contributions

B.S.O. supervised J. L., H.S.T., M.L. and S.H.L. in semiconductor material development, device fabrication/characterization, and device performance and stability studies. Y.Q.L. supervised Y.Z., Y.L.G., C.-A.D. and G.Y. in device fabrication/characterization, charge transport studies, and fabrication/characterization of inverter and oscillator devices. Y.Z., H.S. and B.S.O. contributed to molecular modeling and simulation studies. B.S.O. directed the overall project and wrote the manuscript.

Additional information

Supplementary information accompanies this paper at <http://www.nature.com/scientificreports>

Competing financial interests: The authors declare no competing financial interests.

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How to cite this article: Li, J. *et al.* A stable solution-processed polymer semiconductor with record high-mobility for printed transistors. *Sci. Rep.* **2**, 754; DOI:10.1038/srep00754 (2012).