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Nonvolatile multilevel data storage memory device from controlled ambipolar charge trapping mechanism

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The capability of storing multi-bit information is one of the most important challenges in memory technologies. An ambipolar polymer which intrinsically has the ability to transport electrons and holes as a semiconducting layer provides an opportunity for the charge trapping layer to trap both electrons and holes efficiently. Here, we achieved large memory window and distinct multilevel data storage by utilizing the phenomena of ambipolar charge trapping mechanism. As fabricated flexible memory devices display five well-defined data levels with good endurance and retention properties showing potential application in printed electronics.

Tremendous efforts have been made to develop non-volatile memory devices with reliable data storage and low cost[1–14]. Among many kinds of memory devices, flash memories which use a floating gate structure are the most widely used[15–17]. To improve the device reliability, the recent trend of designing charge trapping layer for flash memory is to store data in discrete charge trapping cites such as metal or semiconductor nanoparticles[18–23]. On the other hand, for the selection of semiconductor layer, polymer materials are excellent candidates for large-area flexible electronic devices and exhibit high throughput because of their printability[24–26]. Most of the researches on polymer memory devices are focused on binary data storage with unipolar polymer semiconductors[27,28]. The memory window in these devices are constrained by unipolar charge carriers trapping mechanism, and tremendous efforts have been made to develop various kinds of charge trapping layers to get reasonable large memory window[19,28]. However, even with enough trapping sites and deep trapping levels the memory window of unipolar flash memories are still usually not enough to achieve distinct multilevel data storage. The capability of storing multi-bit information is one of the most important challenges in memory technologies and it provides a low-cost way to increase the memory density per unit cell area[29–31]. Ambipolar materials, which possess both electrons and holes, have got significant technological interest as an alternative approach to mimic complementary circuits[32–34]. The fabrication procedure of logic circuits could be further simplified by using single-component ambipolar materials with symmetric electrodes, and for that purpose solution-processable ambipolar polymers are one of the promising materials in printed electronics. Exploring the application of single-component ambipolar materials in flash memories is necessary to achieve unique properties that are not possible with unipolar counterparts. Reduced graphene oxide and semiconducting polymer have been investigated in charge trapping memory device, however, the practical application of such devices are still constrained by several factors such as unbalanced charge transport or high voltage operation[35,36]. On this regard, balanced trapping of both electrons and holes (ambipolar trapping)[37], is a way to achieve large memory window for designing multi-bit flash memories.

Here, we demonstrate a multilevel data storage memory based on a single-component solution-processable ambipolar polymer. A self-assembly monolayer of gold (Au) nanoparticle was inserted into the aluminum oxide (Al_2O_3) gate dielectrics which acted as both electron and hole trapping elements. The electrical behavior can be tuned in a large range by either trapping electrons or holes in the Au nanoparticles. We systematically studied the charging behavior under different gate bias and five well-defined data levels with good endurance and retention properties were demonstrated. Our reported approach offers new opportunities to fabricate novel multi-bit flash memory for printed electronics.

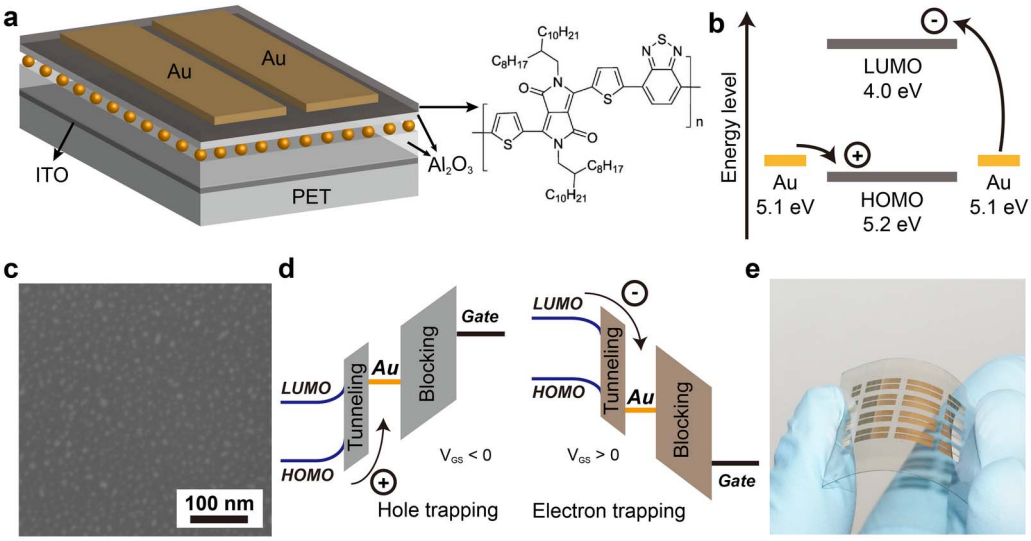

Figure 1 | (a) Three-dimensional schematic diagram of the ambipolar memory device and the chemical structure of PDPP-TBT. (b) Band diagram of PDPP-TBT in contact with gold electrodes. (c) SEM image of Au nanoparticle monolayer. (d) Energy band diagrams of the memory transistor at hole trapping mode and electron trapping mode. (e) Optical image of the flexible memory device on PET substrate.

Results

Device configuration and operation principle. The three-dimensional (3D) structure of the memory transistor and the chemical structure of the ambipolar polymer material, poly(diketopyrrolopyrrole-thiophenebenzothiadiazolethiophene) (PDPP-TBT), are shown in Figure 1a. The design and synthesis of PDPP-TBT has been reported before[38]. Bottom-gate top-contact structure was used for the fabrication of memory device. Atomic layer deposited Al_2O_3 was used as both blocking and tunneling dielectric layers, while the Au nanoparticle charge trapping layer was inserted between two dielectric layers. Au nanoparticles with a size of around 5 nm were synthesized by the citrate reduction method and adsorbed on Al_2O_3 with the help of 3-aminopropyltriethoxysilane (APTES)[39]. The blocking dielectric layer was used to prevent charge transfer from the gate to Au nanoparticle or vice versa. A thin tunneling/thick blocking dielectric system enables the inducement of an efficient charge transfer from semiconductor to Au nanoparticle. The applied electrical field in the tunneling dielectric layer can be estimated from the equation $E_1 = V_{GS}/(d_1 + d_2) + Q/(\varepsilon(1 + d_1/d_2))$, where d_1 (5 nm) is the thickness of tunneling dielectric layer, d_2 (200 nm) is the thickness of blocking dielectric layer, Q is the stored charge in the Au nanoparticles and ε is dielectric constant of Al_2O_3, respectively[35]. Initially during programming operation, the stored charges in Au nanoparticles were equal to zero. The applied electric field in the tunneling dielectric layer is estimated to be about 2 MV cm^{-2}. This high electrical field leads to efficient injection of the positive/negative charge carriers from the semiconductor and trapped in Au nanoparticles, which attributed to direct band-to-band tunneling or Fowler-Nodheim tunneling[22,27]. Fig. 1b shows the work function of the Au electrodes, the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) of the material, demonstrating both holes and electrons can be injected, accumulated and transported[38,40]. The scanning electron microscope (SEM) image of the self-assembly monolayer of Au nanoparticles is shown in Fig. 1c. The adsorbed Au nanoparticles made by citrate reduction method are well dispersed due to the repulsive force between neighboring nanoparticles. The average diameter is 5 ± 0.5 nm and density is 3.2×10^{11} cm^{-2}. Fig. 1d shows the schematic illustration of energy band structure of the ambipolar memory devices. Electrons/holes are injected from the active layer to the charge storage layer through the tunneling oxide at positive/negative gate bias. The optical image of the polymer memory devices on flexible PET substrate is shown in Fig. 1e.

Electrical performance of ambipolar trapping. Fig. 2a and 2b show the typical output characteristics of the ambipolar memory transistor. The curves show proper saturation at higher gate biases. The transfer curves in hole-enhancement mode at initial state and different programmed state (±40 V for 100 ms) are shown in Fig. 2c and 2f. The transfer curves in electron-enhancement mode at initial state and different programmed state (±40 V for 100 ms) are shown in Fig. 2e and 2h. It should be noted that the programming/erasing time can be further reduced by reducing the thickness of tunneling dielectric layer or increasing the programming voltage. The average saturation mobilities were about 0.051 cm^2 V^{-1} s^{-1} and 0.037 cm^2 V^{-1} s^{-1} for electrons and holes, respectively. Embedding Au nanoparticles in Al_2O_3 slightly decreases the mobilities of the ambipolar polymer[41]; however, the electrical performances are still satisfactory enough to ensure efficient operations. In addition, we fabricated transistors without Au nanoparticles (Fig. S1) to confirm that there is no charging in the Al_2O_3 gate dielectric layer. Thus, the holes/electrons are mostly trapped in the Au nanoparticles. In the hole-enhancement mode, the switch on voltage (V_s, the voltage when the transistor starts to operate in the enhancement mode) shifted to negative direction after the negative gate bias and shifted to positive direction after the positive gate bias. In the electron-enhancement mode, V_s shifted to positive direction after the positive gate bias and shifted to negative direction after the negative gate bias. From this observation, it is understood that the Au nanoparticles could act as both hole and electron trapping elements in our system. Fig. 2d and 2g illustrate the hole and electron trapping at negative and positive gate bias. It is noted that Vs reach certain saturated values under programming operations in both hole-enhancement mode and electron-enhancement mode. We estimate the coulomb charging energy from the equation $e^2/2C(r)$, where e is fundamental unit of charge and C(r) is the capacitance of Au nanoparticle. The capacitance of Au nanoparticle is estimated from $C(r) = 4\pi\varepsilon_0\varepsilon_r r$, where ε_0 is the permittivity of vacuum, ε_r is the dielectric constant of Al_2O_3 which surrounds the Au nanoparticle and r is the radius of nanoparticle[31]. The dielectric constant of atomic layer deposited Al_2O_3 is about 7 according to previously reported result[42]. From the above equation, charging energy for a 5 nm Au nanoparticle in a matrix of Al_2O_3 is about 34.7 meV which is similar to the thermal

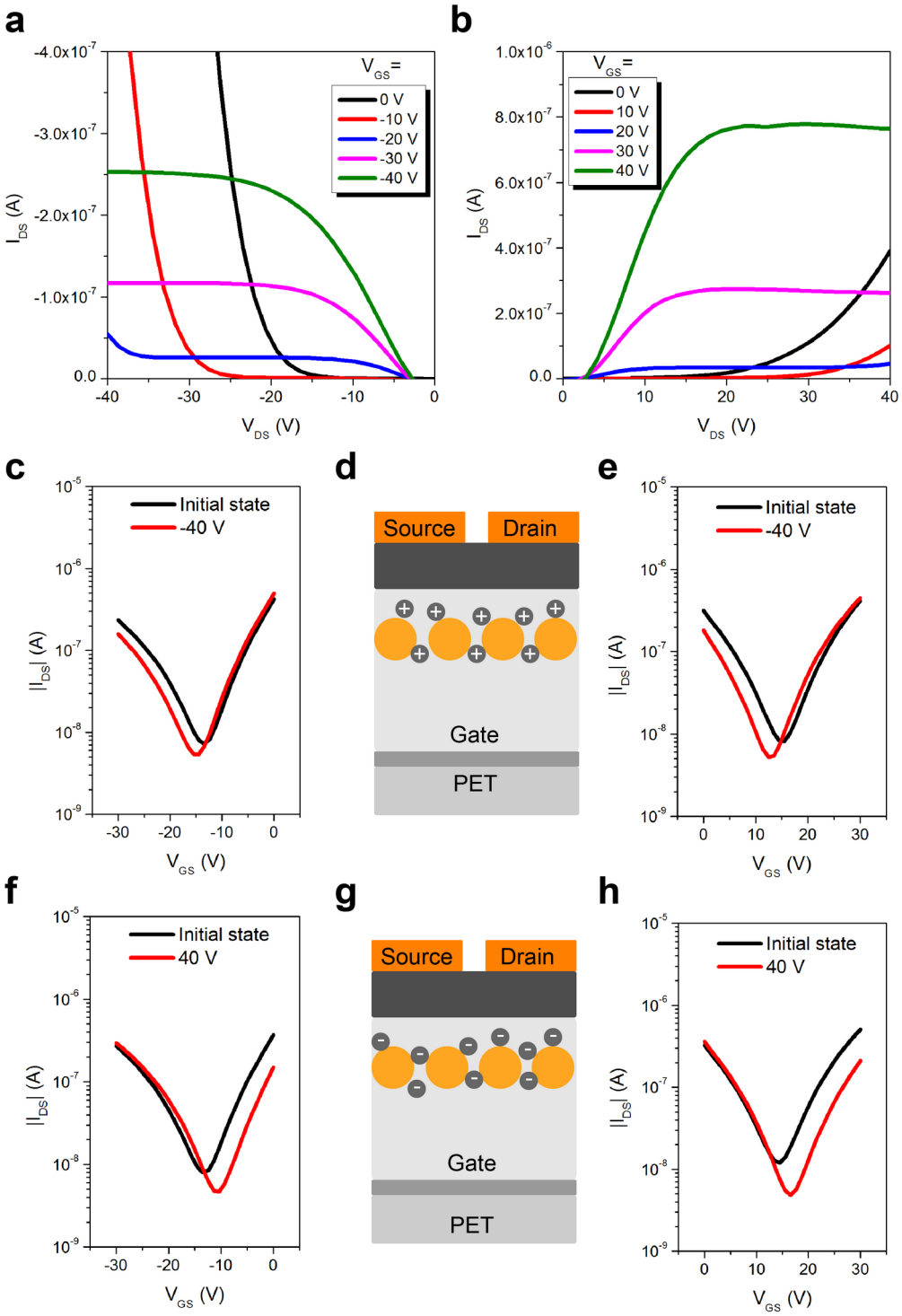

Figure 2 | (a) Initial output curves of the memory transistor at hole-enhancement mode. (b) Initial output curves of the memory transistor at electron-enhancement mode. (c) Transfer characteristics of the memory transistor before and after programming at −40 V for 100 ms at hole-enhancement mode. (d) Schematic illustration of the hole trapping phenomenon. (e) Transfer characteristics of the memory transistor before and after programming at −40 V for 100 ms at electron-enhancement mode. (f) Transfer characteristics of the memory transistor before and after programming at 40 V for 100 ms at hole-enhancement mode. (g) Schematic illustration of the electron trapping phenomenon. (h) Transfer characteristics of the memory transistor before and after programming at 40 V for 100 ms at electron-enhancement mode.

energy (k_BT, k_B is Boltzmann constant and T is temperature) at 300 K, indicating almost continuous charging without Coulomb blockade effect in the case of single nanoparticle[27]. However, in our memory devices, the coupling capacitances induced by the nanoparticle array should be considered. Here, the trap energy levels are fixed by the work function of Au nanoparticles. The charging process is random at the beginning; however, as the number of trapped charge carriers in single Au nanoparticle increases, the increased capacitive coupling will result in increased Coulomb repulsion[31].

Multi level data storage with ambipolar trapping mechanism. With the property of hole and electron trapping, we further investigate to tune the electrical performance of the ambipolar transistor in a wide range, specifically, from the hole trapping state to the electron trapping state or from the electron trapping state to the hole trapping state. The large memory window achieved by this concept will be of benefit to get multi data levels in memory devices. Fig. 3a shows the transfer curve shifts from the electron trapping state to hole trapping state in the hole-enhancement mode. The device was programmed at 40 V for 1s (data level 0), followed by the application of pulses with different length (−40 V) at the gate to get data level 1 to data level 4. Fig. 3b shows the transfer curve shifts from the hole trapping state to electron trapping state in the electron-enhancement mode. The device was programmed at −40 V for 1s (data level 0), followed by the application of pulses with different length (40 V) at the gate to get data level 1 to data level 4. The details of the applied bias in the measurements are illustrated in the supporting information (Fig. S3). These observations exhibit an interesting behavior of ambipolar memories for the design of multilevel data storage devices. Furthermore, to prove the significance of ambipolar transport mechanism in memories, we fabricated a memory device with solution processed p-type polymer poly(3-hexylthiophene) (P3HT) as the semiconductor layer (Fig. S4). We chose P3HT because it has similar hole mobility values with the polymer PDPP-TBT that has been used in our study. The fabricated device show clear unipolar electrical characteristics and the hole trapping mechanism in this device architecture leads to a memory window of about 7.5 V at the same program/erase bias. Compared with single type trapping system, the ambipolar memory provides broader range of tunable electrical properties. The threshold voltage shift is 12.5 V in hole enhancement mode and 13 V in electron enhancement mode. In Comparison with the unipolar device, a large threshold voltage shift is achieved in ambipolar device due to the transformation of different trapping states, from hole to electron trapping or from electron to hole trapping. In contrast, the threshold voltage shift in unipolar device is usually achieved by trapping and de-trapping of holes or electrons. The combined hole and electron trapping states induce more levels of data storage, which has a great potential for scaling down the memory cell. Fig. 3c and 3d shows the multilevel data storage characteristics in the hole-enhancement mode and

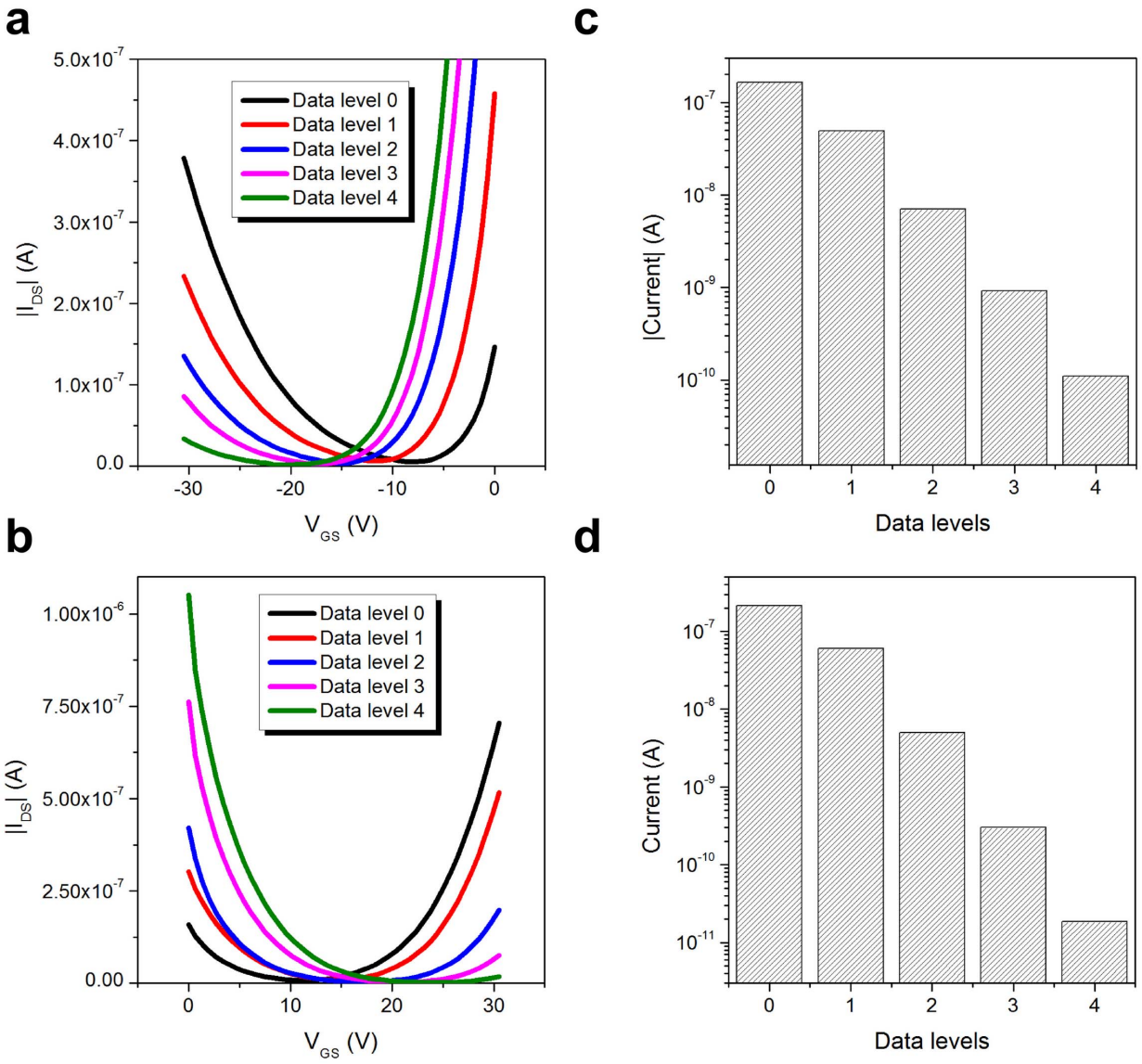

Figure 3 | (a) Transfer curves of different data levels in hole-enhancement mode. (b) Transfer curves of different data levels in electron-enhancement mode. (c) Drain-source current at different data levels in hole-enhancement mode. (d) Drain-source current at different data levels in electron-enhancement mode.

electron-enhancement mode. The reading gate bias was set as −18 V for hole enhancement mode and 21 V for electron enhancement mode, respectively. Five well-defined data storage levels are observed in both the modes. The enough data sensing margins demonstrate that this design could be readily applied to reliable multilevel operations. Endurance capability of memory devices is an important phenomenon in the operation of nonvolatile memory devices. The memory transistor exhibited stable operation for more than 1000 cycles without degradation (Fig. S5), which is promising for future applications.

Data retention and flexibility of the memory device. Fig. 4a and 4b show the data retention properties at different data levels in the hole and electron enhancement mode. Vertical loss of storage is usually resulting from the charge tunneling from the Au nanoparticles through the tunneling dielectric layer. The Au nanoparticle/Al_2O_3 can offer a large electronic barrier height to confine the trapped charge carriers in Au nanoparticles[43]. Lateral loss can be ignored in our system due to the controlled separation of neighboring Au nanoparticles[44]. All these states are maintained well for more than 10^6 s, which is adequate for practical applications. These results also demonstrate that both the holes and electrons are deeply trapped in Au nanoparticles, making it possible to tune the electrical performances of the transistors in a wide range. In addition to the reliable memory operations, the bending stability is another important property to determine the suitability of applying the ambipolar memory devices in flexible electronics. The flexible memories were repeatedly bended with a tensile strain of 1% which has been approximated from the values of D/2R, where D (200 μm) is the thickness of the flexible PET substrate and R (10 mm) is the bending radius[45]. Fig. 4c and 4e show the transfer characteristics of data level 0 and 4 in hole-enhancement mode before and after bending the substrate. Fig. 4d and 4f show the transfer characteristics of data level 0 and 4 in electron-enhancement mode before and after bending. The electrical properties have negligible changes during the bending test. The electrical properties of the ambipolar memories were also characterized during the bending state, and the transistors could be well operated (Fig. S6). In addition, we recorded the two data levels with respect to numbers of bending cycles, as shown in Fig. 4g and 4h. These data states of the memory devices were well maintained and the whole data level range did not degrade for over 1000 cycles. In addition, to further extend our ambipolar device to low voltage operation, we fabricate the flexible memory cell with thinner blocking dielectric layer (40 nm). The resulted device can work properly under ±10 V in both hole-enhancement mode and electron-enhancement mode (Fig. S7), demonstrating the potential for low power consumption applications.

Discussion

Although the applications of ambipolar materials (reduced graphene oxide or semiconductor polymer) have been investigated in memory devices previously[35,36], the multilevel operation by the transition between holes and electrons (ambipolar) trapping mechanism provides a new concept. Through a solution processed ambipolar polymer layer, we demonstrated multilevel data storage and proved the

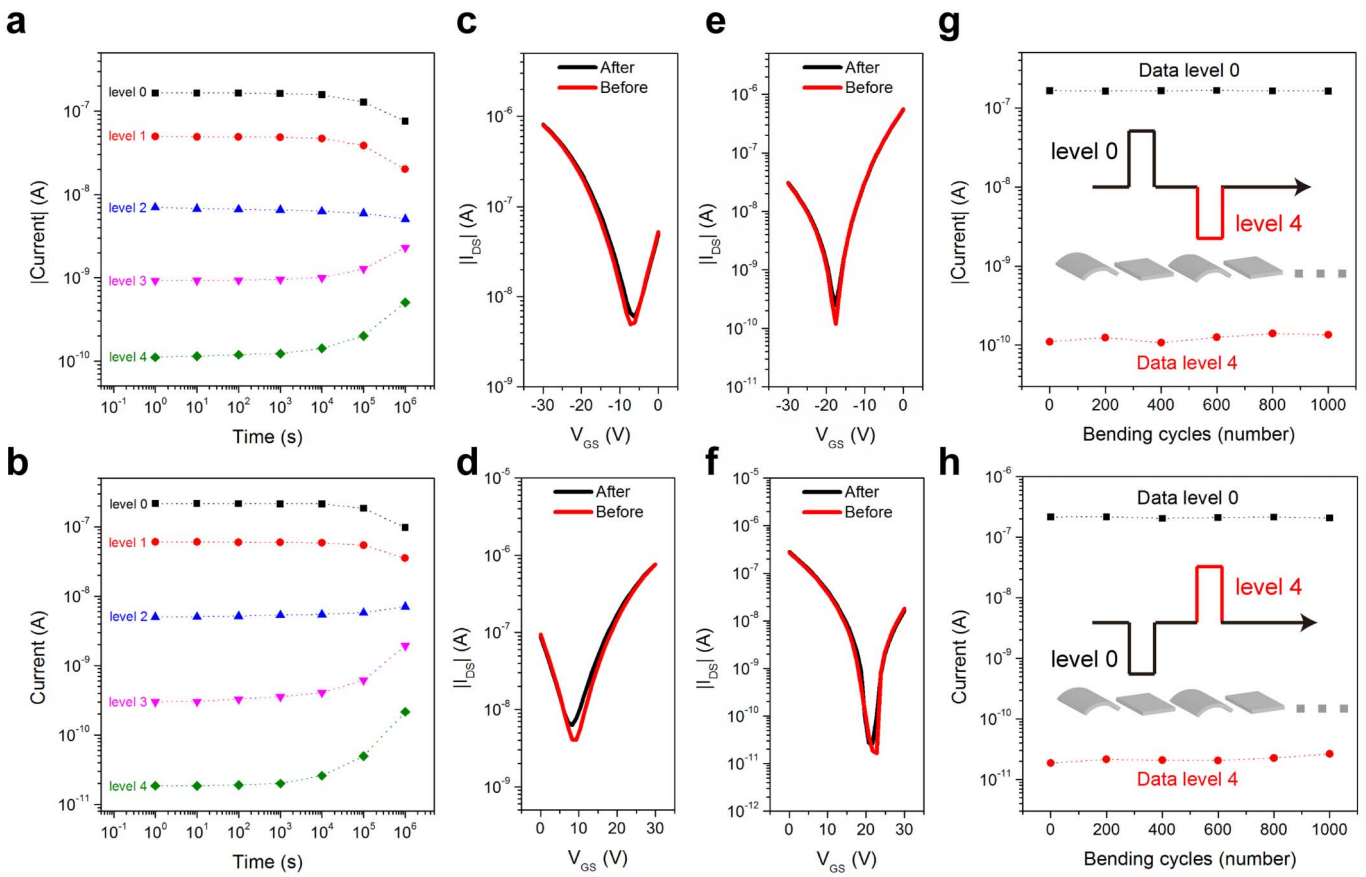

Figure 4 | (a) Retention properties of the data levels in hole-enhancement mode. (b) Retention properties of the data levels in electron-enhancement mode. (c) Transfer characteristics of data level 0 in hole-enhancement mode before and after bending the substrate. (d) Transfer characteristics of data level 0 in electron-enhancement mode before and after bending the substrate. (e) Transfer characteristics of data level 4 in hole-enhancement mode before and after bending the substrate. (f) Transfer characteristics of data level 4 in electron-enhancement mode before and after bending the substrate. (g) Bending stability of data level 0 and 4 in hole-enhancement mode. (h) Bending stability of data level 0 and 4 in electron-enhancement mode.

concept of ambipolar trapping hence an enhancement in memory window compared with the unipolar devices (Fig. S4). The large memory window in ambipolar device is achieved by the transformation of different trapping states, from hole trapping to electron trapping or from electron trapping to hole trapping. In the unipolar trapping system, the memory behavior is achieved by trapping and releasing only one kind of charge carriers. The balanced hole and electron mobilities in our ambipolar materials would facilitate achieving wide range shift of the transfer curves in both positive and negative direction and result in large changes in current levels. Our proposed structure can also be applied to various types of trapping elements for ambipolar charge trapping mechanism.

In order to investigate the effect of charge mobility on memory characteristics, we annealed the devices at high temperature (200°C) that are fabricated on rigid substrates (heavily doped Si wafer) with same device architecture. The memory transistors exhibited higher mobility than that of devices annealed at low (160°C) temperature (Fig. S8 and S9). Although the current level of 200°C annealed device is an order magnitude higher than that of 160°C annealed device, the reading current ratio before and after programming the high mobility device is similar with the low mobility device. Therefore, we conclude that there is no obvious improvement in the multi-level memory characteristics. In ambipolar memory, the current levels are used to differentiate various data states. Enhanced memory properties could be achieved by increasing the reading current ratio so that more data levels could be introduced. Further improvement of ambipolar transistor performance can be achieved by adopting high mobility ambipolar materials with high on/off current ratios and good air stability.

The working voltage of the memory device could be further reduced to 10 V by applying thin blocking dielectric layer, which is another advantage compared with previously reported high voltage polymer ambipolar devices[46–48]. Furthermore, we fabricated the metal-insulator-semiconductor (MIS) structure to investigate the charge trapping density in the ambipolar memory. The capacitance-voltage curve of the MIS device is shown in Fig. S10. From the shift of the flatband voltage (ΔV_{FB}), we can estimate the charge trapping density using the equation $Q = C_i \Delta V_{FB}$, where C_i is the capacitance of the dielectric layer. The charge trapping density in the process is estimated to be about 4.9×10^{12} cm^{-2} while the density of the Au nanoparticles is about 3.2×10^{11} cm^{-2}. Therefore, in the ambiplar trapping process there are about 15 charge carriers trapped in each Au nanoparticle.

To evaluate the reliability of the memory, we test the multilevel operation in both hole-enhancement region and electron-enhancement region. We have realized the hole and electron trapping through different program/erase pulses, which is our proposed concept to get different data levels. The advantage of an ambipolar device is that it could work in two regions and we can choose one of the regions to operate. The data levels can be set only by the program/erase pulse, one data level in the hole-enhancement region has a corresponding level in the electron-enhancement region, and vice versa.

In conclusion, we successfully demonstrate a multilevel data storage memory based on a solution-processable single-component ambipolar polymer. Ambipolar polymer semiconducting layer has an ability to transport both electrons and holes in a balanced manner. This provides an opportunity for the charge trapping layer (metal nanoparticles in aluminum oxide) to trap both electrons and holes efficiently. Therefore, we obtained a wide memory window with tunable electrical behavior which is not possible with unipolar semiconductors. Due to a wide memory window, five data levels with well separated data sensing margins have been realized in the memory transistor. The memory device exhibit reliable data retention capability, endurance property and mechanical flexibility. The methods for generating charge trapping layer and semiconductor layer are based on solution processed technique, which could be readily adopted in large area flexible electronics to achieve low-cost device fabrication. Furthermore, our approach offers new opportunities to fabricate novel multi-bit flash memory for printed electronics and may show promising applications in advanced electronic devices.

Methods

Materials. The following materials were obtained from Aldrich: auric acid ($HAuCl_4 \cdot 3H_2O$), trisodium citrate (Na_3Ct), sodium borohydride ($NaBH_4$), APTES and P3HT. All chemicals and solvents were used without further purification.

Preparation of Au nanoparticle monolayer. The Au NPs colloidal solution was prepared by the reduction of $HAuCl_4 \cdot 3H_2O$ (0.25 mM in 20 ml) by ice-cold 0.6 mL $NaBH_4$ (0.1 M) in the presence of Na_3Ct (0.25 mM). After routine solvent cleaning and drying under nitrogen gas, the substrates coated with Al_2O_3 were immersed in a solution of ethonal containing 0.1 v/v% APTES for 45 mins at room temperature. Then, the functionalized substrates were dipped into 5 nm Au colloidal solutions for 12 hours.

Device fabrication and characterization. Ambipolar memory devices were fabricated on 200 μm PET film with 100 nm indium tin oxide (ITO) as gate electrode. Al_2O_3 layers were deposited using a Savannah 100 ALD system at a substrate temperature of 80°C. The formation of of Au nanoparticle monolayer is described in supporting information. Thin films of PDPP-TBT were deposited on Al_2O_3 by spin-coating using a polymer solution (7 mg ml^{-1}) in chloroform, followed by thermal annealing at 160°C under nitrogen environment. Gold electrodes (50 nm) were thermally evaporated through a shadow mask with a channel length (L) of 50 μm and width (W) of 1000 μm at a rate of 0.2 Å/s and under a base pressure of 3×10^{-6} Torr. Au nanoparticle monolayer was confirmed by a field emission scanning electron microscope (FE-SEM, JEOL JSM-6335F). The thicknesses of the deposited layers were measured using the ellipsometer. The morphologies of these films were investigated by atomic force microscope (AFM, Veeco Multimode V). The capacitances were measured by a HP 4284A LCR meter at 1 KHz with an AC amplitude of 50 mV superimposed on the DC bias. The electrical characteristics of the transistors were measured using a Keithley 2612 source meter and an Agilent 4155C semiconductor analyzer at room temperature in a nitrogen glove box.

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Author contributions

Y.Z. and S.T.H. planned and performed the experiments. P.S. synthesized the polymer material. V.A.L.R. supervised the project and finalized the manuscript.

Additional information

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