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Metal-Semiconductor Barrier Modulation for High Photoresponse in Transition Metal Dichalcogenide Field Effect Transistors

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A gate-controlled metal-semiconductor barrier modulation and its effect on carrier transport were investigated in two-dimensional (2D) transition metal dichalcogenide (TMDC) field effect transistors (FETs). A strong photoresponse was observed in both unipolar MoS_2 and ambipolar WSe_2 FETs (i) at the high drain voltage due to a high electric field along the channel for separating photo-excited charge carriers and (ii) at the certain gate voltage due to the optimized barriers for the collection of photo-excited charge carriers at metal contacts. The effective barrier height between Ti/Au and TMDCs was estimated by a low temperature measurement. An ohmic contact behavior and drain-induced barrier lowering (DIBL) were clearly observed in MoS_2 FET. In contrast, a Schottky-to-ohmic contact transition was observed in WSe_2 FET as the gate voltage increases, due to the change of majority carrier transport from holes to electrons. The gate-dependent barrier modulation effectively controls the carrier transport, demonstrating its great potential in 2D TMDCs for electronic and optoelectronic applications.

Compared to graphene which cannot achieve the low off-state and saturated on-state currents due to its zero bandgap[1–3], transition metal dichalcogenides (TMDCs) have opened up new opportunities for two-dimensional (2D) electronics and optoelectronics such as transistors[4,5], memories[6,7], integrated circuits[8,9], photodetectors[10,11], and electro-luminescent devices[12] etc., because of their selectable electronic properties ranging from metallic to semiconducting, and tunable bandgaps with layer-dependence[13,14]. Particularly for semi-conducting TMDCs such as MoX_2 and WX_2 compounds (X is a chalcogen), their sub-nanometer thickness with sizable bandgaps around 1–2 eV can provide high on/off ratios and more efficient control over switching. The immunity of short-channel effect and ultralow power dissipation which are made possible by using 2D materials can break through the scaling limit for future transistor miniaturization[15,16]. For example, MoS_2 as a representative *n*-type semiconducting TMDC has an indirect bandgap of 1.3 eV in bulk structure but a direct bandgap of 1.8 eV in single-layer form[13]. Owing to the thickness-dependent bandgap modulation, the triple-layer MoS_2 shows a strong photoresponse for red light detection, while the single- and double-layer MoS_2 are preferred for green light detection[11]. The direct bandgap in single-layer MoS_2 also gives rise to photo- and electro-luminescence, posing the potential for novel 2D optoelectronic devices such as light detectors and emitters[12]. Another example, WSe_2 with the bandgap of 1.2 eV in bulk structure and 1.7 eV in single-layer form[13] has also been studied for transistor[17,18] and photovoltaic applications[13]. Although carrier mobility of MoS_2 and WSe_2 are relatively low, it can be improved significantly by the optimized or chemically doped metal contacts[17,19], dielectric engineering via high-*k* materials[4,17], and formation of an inversion channel[5] etc.

In this work, both few-layer MoS_2 and WSe_2 flakes were applied to the back-gate field effect transistors (FETs) with Ti/Au metallization, and their carrier transport was investigated over a wide range of drain voltage (0 to 5 V) and gate voltage (−50 to 50 V) to demonstrate its strong dependency on bias modulation. To understand the modulation effects more clearly, we investigated the formation of Schottky and ohmic contacts from the MoS_2 and WSe_2 FETs, by measuring the energy barriers of the carriers at the contacts and relating them to the carrier transport and photo-response of these FETs.

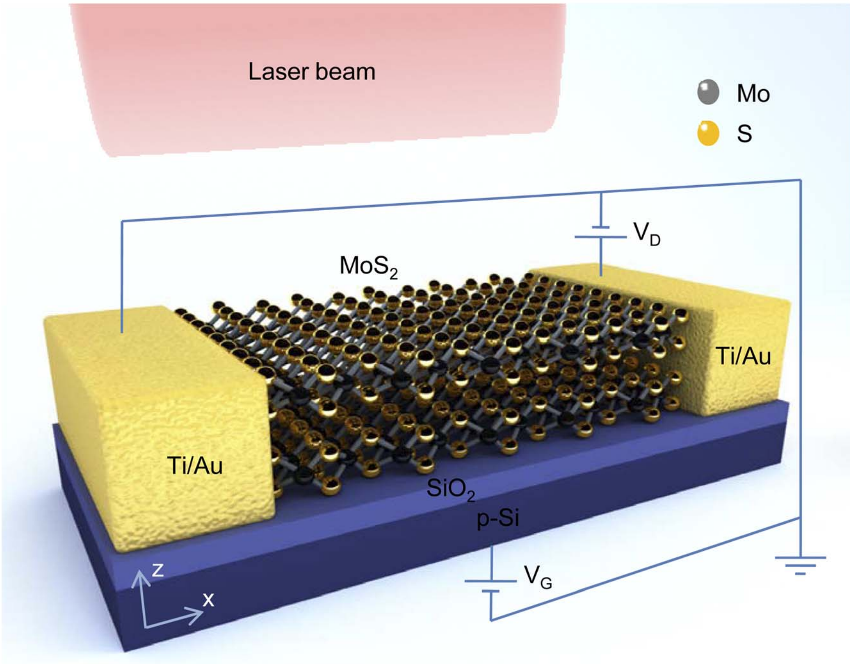

Figure 1 | **TMDC FETs under laser illumination.** Schematic perspective view and circuit diagram of a TMDC FET under laser illumination with few-layer MoS_2 as channel layer.

Results

Thin MoS_2 and WSe_2 flakes are obtained by mechanical exfoliation from the bulk crystals, and transferred to a *p*-type Si substrate (1.0–10.0 Ωcm) with 90-nm-thick thermally grown SiO_2 surfaces. The back-gate FET devices are fabricated via electron beam lithography (EBL) with Ti/Au (5 nm/50 nm) electrodes deposited by electron beam evaporation, as shown in Fig. 1. The MoS_2 flake has the thickness of ~3 nm measured by atomic force microscopy (AFM), and its Raman spectrum shows two typical peaks (E_{2g}^1 and A_{1g}) with a large separation of 23 cm^{-1}. The WSe_2 flake has the thickness of ~9 nm, and only shows a single peak at around 250 cm^{-1} [20] (Supplementary Information Fig. S1). These suggest the few-layer structure of both MoS_2 and WSe_2 flakes.

The electrical characterization of MoS_2 and WSe_2 FETs is performed by a semiconductor parameter analyzer in a vacuum condition (10 mTorr) at the room temperature. The optoelectronic performance is analyzed by combining a dot laser (655 nm, 15 mW) illuminating system, where the photocurrent (PC) signal is defined as the difference of drain current (I_D) in dark and laser illuminating environments at certain drain and gate voltages (V_D and V_G). The I_D-V_G transfer characteristics of MoS_2 FET illustrate an *n*-type unipolar carrier transport. As a comparison, an asymmetric ambipolar transport with the dominant electron conduction is observed in WSe_2 FET. The trapping-induced hysteresis with voltage shift of 2 and 10 V suggests an equivalent trap density of 4.79×10^{11} and 2.40×10^{12} cm^{-2} in MoS_2 and WSe_2 FETs, respectively[21] (Supplementary Information Fig. S2). Before measuring the PC of TMDC FETs, a calibration is performed by measuring the photoresponse of metal and metal/SiO_2 interface. The identical electrical performance in both dark and illuminating environments excludes the photoresponsive contributions of metal and metal/SiO_2 interface, and suggests that all the PCs are generated in TMDC FETs.

The carrier transport in both MoS_2 and WSe_2 FETs is investigated over a wide range of V_D (0 to 5 V) and V_G (−50 to 50 V), as shown in Fig. 2 for MoS_2 FET and in Fig. 3 for WSe_2 FET. In the dark environment, the carrier transport is maximized at the high V_G (50 V) and V_D (5 V) levels in both MoS_2 and WSe_2 FETs due to the high carrier density induced by electrical gating and the high electric field along the channel for carrier drift, respectively. This is consistent with the carrier transport theory in conventional semiconductor FETs. As a comparison, it is interesting to find out that the PC generation in both MoS_2 and WSe_2 FETs is not proportional to the carrier transport in dark environment. The PC peaks under illumination are located at the high V_D (5 V in both MoS_2 and WSe_2 FETs), owing to the high electric field along the channel for separating the photo-excited charge carriers. However, the PC peaks are located at the different certain V_G (~0 V in MoS_2 FET and ~20 V in WSe_2 FET), not at the V_G of the maximized carrier transport (~50 V in both MoS_2 and WSe_2 FETs). Therefore, the conventional carrier transport theory is not suitable to explain the transport of photo-excited charge carriers, and thus a new mechanism is required to interpret the gate-dependent photoresponse in TMDCs.

Discussion

A gate-controlled metal-semiconductor barrier modulation is proposed to interpret the carrier transport of both MoS_2 and WSe_2 under illumination. Here we take the MoS_2 FET as an example due to its unipolar carrier transport which is simpler compared to the case of ambipolar WSe_2 FET. Firstly, the energy band diagrams of MoS_2 FET illustrate the electrical gating effect along the vertical axis for various V_G conditions, as shown in Fig. 4(a). When $V_G > 0$, the electrons are attracted to the interface between MoS_2 and SiO_2 to form an accumulation layer. When $V_G < 0$, the electrons are repelled from the interface to establish a depletion layer. Further increasing the negative V_G may create an inversion channel which gives rise to the high mobilities[5]. Secondly, the metal-semiconductor barriers at both source and drain ends are modulated capacitively by the gate, as shown in Fig. 4(b). The barriers are induced due to a mismatch between the workfunctions of MoS_2 and Ti, and they can be enlarged or reduced by applying the negative or positive V_G, respectively. The barrier height (ϕ_{ms}) at the equilibrium can be theoretically estimated as $\Phi_M - \chi$[22], where Φ_M is the work function of Ti (4.3 eV), and χ is the electron affinity of MoS_2 (4.0 eV)[19]. In MoS_2 FET, ϕ_{ms} is estimated as 0.3 eV, which is in agreement with the theoretical estimation[22,23] and experimental results obtained by temperature-dependent electrical

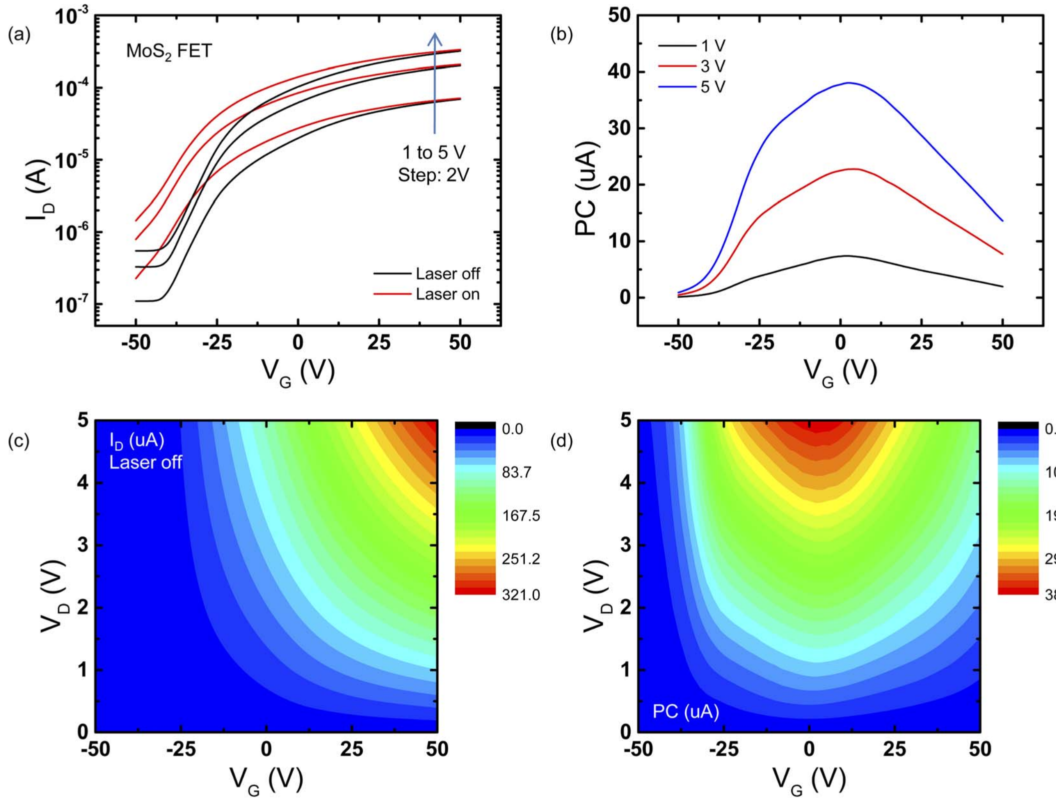

Figure 2 | Photoresponse of transfer characteristic in MoS_2 FET. (a), (b) Transfer characteristic of MoS_2 FET in dark and illuminating environments in forward sweep for various V_D levels, and the corresponding PCs. (c), (d) Mapping of dark current (laser off) and PC as functions of V_D and V_G.

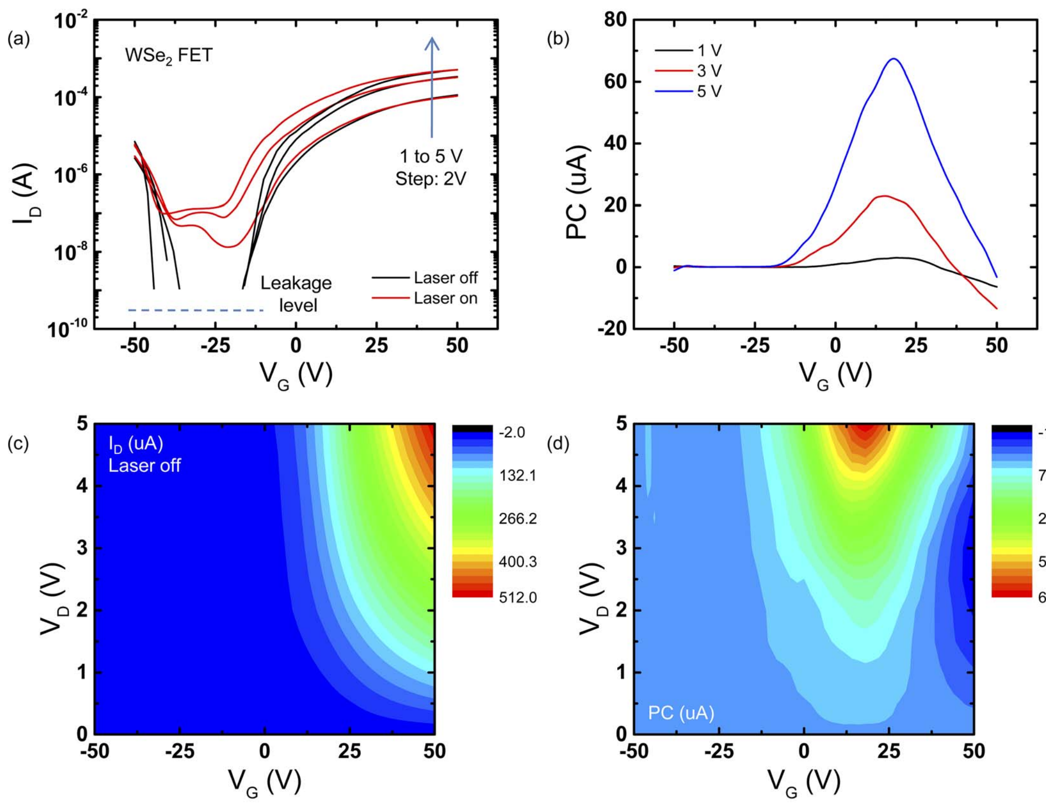

Figure 3 | Photoresponse of transfer characteristic in WSe_2 FET. (a), (b) Transfer characteristic of WSe_2 FET in dark and illuminating environments in forward sweep for various V_D levels, and the corresponding PCs. (c), (d) Mapping of dark current (laser off) and PC as functions of V_D and V_G.

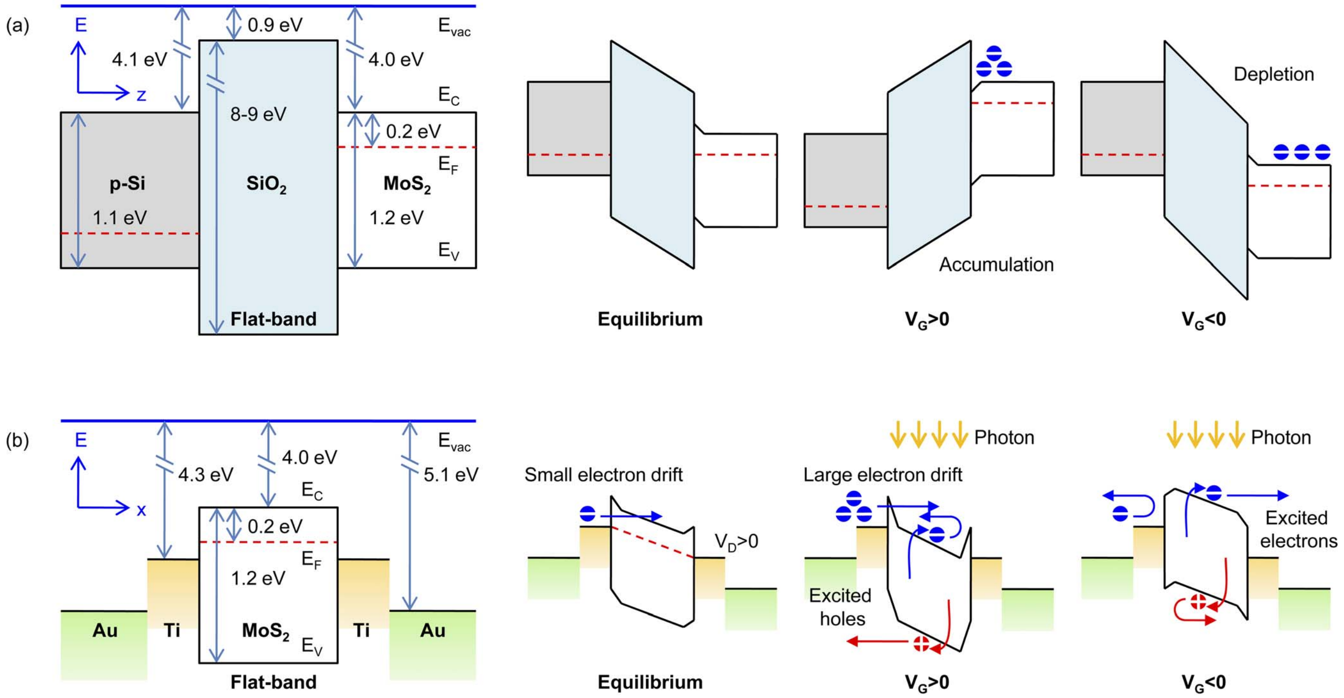

Figure 4 | Energy band diagrams of MoS_2 FET. The energy band diagrams along (a) the vertical axis (z) and (b) the horizontal axis (x) illustrate various gating conditions, including flat-band, equilibrium ($V_G = 0$), accumulation ($V_G > 0$) and depletion ($V_G < 0$). The blue solid line and red dash line denote the vacuum and Fermi levels, respectively. The blue and red arrows indicate the transport of electrons and holes.

measurements[8,19,24,25] previously. Thirdly, the carrier transports in both dark and illuminating environments are strongly affected by the gate-dependent barrier modulation. For the electron drift along the channel driven by a positive V_D, the barriers are reduced with increasing V_G, allowing the electrons to transport through by tunneling effect or thermionic emission in the dark environment. As a comparison, for the photon-excited charge carriers generated within the channel under illumination, the barriers only allow the electron collection at the drain end, but suppress the hole collection at the source end when $V_G < 0$, and vice versa when $V_G > 0$. Therefore, the PC generation is still relatively small at the high positive and negative V_G levels due to the inefficient carrier collection. However, there should be an optimized V_G condition where the barriers for both electron and hole collection are minimized at the source and drain ends concurrently, contributing to a peak PC generation. This gate-controlled barrier modulation can thoroughly interpret the gate-dependent photoresponse of MoS_2 FET, as shown in Fig. 5. Similarly, it can also be applied to WSe_2 FET due to the analogous energy bandgap. Finally, the channel current under illumination, which is the sum of both dark current and PC, shows the gate dependence following a combined barrier modulation for both electron drift and photo-excited charge carriers.

To quantitatively analyze the barrier modulation, the effective value of (ϕ_{ms}) between metal and TMDC is obtained by testing the temperature dependence of channel current[25,26]. A typical ohmic contact behavior in the I_D-V_D output characteristics of MoS_2 FET and its photoresponse are observed at various V_G levels, as shown in Fig. 6. For the carrier transport through a metal-semiconductor barrier, the tunneling effect dominates when the semiconductor is highly doped, whereas the thermionic emission dominates when the semiconductor is slightly or moderately doped. Since the MoS_2 is intrinsic in this work, the current-voltage relation is determined by thermionic emission as[26]

$$I_D = AA^*T^2 \exp\left(\frac{-\phi_{ms}}{k_BT}\right)\left[\exp\left(\frac{-qV_D}{k_BT}\right)-1\right] \qquad (1)$$

where A is the area of the contact junction, A^* is the effective Richardson constant, q is the electronic charge, k_B is the Boltzmann constant, and T is the temperature. Considering the electron transport from the source to the drain ends, a back-to-back metal-semiconductor-metal contact is formed, and the carrier transport is mainly affected by the contact condition at the drain end due to the applied V_D. Under a high V_D, the contact at the drain end is reversely biased [$\exp(-qV_D/k_BT) \ll 1$], and I_D becomes proportional to $T^2\exp(-\phi_{ms}/k_BT)$. A linear relation between $\ln(I_D/T^2)$ and q/k_BT can be plotted for various V_G levels, and the gate-dependent ϕ_{ms} for a given V_D is estimated from the slope of each curve, as shown in Fig. 7. ϕ_{ms} has a very low value

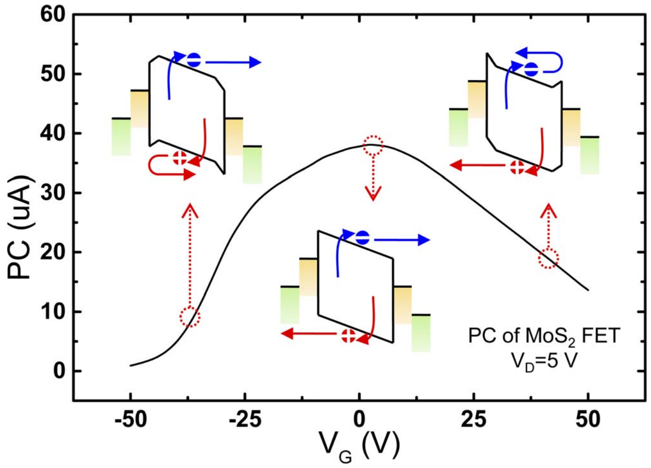

Figure 5 | Gate-dependent barrier modulation in MoS_2 FET. The barriers at both source and drain ends can be minimized at certain V_G, which promote the collection of photo-excited charge carriers and contribute to a PC peak. The PC generation as a function of V_G in WSe_2 FET can also be interpreted analogously.

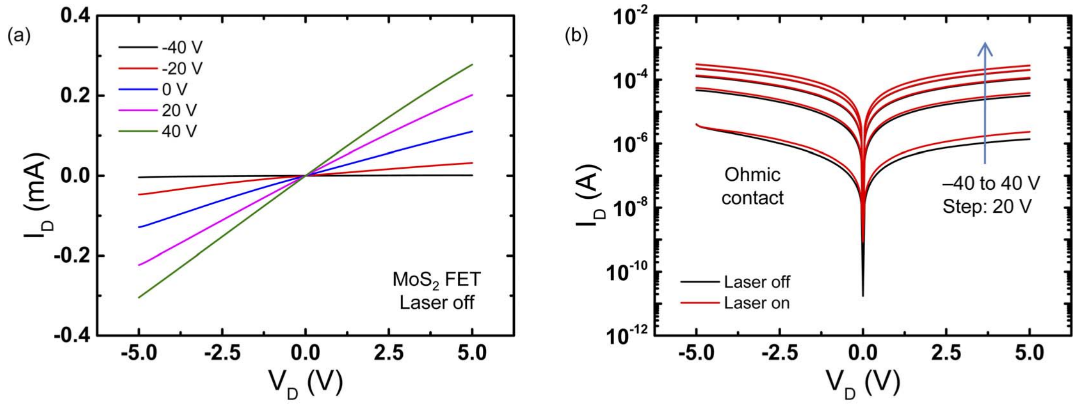

Figure 6 | Ohmic contact and its photoresponse in MoS_2 FET. (a), (b) Output characteristic of MoS_2 FET for various V_G levels in linear scale and its photoresponse in logarithmic scale, suggesting an ohmic contact behavior.

on the order of 10 meV, which is in agreement with the presence of ohmic contact. ϕ_{ms} also shows a reduction as V_G increases, being consistent with the barrier modulation theory. Moreover, a reduction of ϕ_{ms} with increasing V_D is clearly observed near zero gate voltage, suggesting a drain-induced barrier lowering (DIBL) effect in MoS_2 FET. Besides, it is noted that ϕ_{ms} is reduced at very high negative V_G. This may be induced by the increased minority carrier density during the formation of inversion layer.

For the WSe_2 FET, a transition from Schottky to ohmic contact is observed, as shown in Fig. 8. The current-voltage relation shows the Schottky contact behavior with opposite polarities at V_G of -40 and -20 V, but then shows the ohmic contact behavior as V_G increases from 0 V to 40 V. Considering the ambipolar transport of WSe_2, this Schottky-to-ohmic contact transition may be induced by the change of majority carrier transport from holes at negative V_G to electrons at positive V_G (see Fig. 3(a)). The experimental value of ϕ_{ms} is obtained as a function of V_G, as shown in Fig. 9. ϕ_{ms} shows a dip near -40 V and a peak near -20 V, indicating the Schottky contact with opposite polarities. As V_G increases further, the value of ϕ_{ms} is reduced from the order of 100 to 10 meV, suggesting a transition from Schottky to ohmic contact.

In conclusion, the bias-controlled barrier modulation in TMDC FETs and its effect on carrier transport were investigated over a wide range of gate and drain voltages. Being disproportionate to the conventional carrier transport in dark environment, a strong photoresponse was observed at the certain gate and drain voltages due to the change in barrier heights between metal and TMDC materials which resulted in ohmic contact or Schottky contact. The gate-dependent

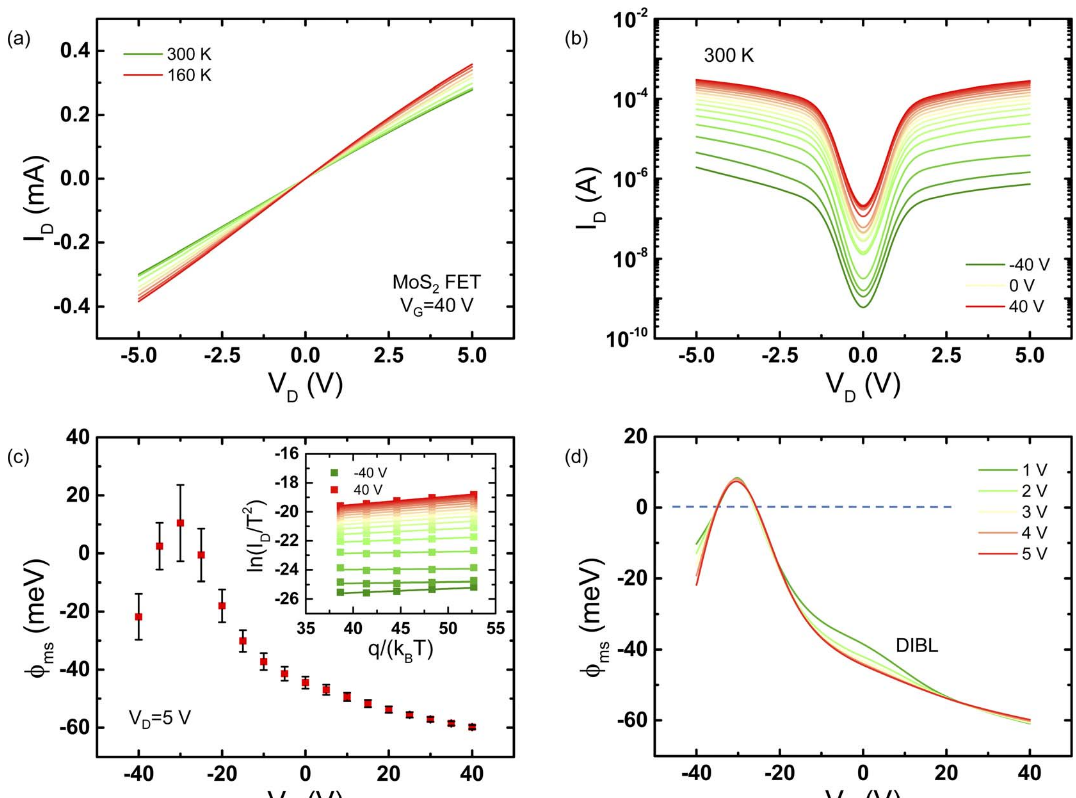

Figure 7 | Extraction of barrier height in MoS_2 FET. (a), (b) Output characteristic of MoS_2 FET for various temperatures (160 to 300 K with a step of 20 K) and V_G (-40 to 40 V with a step of 5 V) levels. (c), (d) Effective barrier height as a function of V_G for various V_D levels. Inset of (c): Temperature-dependent current characteristics and their corresponding linear fit for various V_G levels at V_D of 5 V.

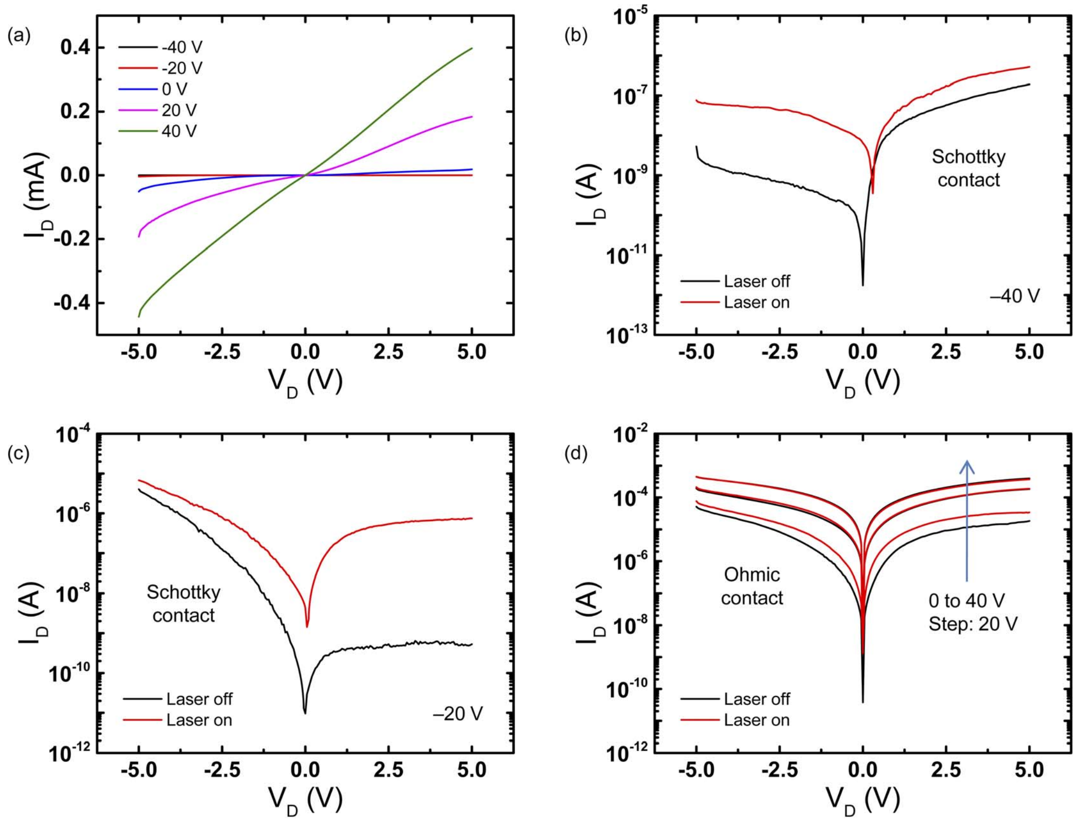

Figure 8 | A Schottky-to-ohmic contact transition and its photoresponse in WSe_2 FET. (a) Output characteristic of WSe_2 FET for various V_G levels in linear scale. (b–d) Photoresponse of output characteristic in logarithmic scale indicates a transition from Schottky contact to ohmic contact as V_G increases.

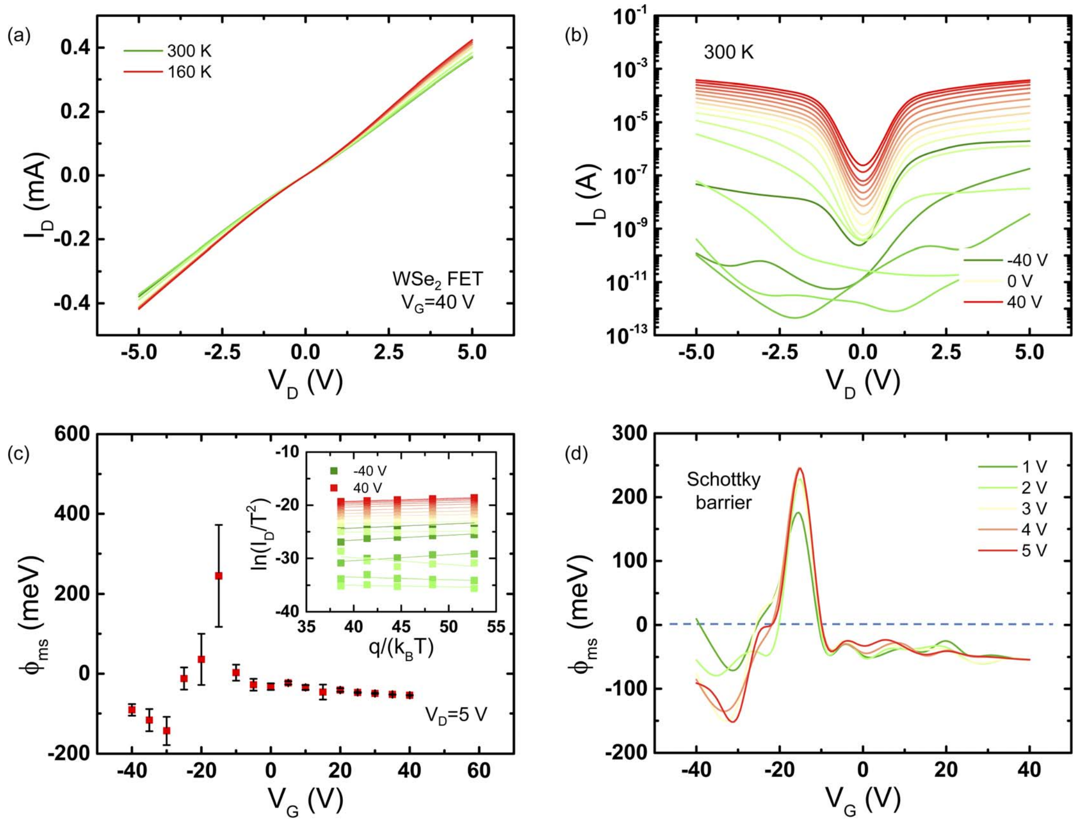

Figure 9 | Extraction of barrier height in WSe_2 FET. (a), (b) Output characteristic of WSe_2 FET for various temperatures (160 to 300 K with a step of 20 K) and V_G (−40 to 40 V with a step of 5 V) levels. (c), (d) Effective barrier height as a function of V_G for various V_D levels. Inset of (c): Temperature-dependent current characteristics and their corresponding linear fit for various V_G levels at V_D of 5 V.

barrier modulation effectively controlled the carrier transport in MoS_2 and WSe_2.

Methods

Fabrication of TMDC FET devices. Both MoS_2 and WSe_2 thin flakes were mechanically exfoliated from bulk crystals by using scotch tapes. Before the transfer procedure, the silicon wafer was pre-cleaned by sonication in acetone, isopropyl alcohol, and deionized water, followed by drying in nitrogen flow and heating on hot plate to remove the moisture. Electrodes were patterned by standard EBL procedure. 5-nm-thick Ti and 50-nm-thick Au were deposited by electron beam evaporation, followed by a post-annealing in N_2 environment at 300°C for 1 hour to improve the metal contact.

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Acknowledgments

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Author contributions

H.M.L. and W.J.Y. conceived the research project, supervised the experiment and wrote the paper. H.M.L., D.Y.L. and M.S.C. performed device fabrication. H.M.L. performed electrical and optoelectronic characterization. D.Q. performed AFM analysis. X.L. performed theoretical simulation. C.H.R. performed Raman spectrum analysis.

Additional information

Supplementary information accompanies this paper at http://www.nature.com/scientificreports

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