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A High Frequency Active Voltage Doubler in Standard CMOS Using Offset-Controlled Comparators for Inductive Power Transmission

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Abstract

In this paper, we present a fully integrated active voltage doubler in CMOS technology using offset-controlled high speed comparators for extending the range of inductive power transmission to implantable microelectronic devices (IMD) and radio-frequency identification (RFID) tags. This active voltage doubler provides considerably higher power conversion efficiency (PCE) and lower dropout voltage compared to its passive counterpart and requires lower input voltage than active rectifiers, leading to reliable and efficient operation with weakly coupled inductive links. The offset-controlled functions in the comparators compensate for turn-on and turn-off delays to not only maximize the forward charging current to the load but also minimize the back current, optimizing PCE in the high frequency (HF) band. We fabricated the active voltage doubler in a 0.5-μm 3M2P std. CMOS process, occupying 0.144 mm^2 of chip area. With 1.46 V peak AC input at 13.56 MHz, the active voltage doubler provides 2.4 V DC output across a 1 kΩ load, achieving the highest PCE = 79% ever reported at this frequency. In addition, the built-in start-up circuit ensures a reliable operation at lower voltages.

Keywords

Active voltage doubler; high speed comparators; implantable microelectronic devices; inductive power transmission; integrated rectifier; near field; offset control; radio-frequency identification (RFID)

I. Introduction

IMPLANTABLE microelectronic devices (IMD) have already been used successfully in the form of cochlear implants to substitute a sensory modality (hearing) that might be lost due to diseases or injuries [1]. More recent IMD applications demand higher performance and more power efficiency to enable very sophisticated treatment paradigms, such as retinal implants for the blind or bidirectional cortical brain-computer-interfaces (BCI) with sensory feedback for amputees or those suffering from severe paralysis [2]–[4]. These IMDs require more power to handle more functions on a larger scale, particularly when they need stimulation through a large number of electrodes at high rates, which power level is less dependent on the circuit efficiency [5]. Therefore, the new IMD power consumption is going to be orders of magnitude higher than more traditional IMDs, e.g., pacemakers [6], and supplying them with primary batteries will not be an option. Inductive power transmission across the skin is, however, a viable solution to overcome size, cost, and longevity while providing sufficient power to such IMDs [5], [7]–[9]. Considering that the temperature at the outer surface of the IMD should not increase more than 2°C for the surrounding tissue to survive [10], it is of utmost importance for the inductive link and the IMD power management circuitry to maintain very high power transfer efficiency. There are also other applications such as

inductively powered wireless sensors, radio frequency identification (RFID), and near-field communication (NFC), in which the size and cost of neither primary nor secondary (i.e., rechargeable) batteries are justified, while high power efficiency and robustness even through weak inductive links are highly desired [11], [12].

Fig. 1 shows the block diagram of an inductively-powered IMD with emphasis on the inductive power transmission that consists of three main components: power transmitter (Tx), inductive link, and IMD (Rx). On the Tx side, the primary coil, L_1, is driven by a power amplifier (PA) at the carrier frequency, f_c. This signal induces power in the secondary coil, L_2, and the active voltage doubler converts the AC voltage in L_2C_2 tank to a DC voltage (V_{OUT}) at higher levels than the peak input voltage.

The size of L_2 is significantly constrained when it is meant to be implantable in the human body or embedded in a small RFID tag, resulting in small L_2 value and low V_{IN} [13]–[15]. There are also IMDs under development, in which the secondary coil has to be embedded in the stimulator package (e.g., to be injectable) or directly implemented on the backside of the microelectrode array to facilitate the system microassembly and packaging by eliminating the flex cable that would otherwise be needed to place L_2 under the skin [16], [17]. In such cases, the distance between L_1 and L_2 can be considerably larger than the size of L_2, significantly limiting V_{IN}. This condition renders even the most efficient rectifiers either ineffective or highly inefficient. Thus, similar to far field RFID tags in the UHF band, in order to generate the desired V_{OUT} from a small V_{IN} while maintaining high efficiency, a viable solution could be using voltage doublers which can operate at lower $V_{IN,peak}$ while providing sufficient V_{OUT}. This can also increase the read range in the RFID tags that operate in the HF band.

Both rectifiers and voltage doublers have been widely used for inductively-powered applications. Passive rectifiers and voltage doublers using diode-connected transistors suffer from large forward voltage drops and power losses because of their threshold voltages [9], [18]–[22]. A bridge rectifier using Schottky diodes has low dropout voltage [23], but it has high leakage current and it is not available in a standard CMOS process without extra fabrication steps. In addition, its reverse breakdown voltage may not be high enough for stimulation applications. Several V_{Th} compensation techniques have been proposed to reduce the effective V_{Th} [24]–[29]. However, they still need to deal with several issues such as sensitivity to process variations, leakage, and back currents.

Synchronous active rectifiers have achieved high power conversion efficiency (PCE) because their pass transistors operate as switches in deep triode region with low dropout voltages [30]–[44]. However, their peak input voltages, which may be significantly limited by weakly coupled inductive links, need to be always higher than the desired output voltages, resulting in lower operating range or higher voltages on the Tx side. In order to address such limitations, comparator-based active voltage doublers have been recently proposed [45], [46]. However, these topologies only operate at low frequencies (< 1 kHz) in applications such as energy scavenging from vibrations using piezoelectric transducers. Improved voltage doublers are required for IMD and RFID applications with inductive links that operate within the HF band, such as 13.56 MHz, in the Industrial, Scientific, and Medical (ISM) band.

In this paper, we propose a fully-integrated power-efficient active voltage doubler employing high speed comparators for inductively-powered applications such as IMD, RFID, and NFC. Comparators are equipped with offset control functions to compensate for both turn-on and turn-off delays. The active voltage doubler achieves high PCE comparable to the active rectifiers while generating the desired DC output voltage with much lower AC

inputs than either active rectifiers or passive voltage doublers. Section II describes the concept, operating principle, and PCE analysis of the active voltage doubler. Section III presents circuit details and design considerations including the effects of the proposed offset-control functions in high speed comparators. Simulation and measurement results are in Section IV, followed by conclusions in Section V.

II. Active Voltage Doubler Architecture

A. Operating Principle of the Voltage Doubler

Fig. 2 shows the topology of the conventional passive voltage doubler using either diodes or diode-connected transistors. It consists of one capacitor, C_{IN}, and two diodes, D_N and D_P, with forward dropout voltages of V_{DN} and V_{DP}, respectively. Rectified output voltage, V_{OUT}, is low pass filtered by C_L, and supplies the load resistor, R_L. The sinusoidal input voltage, V_{IN}, generated across the secondary resonance circuit, L_2C_2, has a peak amplitude of $V_{IN,peak}$, which depends on the inductive link parameters and V_{PA} at the output of the power amplifier (PA), shown in Fig. 1 [14].

When V_{IN} goes below $-V_{DN}$, V_{VD} is connected V_{SS} to through D_N, and C_{IN} is charged to $V_{IN,peak} - V_{DN}$, with V_{VD} as the positive node. When V_{IN} increases above $-V_{IN,peak}$, D_N turns off again and the isolated V_{VD} increases by following $V_{IN,peak} - V_{DN} + V_{IN}$. When $V_{VD} > V_{OUT} + V_{DP}$, D_P turns on and current flows from V_{IN} to V_{OUT} to charge the R_LC_L load. In this step, the charge stored in C_{IN} decreases by the amount of charge delivered to the load, but C_{IN} is charged again to $V_{IN,peak} - V_{DN}$ in the next cycle. Due to the dropout voltage across D_P, V_{OUT} can reach a maximum voltage of $2V_{IN,peak} - V_{DN} - V_{DP}$. The total dropout voltage of the voltage doubler, V_{Drop}, can be calculated from

$$V_{Drop}=2V_{IN,peak} - V_{OUT}=V_{DN}+V_{DP}. \quad (1)$$

This equation shows that the diode dropout voltages, V_{DN} and V_{DP}, directly affect the voltage doubler output voltage and consequently its PCE. Thus, substituting them with fast MOS switches with low on-resistance and leakage would be an effective way of reducing V_{Drop} and improving the PCE.

B. Implementation of the Active Voltage Doubler

Fig. 3 shows a simplified schematic diagram of the proposed active voltage doubler, in which two pass transistor switches, N_1 and P_1, are driven by high-speed comparators, CMP_N and CMP_P, respectively. When $V_{VD} < V_{SS}$, CMP_N output goes high, N_1 turns on with a low dropout voltage, $V_{DS(N1)}$, and C_{IN} is charged to $V_{IN,peak} - V_{DS(N1)}$ in the shown polarity. Similarly, when $V_{VD} < V_{OUT}$, CMP_P output goes low, P_1 turns on with a low dropout voltage, $V_{SD(P1)}$, and current flows through P_1 to charge R_LC_L in the shown polarity. Therefore, after a few cycles, V_{OUT} is charged up to $2V_{IN,peak} - V_{DS(N1)} - V_{SD(P1)}$, and the total dropout voltage, $V_{Drop} = V_{DS(N1)} + V_{SD(P1)}$, which results from the instantaneous input current flowing through the on-resistance of N_1 and P_1, will be much smaller than that of the passive voltage doubler in Fig. 2 ($V_{GS(N)} + V_{SG(P)}$).

To drive N_1 and P_1 at high frequencies in the order of 13.56 MHz, comparators are equipped with internal offset-control functions that are externally adjustable (CTL0:3) to reduce the effects of the comparators' delay. Also, the separated N-well body terminal of P_1 needs to be connected to the highest potential on the chip to prevent latch-up and substrate leakage problems. Therefore, in Fig. 3 we have adopted the dynamic body biasing technique from [18] with auxiliary transistors, P_3 and P_4, automatically connecting V_{BODY} to the highest potential between V_{VD} and V_{OUT}.

Since the comparators are supplied from V_{OUT}, which is initially at 0 V, it is necessary for the active voltage doubler to have startup capability. The startup block in Fig. 3, which has been described in Section III.C, generates a complementary pair of startup enable signals, *SU* and SU_B, depending on the V_{OUT} level to control the startup switches, N_2 and P_2, as well as the comparators. When V_{OUT} is too low to operate the comparators, the startup circuit sets *SU* = high and SU_B = low, which turn on N_2 and P_2, respectively, while disabling the comparators. In this condition, both N_1 and P_1 are diode-connected to form a passive voltage doubler, which starts charging V_{OUT} regardless of the comparators' status. When V_{OUT} exceeds a certain level that is sufficient to operate the comparators, *SU* and SU_B toggle and turn N_2 and P_2 off, while enabling the comparators to normally run the active voltage doubler.

C. PCE Analysis and Optimization

The PCE of the active voltage doubler can be expressed as

$$\mathrm{PCE}=\frac{P_{OUT}}{P_{IN}}=\frac{P_{Load}}{P_{Load}+P_{CMP}+P_{Tr,sw}+P_{Tr,Ron}} \quad (2)$$

where P_{Load} is the power delivered to the load and P_{CMP} is the internal power consumption of comparators excluding the power needed to drive the gates of P_1 and N_1. $P_{Tr.sw}$ and $P_{Tr.Ron}$ are the power losses in the pass transistors due to gate switching and dissipation in R_{on}, respectively. The sizing of P_1 and N_1 plays an important role in the PCE optimization since $P_{Tr.sw}$ and $P_{Tr.Ron}$ are affected by *W* and *L* of each pass transistor. Some of the terms in (2) can be approximated by

$$P_{Load}=\frac{V_{OUT}^2}{R_L} \quad (3)$$

$$P_{Tr,sw} \approx W_p C_{gp} V_{OUT}^2 f_c + W_n C_{gn} V_{OUT}^2 f_c \quad (4)$$

$$\begin{aligned} P_{Tr,Ron} &\approx I_p^2 R_{onp} D + I_n^2 R_{onn} D \\ &= \frac{1}{D}\left(I_{Load}+I_{CMP}+I_{Tr,sw}\right)^2 (R_{onp}+R_{onn}) \\ &= \frac{V_{OUT}^2}{D}\left(\frac{1}{R_L}+\frac{P_{CMP}+P_{Tr,sw}}{V_{OUT}^2}\right)^2 (R_{onp}+R_{onn}) \end{aligned} \quad (5)$$

where W_p and W_n are the widths of P_1 and N_1, and C_{gp} and C_{gn} are the gate capacitance per unit width of P_1 and N_1, respectively. F_c = 13.56 MHz is the carrier frequency, and *D* is the operating duty cycle (see Appendix). I_p and I_n are currents flowing through P_1 and N_1, respectively, and they are assumed to be equal. We also found P_{CMP} at each V_{OUT} from simulations (0.1 ~ 0.8 mW), and used it in the PCE analysis. L_p and L_n are 0.6 μm, the minimum length in this process.

Even though larger widths of pass transistors decrease $P_{Tr.ron}$, they increase switching losses, $P_{Tr.sw}$, due to larger parasitic gate capacitances. Hence, each pass transistor has an optimal size for minimum power dissipation depending on several parameters, such as V_{OUT}, R_L, and f_c. In the Appendix, we have derived detailed equations for the PCE and V_{Drop} while calculating optimal sizing of pass transistors for our target specifications.

III. Circuit Details and Design Considerations

A. Offset-Controlled High Speed Comparator

CMP_N and CMP_P need to drive large gate capacitances of N_1 and P_1 at high frequencies, respectively. Thus, key design parameters are drive capability and short delay. Comparator delay can reduce the PCE by either decreasing the input power that could otherwise be delivered to the load or allowing instantaneous back currents that flow from C_L back to L_2C_2 tank when $V_{IN} < V_{OUT}$. To reduce such delays, we have designed high-speed comparators with adjustable internal offsets, which basic concept was introduced in [44]. These built-in offset control functions help comparators turn their pass transistors on and off at proper times, leading to higher PCE.

Fig. 4 shows the schematic diagram of two symmetrical high-speed comparators, CMP_N in Fig. 4(a) and CMP_P in Fig. 4(b), each of which is equipped with three built-in offset-control functions. In Fig. 4(a), P_7-P_8, N_3-N_4, and P_{15}-N_7 form a common-gate comparator, which input terminals at the sources of N_3 and N_4 are connected to V_{SS} and V_{VD}, respectively. P_6 and R_1 form a biasing branch, which is mirrored on to P_7 and P_8. Thus, the comparator requires a minimum supply voltage of $V_{TH(P6)}$ in order to start its operation. Since the gate of the diode-connected N_3 is coupled with N_4, currents flowing through N_3 and N_4 depend on their source voltages, V_{SS} and V_{VD}, respectively. When $V_{VD} < V_{SS}$, the current flowing through N_4 tends to be larger than that of N_3, P_7, and P_8. Hence, V_1, the input of the P_{15}-N_7 inverter rapidly drops, leading to a high comparator output voltage, V_{CN}, which turns N_1 on.

Even though common-gate comparators are considered high speed due to their low input impedance and simple structure, their speed of operation in our 0.5-μm process was not fast enough to drive large capacitive loads (N_1 and P_1) at 13.56 MHz. Therefore, we added Offset-1_N and Offset-2_N-inside CMP_N (and their duals in CMP_P) in order to compensate for the turn-on and turn-off delays, respectively. Offset-1_N block is implemented using N_5 current source, controlled by N_6 switch, which can pull additional offset current from CMP_N output branch, leading V_1 to start dropping earlier when this offset mechanism is activated by V_{OS1N} = high. Constant Offset-2_N has been implemented using the size mismatch between P_8 and P_7. The larger W/L ratio of P_8 pushes additional offset current into the comparator output branch to increase $V1$ early.

The offset control signal, V_{OS1N}, is provided by an offset control block that consists of the current-starved inverter, P_{16}-P_{17}-N_8, and other logic gates in Fig. 4(a). When $V_{VD} > V_{SS}$, V_{CN} = low, and V_{OS1N} = high. Thus, N_6 turns N_5 on to pull offset current in parallel with N_4 at a level that is higher than the additional current that is pushed in P_8 by Offset-2_N. Therefore, V_{VD} starts to increase earlier to turn on N_1a bit before V_{VD} falls below V_{SS} to compensate for the comparator turn-on delay. Once V_{CN} = high, the Offset-1_N block turns off, and the offset current pushing through P_8 becomes dominant. As a result, V_{CN} starts to decrease earlier to turn N_1 off a bit before V_{VD} exceeds V_{SS} to compensate for the comparator turn-on delay. In this case, V_{OS1N} goes high after the delay generated by the current- starved inverter, which should be shorter than one carrier cycle period. Since switches to high when V_{VD} is much higher than V_{SS}, it does not cause any fluctuation or instability issues through its feedback loop.

Sudden variations in V_{VD} may occur with rapid changes in the forward current due to interconnect parasitic inductance between L_2C_2 tank and the voltage doubler. These variations may disrupt proper switching of the pass transistors and should be avoided. To protect the comparators against such effects, we have added a 3rd offset branch, Offset-3_N, which consists of P_9 current source, controlled by P_{13} switch. When V_{CN} goes low, it takes a while before the current-starved inverter output goes high. During this time, V_{OS3N} = low,

activating the Offset-3_N branch to inject additional current into V_1 node and prevent V_{CN} from undesired changes due to V_{VD} variations. This will keep N_1 off until the next carrier cycle.

Fig. 5 shows the timing relationship between the input, output, and comparator voltages of the voltage doubler and the offset control signals of each comparator. All transitions of the offset control signals occur fast with negligible rising and falling times even in the gray area in Fig. 5. When the current-starved inverter delay is changed, the transitions of $V_{OS1,3N}$ and $V_{OS1,3P}$ may start earlier or later, but their rising and falling times still remain very small. V_1 and V_2 in Fig. 4 also have small rising and falling times. Based on simulation results, V_1 starts to drop ~ 2.5 ns earlier before $V_{VD} < V_{SS}$ (due to Offset-1_N) and starts to increase ~ 4 ns earlier before $V_{VD} > V_{SS}$ (due to Offset-2_N), expediting V_{CN} transitions.

It should be noted that the current-starved inverter delay does not need to be accurate, and its changes due to process variations can be tolerated as long as the delay time is terminated before the next transition time. For example, V_{OS1N} goes low when $V_{VD} < V_{SS}$, and it should go back high again sometime after $V_{VD} > V_{SS}$ and before V_{VD} goes below V_{SS} again in the next cycle. Therefore, the low-to-high transition of V_{OS1N} can occur anytime during $V_{VD} > V_{SS}$. When designing comparators for this active voltage doubler, the current-starved inverter delay should be set first, and then Offset-1, -2, and -3 should to be tuned in this order by adjusting the sizes of their current source transistors because modifying each parameter can affect the timing and values of the following parameters.

In addition, we have added 4-bit off-chip digital control signals, two for each comparator, CTL0:1 (CMP_N) and CTL2:3 (CMP_P), which should be connected to either V_{OUT} (high) or V_{SS} (low), to adjust the switching times of the voltage doubler against process variations before the chip is used. For example, when CTL0 = low, the reduced current in P_8 drives node V_1 more weakly, delaying V_{CN} decrement and the onset of turning N_1 off. On the contrary, when CTL1 = low, P_{10} increases the size mismatch in the Offset-2_N, V_{CN} increases more rapidly, and N_1 turns off earlier. Moreover, startup control switches, P_{12} and N_{16}, are added in CMP_N and CMP_P, respectively, for a reliable startup operation as a passive voltage doubler. These switches turn on during the initial startup period and ensure that V_{CN} and V_{CP} are connected to V_{SS} and V_{OUT}, respectively.

B. PCE Optimization With Offset-Control Functions

To further clarify the effects of offset-control functions on the PCE, in Fig. 6(a) and (b) we have compared simulation results that show the voltage doubler input/output voltages (V_{VD} and V_{OUT}), comparator output voltages (V_{CN} and V_{CP}), and input power waveforms with the offsets disabled and enabled, respectively. In these simulations, we applied an AC voltage of $V_{IN,peak}$ = 2 V at f_c = 13.56 MHz to the input and connected R_LC_L = 1 kΩ ∥ 2 nF to the output of the active voltage doubler. Fig. 6(a) shows that without offset-control functions, because of the comparator turn-on delays, V_{CN} and V_{CP} turn on N_1 and P_1 too late, respectively. This results in power conduction delays through the pass transistors, from L_2C_2 tank to the load, when $V_{VD} < V_{SS}$ or $V_{VD} > V_{OUT}$. Moreover, comparator turn-off delays result in V_{CN} and V_{CP} turning off N_1 and P_1 too late, inducing back currents flowing from C_{IN} to V_{SS} and from the output load to the L_2C_2 tank, respectively. Both of these effects significantly decrease V_{OUT} (= 2.4 V) and PCE (= 28%).

Fig. 6(b) shows that the abovementioned conduction delays and back currents can be significantly reduced using offset-control functions utilized in Fig. 4 comparators. Offset-1 and offset-2 functions compensate for the turn-on and turn-off delays, respectively, such that V_{CN} and V_{CP} can turn on/off their pass transistors at the right time, leading to the highest possible PCE. Thanks to these offset-control functions, the active voltage doubler can

achieve much higher V_{OUT} (= 3.43 *V*) and PCE (= 80%) with the same $V_{IN,peak}$ and loading. Offset-3 function forces V_{CN} and V_{CP} to stay at V_{SS} and V_{OUT}, respectively, after their conduction periods in order to provide reliable pass transistor turn-off against spurious V_{VD} variations (not shown in these simulations).

C. Self-Startup Capability

The active voltage doubler is cable of starting up before its supply rail, V_{OUT}, is charged up to the level that is needed for the comparators to operate. The startup circuit in Fig. 7 reconfigures the doubler circuit as a diode-connected passive voltage doubler by generating SU and SU_B signals based on V_{OUT}. When V_{OUT} = 0 V, comparator outputs, V_{CN} and V_{CP} in Fig. 3, are also at 0 V. In this condition, P_1 and N_1 are diode-connected and conduct when $V_{VD} > V_{Th(P1)}$ and $V_{VD} < -V_{Th(N1)}$, respectively, and V_{OUT} starts to charge up. In Fig. 7, when $V_{OUT} < V_{Th(N22)} + V_{Th(P24)}$, P_{24} stays off and V_3 remains at 0 V through R_4. SU and SU_B follow V_{OUT} and V_{SS} and result in N_1 and P_1 to stay diode-connected. During the same period, P_{12} and N_{16} in Fig. 4(a) and (b) force V_{CN} and V_{CP} to be low and high, respectively, further supporting N_1 and P_1 to be diode- connected. When $V_{OUT} > V_{Th(N22)} + V_{Th(P24)}$, N_{22} turns on creating sufficient voltage across R_3 to turn on P_{24} and pull V_3 up. This, SU and SU_B become V_{SS} and V_{OUT}, respectively, turning N_2 and P_2 off, releasing the comparator outputs, and allowing N_1 and P_1 to operate as switches. Both R_3 and R_4 have 1 MΩ values to reduce static power consumption.

Fig. 8 shows the simulated waveforms for the self-startup process of the active voltage doubler, which guarantees that V_{OUT} is charged up to about 1.4 V before resuming its normal operation. Since sub-threshold operation of transistors also conducts a small amount of currents, the startup switching voltage may practically be less than the theoretical limit of $V_{Th(N22)} + V_{Th(P24)}$.

IV. Simulation and Measurement Results

A. Chip Micrograph and Measured Waveforms

The active voltage doubler was fabricated in the ON Semiconductor 0.5-μm 3M2P standard CMOS process for its relatively high voltage handling capability. Fig. 9 shows the chip micrograph of the active voltage doubler, which includes comparators (CMP_N and CMP_P), pass transistors (N_1 and P_1), control switches (N_2 and $P_{2–4}$), and the startup circuit (SU). The active voltage doubler occupies 0.144 mm^2 of silicon area with W_p/L_p = 2100 μm/0.6 μm and W_n/L_n = 1200 μm/0.6 μm. In our test setup, a class-C power amplifier drives the inductive link, which specifications are shown in Table II, to provide the active voltage doubler with 13.56 MHz sinusoidal input.

Fig. 10 shows the measured input and output waveforms of the active voltage doubler under two conditions when ($V_{IN,peak}$, V_{OUT}) = (1.46 V, 2.4 V) and (2 V, 3.2 V). Directly probing the comparator outputs induces extra loading, which results in undesired additional delays. Hence, we inferred the underlying events in the circuit by inspecting V_{IN} and $V_{VD} = V_{IN} + V_{Cin}$. In Fig. 3 once V_{VD} exceeds V_{OUT}, P_1 turns on, and a large current flows from the L_2C_2 tank to charge R_LC_L load. This forward current flow creates a voltage drop across the parasitic coil resistance and the interconnect inductance, resulting in a small dip in V_{VD}. While P_1 is on, $V_{VD} = V_{OUT} + I_pR_{op}$, which is fairly constant due to large C_L and L_2 that keep V_{OUT} and I_P constant, respectively. When P_1 turns off, the charging current instantaneously stops leading to a small bump in V_{VD} waveform following which V_{VD} returns to its normal sinusoidal shape. Therefore, P_1 and N_1 switching times can be estimated from V_{VD} variations, as shown in Fig. 10. We considered the peak voltages of V_{IN}

and V_{VD} when P_1 and N_1 just turned on or off in order to measure $V_{IN,pp}$ (= $2V_{IN,peak}$) and $V_{VD,peak}$, respectively. In these measurements, R_L = 1 kΩ, C_{IN} = 1 μF, and f_c = 13.56 MHz.

B. PCE and Dropout Voltage Measurements

To consider key factors that affect the active voltage doubler performance, we measured the PCE and V_{Drop} while sweeping 1) V_{OUT}, 2) R_L, and 3) f_c. Each panel in Figs. 11 – 13 shows the calculated, simulated, and measured (in two conditions) values of the PCE and V_{Drop} to verify the accuracy of our measurements and circuit models, while providing insight for improvements. Calculated PCE and V_{Drop} have been derived from (1) to (5) and the active voltage doubler model in the Appendix, where the switching times are assumed to be ideal.

Simulations are post-layout and include estimations of parasitic inductances. To measure the input current, we connected a small current-sense resistor, R_{sense} = 10 Ω, in series with the voltage doubler input and differentially measured the voltage across it. P_{IN} was then calculated offline by integrating the instantaneous product of the input current and voltage samples. V_{OUT} was also measured to calculate $P_{Load}=V_{OUT}^2/R_L$. We also considered V_{Drop} = $V_{IN,pp} - V_{OUT}$.

Fig. 11 shows the measured, simulated, and calculated PCE and V_{Drop} versus V_{OUT} for R_L = 0.5 kΩ and 1 kΩ, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz. In our measurements, the highest PCE was 79% achieved at V_{OUT} = 2.4 V, which was the onset of circuit operation with 1 kΩ loading. Unlike rectifiers in which the dropout voltage stays more or less constant with the PCE generally improving with higher V_{OUT} (see [44]), we observed increments in V_{Drop} and reductions in the PCE with increased V_{OUT}, which is evident in Fig. 11. These are some of the possible reasons behind this observation: First, increasing V_{OUT} with constant R_L requires higher input current, resulting in higher power loss ($P_{Tr,Rom}$) in the pass transistors. The power dissipation of comparators (P_{CMP}) and gate switching ($P_{Tr,sw}$) also increase as the comparator supply voltage, V_{OUT}, increases. Second, it turned out that the 2-bit offset control that we have included in each comparator was only sufficient to adjust the switching times around V_{OUT} = 2 ~ 2.8 V. Therefore, the voltage doubler operation was not optimized for V_{OUT} > 2.8 V, resulting in both measured and simulated PCEs in Fig. 11(a) to degrade at higher V_{OUT}. It can be observed in Fig. 10 that P_1 and N_1 turn off too early when V_{OUT} = 3.2 V, limiting the input power delivered to the load and decreasing the PCE. Third, increasing V_{OUT} resulted in higher peaks on V_{IN} and V_{VD}, which were also noticeable in Fig. 10, because of larger input current variations and more prominent effect of parasitic inductance. When $V_{VD} > V_{OUT} + V_{Th(P1)}$, P_1 is forced to conduct as a diode-connected transistor even after CMP_P tries to turn it off (due to suboptimal timing). This forced conduction in saturation region results in more power loss in P_1, and consequently lowers the PCE. Similarly, if $V_{VD} < V_{SS} - V_{PN-junction}$, it results in substrate leakage in N_1 because all NMOS body terminals should be connected to V_{SS} in this standard CMOS process. Therefore, some portion of the input current can flow through the parasitic PN junction instead of the N_1 switch, leading to additional power loss.

Calculated results in Fig. 11(a) and (b) show considerably higher PCE (86%) and lower V_{Drop} (0.27 V) compared to both simulated and measured results. Because in the theoretical circuit model we have assumed that the comparators turn the pass transistors on/off sharply with ideal timing regardless of variations in V_{OUT}, R_L, and f_c to achieve the maximum possible PCE, while the switching times in simulations and measurements are optimized for a certain operating condition, V_{OUT} = 2.4 V, R_L = 1 kΩ, and f_c = 13.56 MHz.

Fig. 12 shows the measured, simulated, and calculated PCE and V_{Drop} versus R_L. In Fig. 12(a), the maximum PCE was achieved with the designated R_L = 1 kΩ. As R_L increases

above 1 kΩ, I_{Load} drops and P_{Load} for the same V_{OUT} decreased. Therefore, the internal power dissipation ($P_{Tr.sw} + P_{CMP}$) in (2) becomes more dominant, reducing the PCE. On the other hand, when R_L decreased below 1 kΩ, higher input current is required to drive the heavy load, increasing $P_{Tr.Ron}$ and V_{Drop}, as shown in Fig. 12(b), and resulting in the PCE to decrease.

Fig. 13 shows the measured, simulated, and calculated PCE and V_{Drop} versus f_c with R_L = 1 kΩ. The comparator offsets of the proposed voltage doubler were designed for operation around f_c = 13.56 MHz. The PCE in Fig. 13(a) sharply decreased at higher f_c because the comparator delays became too long and allowed for back current to flow from C_L back to the L_2C_2 tank. At lower operating frequencies the PCE decreased again, though at a slower rate, due to the fixed comparator offsets and CS inverter delays leading the pass transistors to turn off earlier than they should, thus conducting smaller amount of power to the load. Fig. 13(b) shows the measured versus V_{Drop}, f_c which is also affected by the switching times. Even though V_{OUT} and R_L were fixed in all frequencies, lower PCE required higher input power to achieve the same V_{OUT}. Therefore, V_{Drop} increased at frequencies that had lower PCE.

We have measured three different chips, all of which showed similar characteristics as in Figs. 11 – 13, where the measured PCE is slightly lower than the simulated PCE due to process variations. Since the active voltage doubler has been optimized for a certain operating condition, i.e., V_{OUT} = 2.4 V, R_L = 1 kΩ, and f_c = 13.56 MHz, the PCE somewhat deviates from its optimal point when the operating condition changes. However, the voltage doubler still operates properly with PCE > 74% within the range of V_{OUT} (2 ~ 4 V) and R_L (0.5 ~ 1.5 kΩ), as long as f_c remains at 13.56 MHz. f_c is unlikely to change, because it is often controlled externally by a crystal-based oscillator that drives the power amplifier, shown in Fig. 1. The best way to oppose such PCE deviations from the optimal point is to form another closed loop around the voltage doubler at the system level to monitor V_{OUT} and change CTL0:3 at any operating condition via a well-defined search algorithm.

Fig. 14 shows post-layout simulated power consumption in the key components of the active voltage doubler in a pie-chart, when $V_{IN,peak}$ = 1.45 V, V_{OUT} = 2.4 V, R_L = 1 kΩ, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz. It can be seen that 80% of the input power has been delivered to the load, while the majority of the remaining 20% dissipates in the pass transistors (N_1 and P_1), followed by the comparators (CMP_N and CMP_P). Losses in N_1 (6.3%) and P_1 (6.4%) are due to their R_{on}, which are represented in our model by $P_{Tr.Ron}$. Power dissipation in CMP_N (2.6%) and CMP_P (4.6%) include the comparators' internal power consumption as well as the switching loss, which are represented in the model by P_{CMP} and $P_{Tr.sw}$, respectively. In addition, the offset-controlled functions in CMP_N and CMP_P consume only 29 μW and 45 μW, which are 0.4% and 0.6% of the total power consumption, respectively.

C. Performance Summary and Comparison

Table I benchmarks several recently reported rectifiers and voltage doublers used in various power management blocks along with the proposed active voltage doubler. In rectifiers, a major limitation is that V_{OUT} is always less than $V_{IN,peak}$, as expected. Passive voltage doublers cannot provide high PCE for the reasons discussed in Section I. Two active voltage doublers have been recently reported in the literature for energy scavenging from mechanical vibrations via piezoelectric transducers, which are designed to operate at low frequencies in the order of 100 Hz [45], [46]. Even though these active voltage doubles offer high PCE, they are not suitable for inductively powered biomedical applications, which operate at much higher frequencies through near-field inductive links. What we have presented in the last column is, to the best of our knowledge, the first active voltage doubler that can operate at 13.56 MHz in the ISM-band, providing 2.4 V of DC supply to a 1 kΩ

load from a peak AC input voltage of only 1.46 V, while offering the highest measured PCE of 79%. This is made possible with the accurate timing provided by offset-controlled high speed comparators for both rising and falling slopes of the carrier signal to maximize the power delivered to the load when turning the pass transistors on, while minimizing the back currents when turning them off. Table II summarizes the specifications of the active voltage doubler and the inductive link used in our measurements.

V. Conclusions

Comparator-based active rectifiers are considered the most promising solutions to achieve not only high PCE but also low dropout voltage in inductive power transmission. These AC-to-DC converters, however, need peak input voltage that should always be higher than the desired output voltage. This will limit the operation range and safe voltages of most inductively- powered devices, such as IMDs and RFID tags, which tend to have weakly coupled links. In order to overcome this limitation, we have developed a fully integrated power-efficient active voltage doubler with offset-controlled high speed comparators, which can offer high PCE and low dropout voltage comparable to active rectifiers, while increasing V_{OUT} well above the $V_{IN,peak}$. Three different offset control functions, built in the comparators, compensate for their turn-on and turn-off delays to maximize forward current to the load, while minimizing the back current. In addition, a novel startup circuit has been added to the voltage doubler to guarantee its reliable initial operation as a passive voltage doubler when V_{OUT} = 0 V. The relationship between the active voltage doubler PCE, dropout voltage, and several power loss factors has also been analyzed to provide designers with better insight towards maximizing the PCE.

Acknowledgments

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Appendix

In this section, we calculate the PCE in (2) and V_{Drop} in (1) using simplified voltage doubler waveforms shown in Fig. 15. In this analysis, D is the voltage doubler operating duty cycle, V_{Cin} is the voltage across C_{IN}, and $T = 1/f_c$ is the period of one operating cycle. In this simplified model, we assume: 1) $V_{IN}(t)$ is sinusoidal, 2) C_L and C_{IN} are large enough to maintain V_{OUT} and V_{Cin} almost constant during $T/2$, i.e., $\Delta V \approx 0$ V, 3) comparators turn on and off their pass transistors, P_1 and N_1, at ideal times and their outputs, V_{CP} and V_{CN}, have negligible rising and falling times, and 4) $V_{VD,peak} - V_{OUT} = V_{SS} - V_{VD,min}$, therefore, V_{Cin} can be expressed as $V_{OUT}/2$.

For this analysis, we also used the optimal size ratio ofP_1 and N_1 in [48] which leads to minimum $R_{onp} + R_{onn}$ in a given area

$$\left(\frac{W_p}{W_n}\right)_{opt} = \sqrt{\frac{\mu_n C_{ox}\left(V_{OUT} - V_{Thn}\right)}{\mu_p C_{ox}\left(V_{OUT} - |V_{Thp}|\right)}}. \quad (6)$$

While (3) and (4) can be solved directly by knowing circuit parameters, D needs to be derived to obtain $P_{Tr.Ron}$ in (5)

$$D=\frac{T_b-T_a}{T}=\frac{T_d-T_c}{T} \quad (7)$$

$$\begin{aligned} T_a&=\tfrac{T}{4}-\tfrac{DT}{2}, T_b=\tfrac{T}{4}+\tfrac{DT}{2},\\ T_c&=\tfrac{3T}{4}-\tfrac{DT}{2}, T_d=\tfrac{3T}{4}+\tfrac{DT}{2}. \end{aligned} \quad (8)$$

The charging current flowing through pass transistors, P_1 and N_1, needs to be the same as the total output and dissipated currents of the voltage doubler. Therefore

$$\begin{aligned} \int_{T_a}^{T_b} I_p dt &= \int_{T_c}^{T_d} I_n dt \\ &= \int_0^T \left(I_{Load}+I_{CMP}+I_{Tr,sw}\right) dt \end{aligned} \quad (9)$$

$$\begin{aligned} \int_{T_a}^{T_b} I_p dt &= \int_{T/4-DT/2}^{T/4+DT/2} \frac{V_{VD}(t)-V_{OUT}}{R_{onp}} dt \\ &= \left(\frac{V_{OUT}}{R_L}+\frac{P_{CMP}}{V_{OUT}}+\frac{P_{Tr,sw}}{V_{OUT}}\right) T. \end{aligned} \quad (10)$$

In (10), V_{VD} (t) can be written as

$$\begin{aligned} V_{VD}(t) &= V_{IN}(t)+V_{Cin}=V_{IN}(t)+\tfrac{V_{OUT}}{2} \\ &= V_{IN,peak}\sin\left(\tfrac{2\pi}{T}t\right)+\tfrac{V_{OUT}}{2} \\ &= \tfrac{\frac{V_{OUT}}{2}}{\sin\left(\frac{2\pi}{T}T_a\right)}\sin\left(\tfrac{2\pi}{T}t\right)+\tfrac{V_{OUT}}{2}. \end{aligned} \quad (11)$$

By substituting (11) in (10), D can be obtained with given values of R_{onp}, R_L, and V_{OUT} from

$$\begin{aligned} R_{onp} &= \left(\frac{1}{R_L}+\frac{P_{CMP}+P_{Tr,sw}}{V_{OUT}^2}\right) \\ &= \left(\frac{\cos\left(\left(\frac{1}{2}-D\right)\pi\right)-\cos\left(\left(\frac{1}{2}+D\right)\pi\right)}{4\pi\sin\left(\left(\frac{1}{2}-D\right)\pi\right)}-\frac{D}{2}\right) \end{aligned} \quad (12)$$

where P_{CMP} and $P_{Tr,sw}$ can be approximated from the simulation results and (4), respectively. Then, we can solve $P_{Tr.Ron}$ in (5) using D from (12), and the PCE can be calculated by substituting (3) – (5) in (2). In addition, using MATLAB we can easily try various R_{onp} values (e.g., by changing W_p) and find the optimal size of the pass transistors, which results in minimum power loss and maximize the PCE. V_{Drop} can also be estimated by obtaining $V_{IN,peak}$ from (11) and substituting it in (1).

Biographies

Hyung-Min Lee (S'06) received the B.S. degree (summa cum laude) in electrical engineering from Korea University, Seoul, Korea in 2006, and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2008.

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Dr. Ghovanloo is an Associate Editor of the IEEE Transactions on Biomedical Circuits and Systems and the IEEE Transactions on Biomedical Engineering. He has received awards in the 40th and 41st Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC) Student Design Contests. He has organized special sessions and was a member of Technical Review Committees for several major conferences, such as ISSCC and ISCAS, in the areas of biomedical circuits, sensors, and systems. He is a member of the Tau Beta Pi, the Sigma Xi, and the IEEE Solid-State Circuits Society, the IEEE Circuits and Systems Society, and the IEEE Engineering in Medicine and Biology Society.

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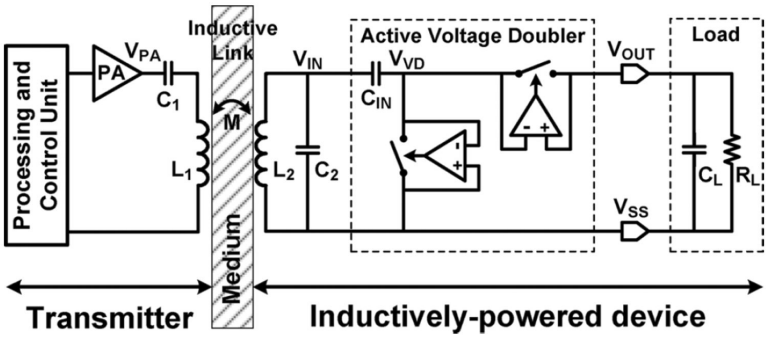


Fig. 1.
Block diagram of an inductively-powered device (e.g., an IMD) with emphasis on the inductive power transmission through the proposed active voltage doubler.

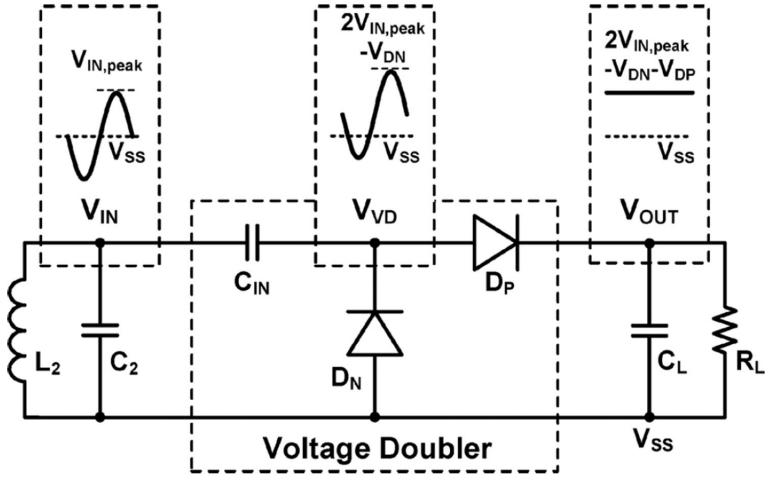


Fig. 2.
Schematic diagram of the passive voltage doubler using diodes or diode-connected transistors.

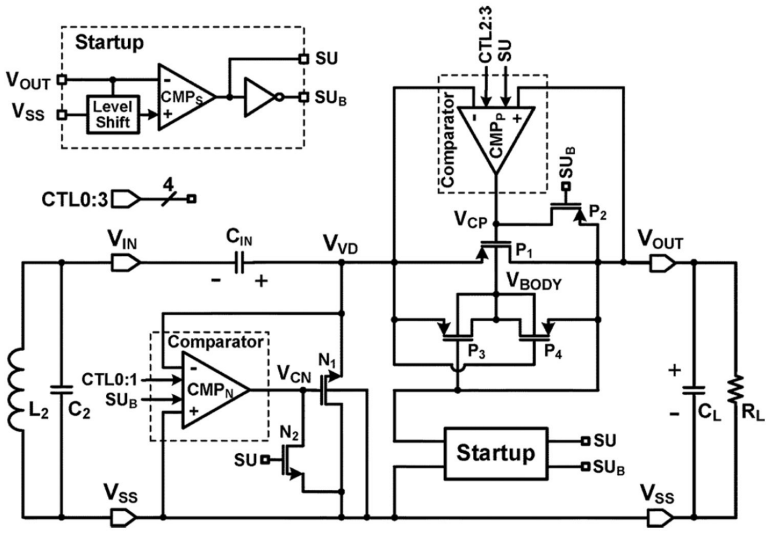


Fig. 3.

Schematic diagram of the proposed active voltage doubler employing high speed offset-controlled comparators, CMP_N and CMP_P, to drive N_1 and P_1 pass transistors, respectively, and achieve higher PCE.

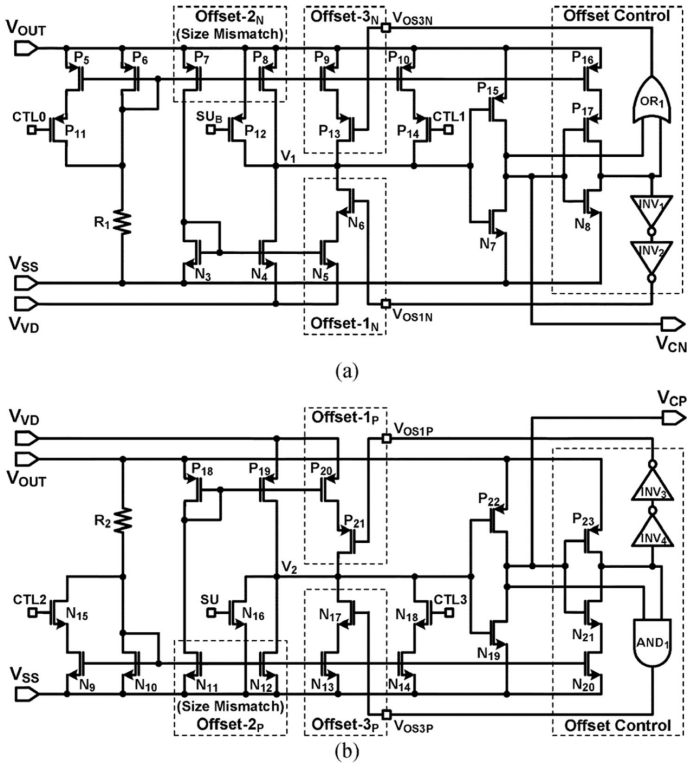


Fig. 4.

Schematic diagram showing three offset-control functions built-in our high speed comparators, (a) CMP_N and (b) CMP_P : Offset-1 for turn-on delay, Offset-2 for turn-off delay, and Offset-3 for reliable turn-off operation.

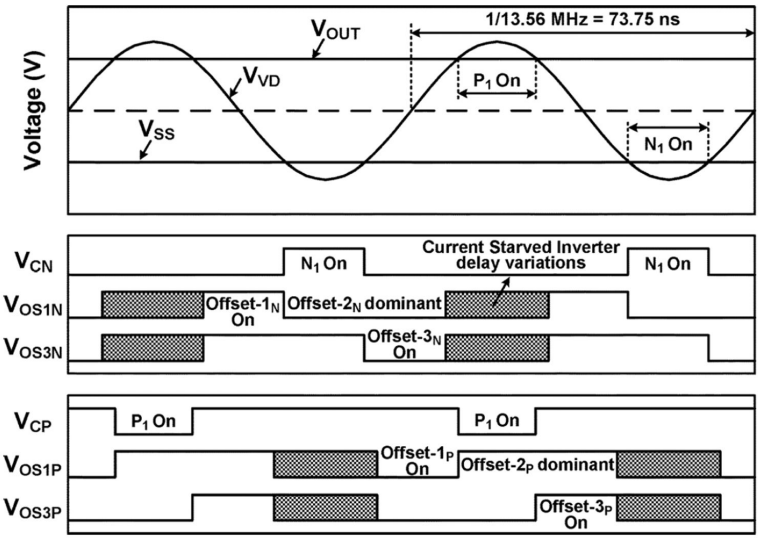
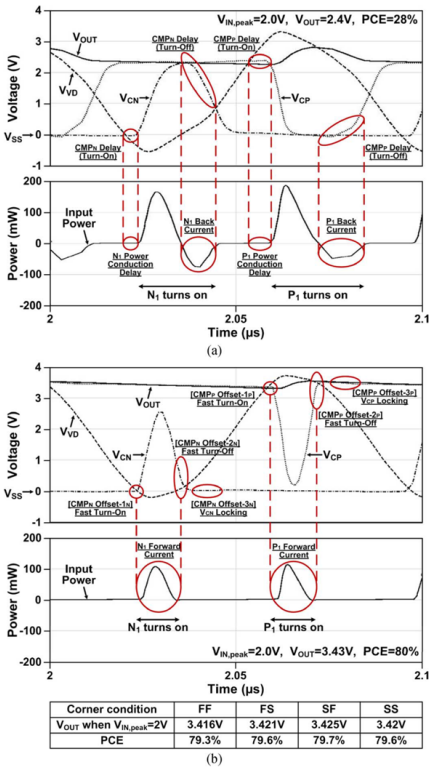


Fig. 5.

Timing diagram showing the relationship between the operating voltages of the active voltage doubler and the offset control signals of each comparator.



Corner condition	FF	FS	SF	SS
V_{OUT} when $V_{IN,peak}$=2V	3.416V	3.421V	3.425V	3.42V
PCE	79.3%	79.6%	79.7%	79.6%

Fig. 6.

Simulation results of the active voltage doubler showing waveforms of the input/output voltages and input power with $V_{IN,peak}$ = 2 V, R_LC_L = 1 kΩ || 2 nF, C_{IN} = 2 nF, and f_c = 13.56 MHz. (a) Without any offset-control functions. (b) With all three offset-control functions in the nominal and four process corner conditions.

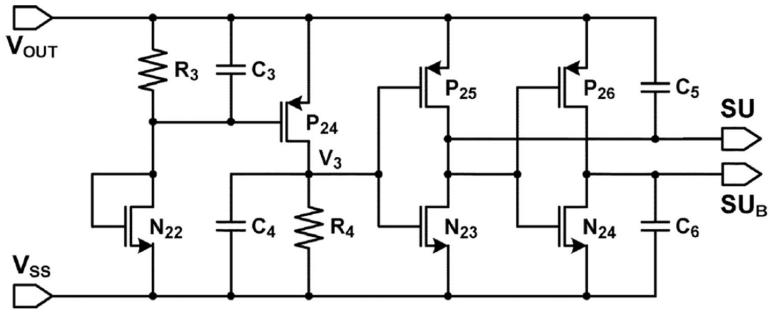


Fig. 7.
Schematic diagram of the startup circuit, which generates the startup enable signals, SU and SU_B.

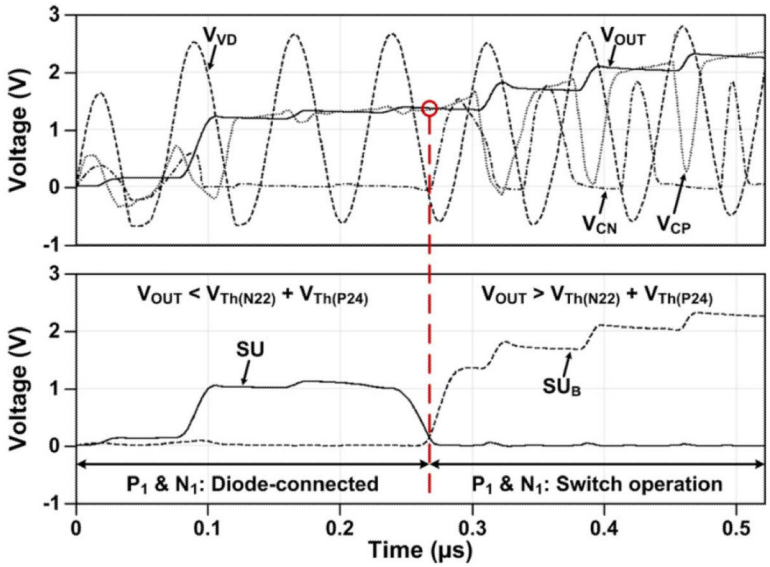


Fig. 8.

Simulation results showing self-startup capability of the active voltage doubler ($V_{IN,peak}$ = 1.5 V, V_{OUT} = 2.4 V, R_L = 1 kΩ, C_{IN} = C_L = 1 nF, and f_c = 13.56 MHz).

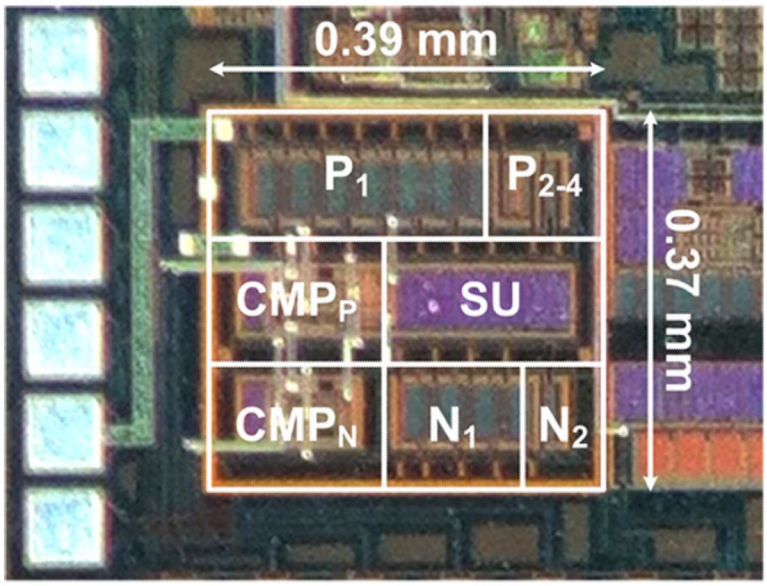


Fig. 9.
Fabricated chip micrograph and floor plan of the active voltage doubler in ON-Semi 0.5-μm Std. CMOS process, occupying an area of 0.144 mm^2.

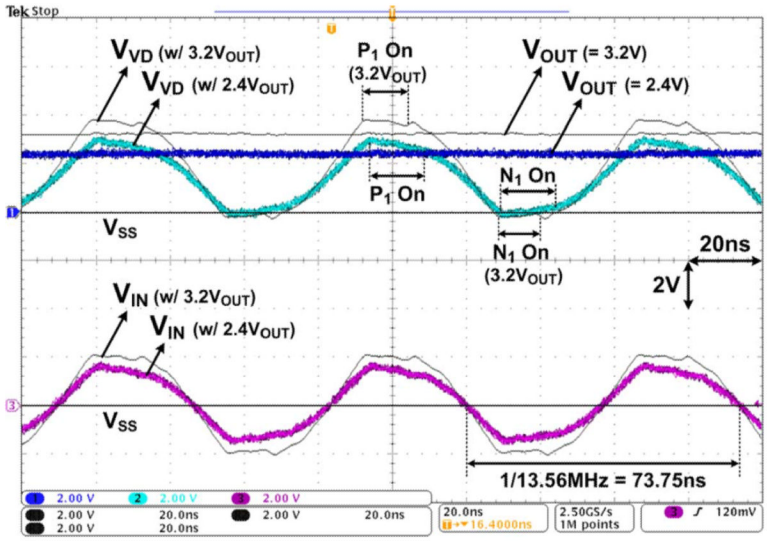


Fig. 10.

Measured waveforms of key nodes in the active voltage doubler, showing V_{IN}, V_{VD}, V_{OUT}, and V_{SS} for ($V_{IN,peak}V_{OUT}$ = (1.46 V, 2.4 V) and (2 V, 3.2 V) when R_L = 1 kΩ, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz.

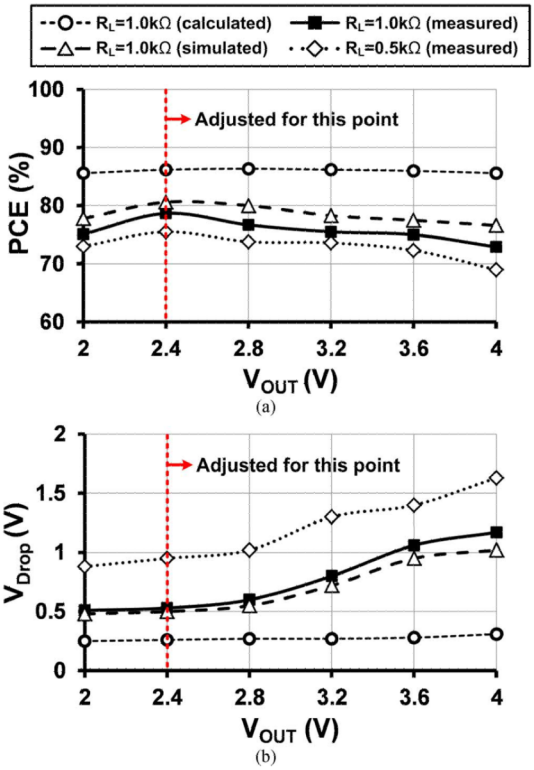


Fig. 11.

Measured (a) PCE and (b) V_{Drop} versus V_{OUT} with R_L = 0.5 and 1 kΩ, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz.

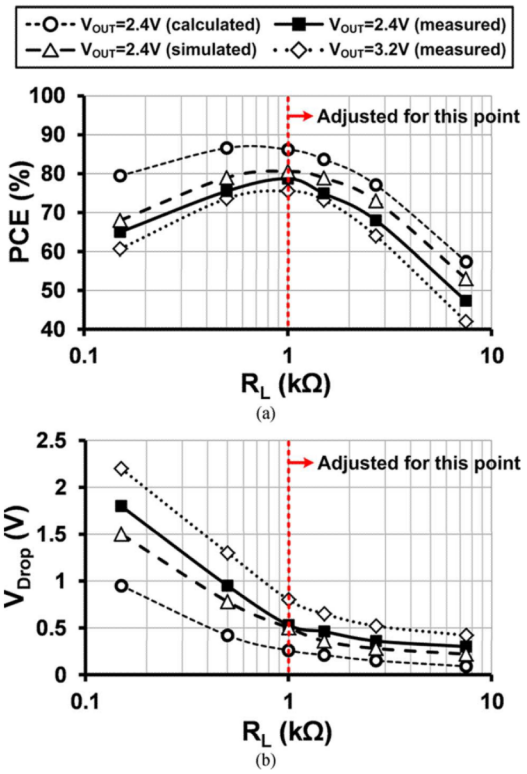


Fig. 12.

Measured (a) PCE and (b) V_{Drop} versus R_L with V_{OUT} = 2.4 and 3.2 V, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz.

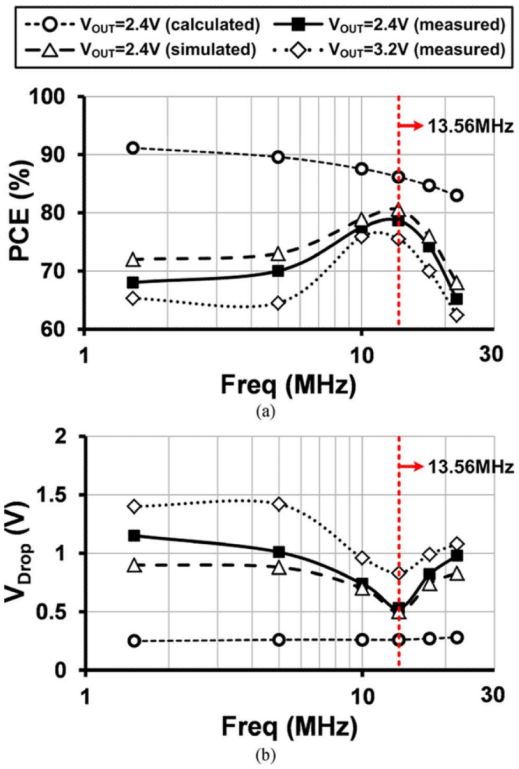


Fig. 13.

Measured (a) PCE and (b) V_{Drop} versus f_c with V_{OUT} = 2.4 and 3.2 V, R_L = 1 kΩ, and C_{IN} = C_L = 1 μF.

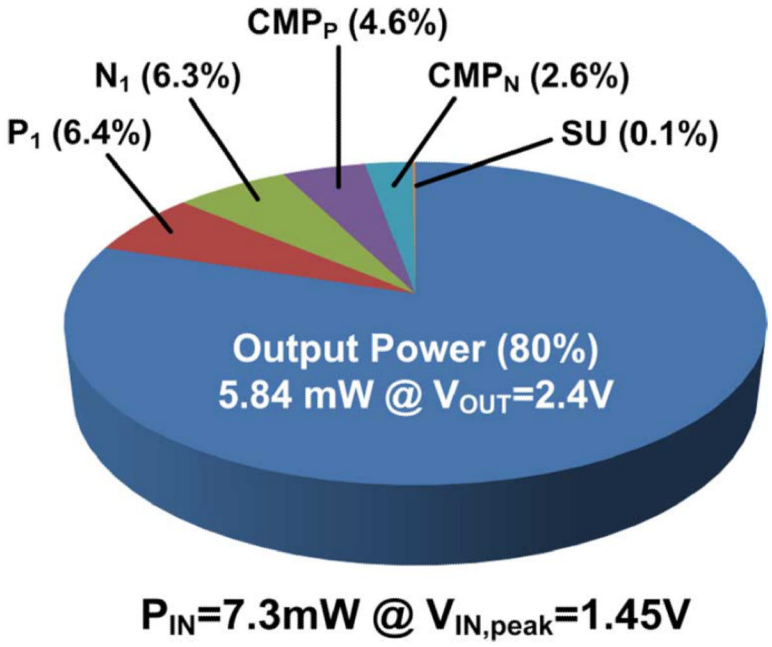


Fig. 14.
Simulated power consumption pie-chart when $V_{IN,peak}$ = 1.45 V, V_{OUT} = 2.4 V, R_L = 1 kΩ, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz.

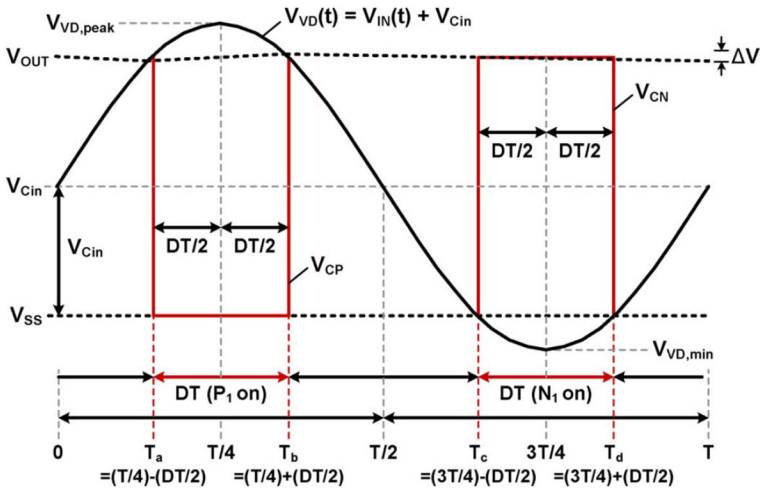


Fig. 15.
Simplified voltage waveforms of the active voltage doubler for the theoretical PCE analysis.

TABLE I

Rectifier and Voltage Doubler Benchmarking

Publication		**2007 [23]**	**2009 [32]**	**2009 [33]**	**2011 [44]**	**[47]**	**2009 [28]**	**2011 [29]**	**2008 [45]**	**2011 [46]**	**This work**
Technology		**0.5 μm CMOS**	**0.35 μm CMOS**	**0.18 μm CMOS**	**0.5 μm CMOS**	**Discrete (1N4148)**	**0.18 μm CMOS**	**0.8 μm HVCMOS**	**0.35 μm CMOS**	**Discrete (TLV3702)**	**0.5 μm CMOS**
Structure		**Passive rectifier (Schottky)**	**Active rectifier**	**Active rectifier**	**Active rectifier**	**Passive voltage doubler**	**V_{Th}-cancelled voltage multiplier**	**V_{Th}-cancelled voltage doubler**	**Active voltage doubler**	**Active voltage doubler**	**Active voltage doubler**
$V_{IN,\,peak}$ (V)		5	2.4	1.25	3.8	2.3	0.8	11.1	N/A	1.2	**1.46**
V_{OUT} (V)		4.2	2.08	0.96	3.12	2.4	1.8	20	3	2.24	**2.4**
VCE (%)*		84	86.7	76.8	82.1	52.2	56.3	90.1	N/A	93.3	**82.2**
R_L (kΩ)		2.8	0.1	2	0.5	1	270	20	400	0.1	**1**
C_{IN} / C_L (μF)		– / 0.0022**	– / 1	– / 200 pF	– / 10	1 / 1	N/A	– / 1	N/A	– / 100	**1 / 1**
f_c (MHz)		4	0.2~1.5	10	13.56	13.56	13.56	13.56	200 Hz	20 Hz	**13.56**
Area (mm^2)		N/A	0.4	0.86	0.18	N/A	0.83	N/A	N/A	N/A	**0.144**
PCE (%)	Sim.	N/A	87	N/A	87	N/A	N/A	90.5	95	N/A	**80**
	Meas.	75	N/A	76	80.2	51	54.9	N/A	> 90	83	**79**

* Voltage conversion efficiency (VCE) = V_{Out} / ($V_{IN,peak}$ × multiplication factor)

** On-chip capacitor. All other C_{IN} and C_L are off-chip components.

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TABLE II

Additional Active Voltage Doubler Specifications

$V_{Th}(N)$ / $V_{Th}(P)$	0.75 V / 0.9 V
Nominal output power	4 ~ 20 mW
Input capacitor (C_{IN}) / Load capacitor (C_L)	1 μF / 1 μF
Output ripple (R_L = 1 kΩ)	22 mV_{pp}
Comparator power consumption	0.1 ~ 0.8 mW*
Primary coil diameter / Inductance (L_1)	16.8 cm / 0.88 μH
Secondary coil diameter / Inductance (L_2)	3.0 cm / 0.41 μH
Pass transistor P_1 size (W_p/L_p)	2100 μm / 0.6 μm
Pass transistor N_1 size (W_n / L_n)	1200 μm / 0.6 μm
Total area on chip	0.144 mm^2

*From simulation