Tuning the threshold voltage of carbon nanotube transistors by n-type molecular doping for robust and flexible complementary circuits

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Tuning the threshold voltage of a transistor is crucial for realizing robust digital circuits. For silicon transistors, the threshold voltage can be accurately controlled by doping. However, it remains challenging to tune the threshold voltage of single-wall nanotube (SWNT) thin-film transistors. Here, we report a facile method to controllably n-dope SWNTs using 1*H*-benzoimidazole derivatives processed via either solution coating or vacuum deposition. The threshold voltages of our polythiophene-sorted SWNT thin-film transistors can be tuned accurately and continuously over a wide range. Photoelectron spectroscopy measurements confirmed that the SWNT Fermi level shifted to the conduction band edge with increasing doping concentration. Using this doping approach, we proceeded to fabricate SWNT complementary inverters by inkjet printing of the dopants. We observed an unprecedented noise margin of 28 V at V_{DD} = 80 V (70% of 1/2V_{DD}) and a gain of 85. Additionally, robust SWNT complementary metal–oxide–semiconductor inverter (noise margin 72% of 1/2V_{DD}) and logic gates with rail-to-rail output voltage swing and subnanowatt power consumption were fabricated onto a highly flexible substrate.

nanomaterials | n-doping | inkjet-printed | CMOS circuit

Flexible electronics have attracted increasing attention recently due to the plethora of possible and realized applications in radio-frequency identification cards (1, 2), flexible displays (3, 4), and digital processors (5). Solution-processed single-walled carbon nanotubes (SWNTs) are a promising candidate for flexible circuits due to their high charge carrier mobility (6), excellent flexibility/stretchability (7–9), and their compatibility with low-cost, large-area manufacturing processes, such as printing (1, 10) of SWNTs. Their applications in thin-film transistors (TFTs) and integrated logic circuits (11–14) have been demonstrated. However, to achieve robust digital circuits with high immunity against the influence of electronic noise in the system, it is important to be able to control the specific value of the threshold voltage of a transistor during the fabrication process (15, 16). This is because transistor threshold voltage determines the input voltage at which a circuit switches between two logic states (trip voltage of an inverter). When the trip voltage is half of the supply voltage, the circuit has the largest noise margin, which is a quantitative measure of the immunity of a logic circuit against noise and a figure of merit to characterize the robustness of the circuit (17, 18). If threshold voltage cannot be controlled during the fabrication process, the resulting circuit might not work reliably due to the electrical noise that is always present in the system.

Because SWNTs have ambipolar electrical transport properties (19), accurately tuning the threshold voltage permits the construction of complementary metal–oxide–semiconductor (CMOS) circuits that use both the p-type and n-type character of SWNTs. The advantages of CMOS circuits compared with unipolar logic circuits include lower power consumption, simpler circuit design, higher noise margin, better tolerance to the spread of threshold voltages of the transistors, and consequently higher circuit yields (15–17). Several approaches have been reported to adjust the threshold voltage of SWNTs and enable n-type SWNT transistors, including the use of (*i*): low-work function metal as source/drain contacts (20–22), (*ii*) atomic layer deposited (ALD) high-κ oxide on the SWNTs (23), and (*iii*) chemical doping on either the contacts or the bulk of SWNTs (14, 24–32). However, the continuous and reliable tuning of the threshold voltage of SWNT TFTs has not been achieved, thereby hindering optimal SWNT circuit performance. In addition, although several groups have fabricated flexible (11, 12, 13) SWNT unipolar circuits, the fabrication of SWNT CMOS electronics on a flexible substrate has yet to be reported.

We recently described the use of dimethyl-dihydro-benzoimidazoles (DMBI) as a highly efficient class of molecular dopants for [6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM), C_{60}, and graphene (33–35). Because these dopants can be deposited via solution processing, their use can be envisioned in large-area printable electronics. We have also developed a simple and scalable SWNT sorting method using regioregular poly(3-dodecylthiophene) (rr-P3DDT) to achieve highly selective dispersion of semiconducting SWNTs (36, 37). As a result, the

Significance

Highly noise-resistant logic gates are needed for large-scale circuits. This was challenging previously with carbon nanotube circuits due to the lack of control of the threshold voltages of nanotube transistors. We demonstrate the use of dopants to tune the charge carrier density of carbon nanotubes films and hence precisely control the threshold voltages of carbon nanotube transistors. This doping method is highly versatile and can be applied through inkjet printing. With this technique, we demonstrate highly noise-resistant and low power consumption carbon nanotube logic gates on a flexible substrate. This work places carbon nanotubes in a highly competitive position for large-scale solution-processed flexible circuits.

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polymer-sorted SWNT network TFTs exhibited a very high yield and good uniformity across large areas (38).

In this work, we demonstrate the effective n-type doping of our rr-P3DDT sorted SWNT films using DMBI dopants, via both vacuum and solution deposition methods. By controlling the dopant concentration or thickness, we can accurately tune the charge carrier density of SWNT films and consequently the device threshold voltages over a wide range. As a result, both the n-type and p-type SWNT transistors with symmetric threshold voltages and current outputs can be fabricated. We have also used photoelectron spectroscopy (PES) to observe the Fermi level shifts of the SWNTs after n-doping. The controlled n-type doping of SWNTs enabled us to fabricate inverters with inkjet-printed dopants that had unprecedented noise margins as high as 28 V at V_{DD} = 80V (70% of 1/2V_{DD}) and gains up to 85. Furthermore, the versatility of our n-type doping method allowed us to fabricate flexible SWNT CMOS inverters, negated AND (NAND) and negated OR (NOR) logic gates. The flexible CMOS inverter also demonstrated robust operation with an even higher noise margin of 1.8 V at V_{DD} = 5 V (72% of 1/2V_{DD}) and a gain of 18. The flexible CMOS NAND and NOR logic gates demonstrated a record rail-to-rail output voltage swings and sub-nanowatt static power consumption.

Results

***n*-Type Doping by Vacuum Evaporation.** We used *o*-MeO-DMBI, *N*-DMBI, and *o*-MeO-DMBI-I as molecular dopants, which were synthesized according to literature procedures (see *Methods* and *SI Appendix*, Fig. S1) (33–35, 39). *o*-MeO-DMBI and *N*-DMBI are solution processable, whereas *o*-MeO-DMBI-I, the iodide salt of *o*-MeO-DMBI, can be vacuum evaporated. These dopants are all air-stable solids that can be stored and handled in ambient conditions for extended periods of time without degradation. The doping mechanism has been described by a hydride or hydrogen atom transfer from the DMBI to the acceptor, as previously investigated for PCBM (39).

To characterize the n-type doping of SWNTs, *o*-MeO-DMBI-I (device and dopant structures are shown in Fig. 1*A*) was evaporated under a high vacuum with different nominal thicknesses determined by a quartz crystal monitor during deposition onto SWNT TFTs (see *Methods* for details). The electrical characteristics of the SWNT TFTs were measured using a probe station in a N_2-filled glovebox. The transfer curves of devices measured before and after doping are shown in Fig. 1*B*, and the threshold voltage statistics with the corresponding doped SWNT carrier densities are summarized in Fig. 1*C*. The error bars represent the standard deviations (SDs) of the five devices measured at each doping concentration.

We observed that the threshold voltage of the transistors was negatively shifted in a continuous manner over a wide range upon deposition of different thicknesses of *o*-MeO-DMBI-I. This shift in threshold voltage is attributed to n-doping and a smaller Schottky barrier thickness for electron injection as a result of the shift of the Fermi level toward the conduction band edge after n-doping (see *PES Measurements*) (27). With a 0.2-nm nominal dopant thickness, we can already observe a clear shift in the threshold voltage toward more negative voltages for the p-type sweep (defined from 40 V to −60 V) from 20.57 ± 1.78 V to −14.57 ± 4.17 V. This demonstrates that the transistors can be operated in both enhancement and depletion modes (40). For the n-type sweeps (defined from −40 V to 60 V), with increasing doping concentrations, we also observed changes in threshold voltage over a wide range from −4.04 ± 1.24 V to −35.17 ± 0.44 V (Fig. 1*C*). The very small error bars for the threshold voltage at each doping concentration demonstrate the highly accurate control of threshold voltage achieved by our chemical doping method. An estimate of the electron density (n) (Fig. 1*C*) of the SWNT films as a function of doping thickness can be obtained from the saturation regime equation (40, 41):

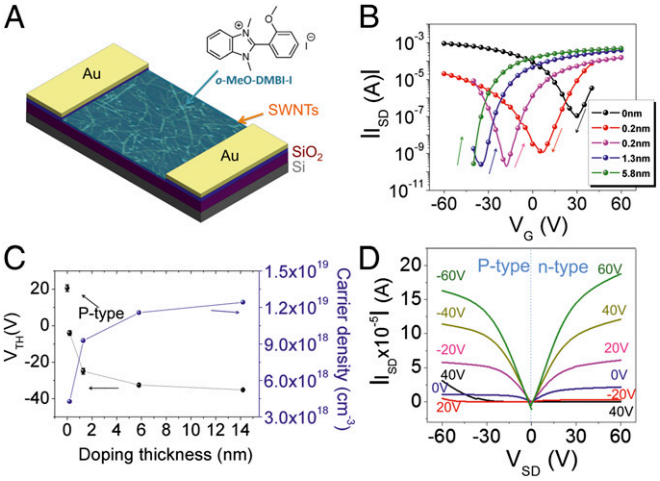

Fig. 1. *N*-doping by vacuum evaporation. (*A*) Schematic of vacuum-evaporated *o*-MeO-DMBI-I doped SWNT TFTs (L = 20 μm, W = 400 μm). (*B*) Transfer characteristics of SWNT TFTs doped by *o*-MeO-DMBI-I at different nominal thicknesses determined by a quartz crystal monitor during deposition (V_{SD} = 80 V for n-type and V_{SD} = −80 V for p-type). (*C*) Average threshold voltage and calculated carrier density as a function of *o*-MeO-DMBI-I thickness. Five devices were characterized for each doping thickness, with error bars showing the standard deviation (SD) from the average value. (*D*) Output characteristics of undoped and n-doped SWNT TFTs at an *o*-MeO-DMBI-I thickness of 5.8 nm.

$$I_{SD} = \left(\frac{C_i \mu W}{2L}\right)(V_G - V_{th})^2 \quad \text{and} \quad \sigma = q\mu n = \frac{I_{SD} L}{V_{SD} W d},$$

where I_{SD} and V_{SD} are the source/drain current and voltage, respectively, V_G is the gate voltage, V_{th} is the threshold voltage, μ is the saturation mobility, W and L are the channel width (400 μm) and length (20 μm), and d is the layer thickness of the SWNTs. The thickness of the SWNT film is estimated to be ∼1.5 nm from the atomic force microscope (AFM) image. We observed a sharp increase in the carrier density at a low doping concentration, increasing more slowly with further increases in doping concentration. The slower gain in carrier density is likely caused by the aggregation of dopants with increasing layer thickness, which limits the contact between the dopant and underlying SWNTs (*SI Appendix*, Fig. S2).

The device mobility also varies with doping concentration. As the dopant thickness was increased, the electron mobility first increased, and the ambipolarity of the devices became more pronounced (*SI Appendix*, Fig. S3). An average electron mobility of 1.94 ± 0.22 $cm^2/V{\cdot}s$ was achieved at a nominal dopant thickness of 5.8 nm, a value almost identical to the hole mobility of the intrinsic SWNTs, which was found to be 1.93 ± 0.17 $cm^2/V{\cdot}s$. Symmetric output curves for the p-type and n-type devices were obtained at this doping thickness (Fig. 1*D*). At an even higher doping thickness, the electron mobility is reduced. We attribute this reduction to both charge carrier scattering at high doping concentrations (42, 43) and the tendency of *o*-MeO-DMBI to aggregate (33, 34) as shown in the AFM images of *SI Appendix*, Fig. S2, which may perturb the morphology of the underlying layers and tube−tube contacts, although the exact origin has not been studied in detail. This mobility value was estimated using a parallel plate model. A rigorous analytical cylindrical model (44) based on the density of SWNTs for our transistors also gave similar mobility values and trends. Furthermore, the on/off ratio of the doped devices remains above 10^5 for all thicknesses, as a consequence of the excellent sorting achieved by the polymer wrapping (36). The disappearance of hole current in the highly doped n-type devices may be due to surface dipole formation at the

metal–SWNT contact that suppresses hole injection (28). We note that the n-doped devices are not air-stable. However, devices exposed to air can recover completely when they are returned to nitrogen atmosphere, as shown in *SI Appendix*, Fig. S4. We also observed hysteresis in our n-doped device (*SI Appendix*, Fig. S5), but the magnitude of the hysteresis is not larger than the hysteresis in our p-type devices (*SI Appendix*, Fig. S6); encapsulation with inorganic or organic layers is expected to improve air stability and reduce the hysteresis of the SWNT TFTs (45, 46).

n-Type Doping by Solution Processing. For solution processing, *o*-MeO-DMBI and *N*-DMBI were used (chemical structures shown in Fig. 2*A*) as the n-type dopants. They are both highly soluble in common solvents suitable for spin coating and inkjet printing. Different dopant concentrations in ethanol were deposited on the SWNT TFTs via spin coating (see *Methods*). The transfer curves after doping by *o*-MeO-DMBI and *N*-DMBI are shown in Fig. 2*B* and Fig. 2*C*, respectively, and the statistics of the threshold voltage shift and the calculated carrier density with respect to the doping concentration for both dopants are shown in Fig. 2*D* and *SI Appendix*, Fig. S7, respectively. The range of the n-type threshold voltage shift for the *o*-MeO-DMBI doped devices is from 6.61 ± 2.73 V at 1 mg/mL to as low as −31.22 ± 0.87 V at 25 mg/mL The changes in performance and morphology (*SI Appendix*, Figs. S8–S10) at different concentrations are similar to those observed with vacuum-evaporated *o*-MeO-DMBI-I at different thicknesses. The best performing *o*-MeO-DMBI doped devices were obtained at 10 mg/mL with an average electron mobility of 1.58 ± 0.37 $cm^2/V{\cdot}s$ and a high average on/off ratio of (1.08 ± 0.91) × 10^5.

In contrast, *N*-DMBI showed a much stronger n-doping effect. At a concentration of 1 mg/mL, for instance, the threshold voltage already shifted to −20.21 ± 1.69 V. The mobility increased to as high as 27.50 ± 5.20 $cm^2/V{\cdot}s$ at a solution concentration of 25 mg/mL (*SI Appendix*, Fig. S8). However, the on/off ratio was greatly reduced due to a significant increase in the off current, which was also observed for our previously reported

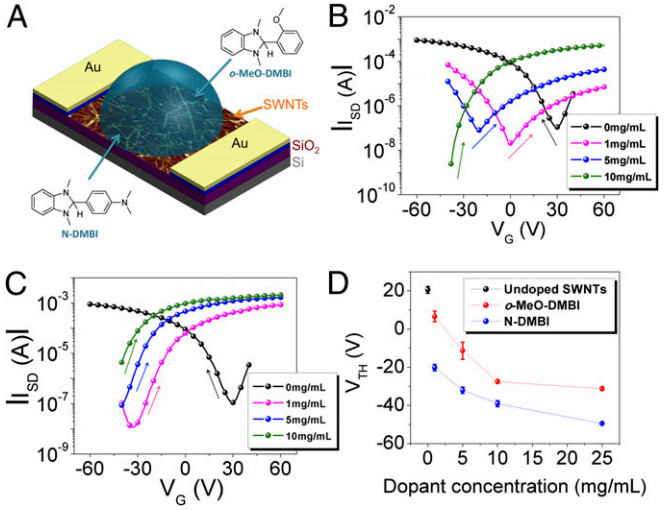

Fig. 2. *N*-doping by solution deposited dopants. (*A*) Schematic of *o*-MeO-DMBI or N-DMBI doped SWNT TFTs prepared by solution doping (L = 20 μm, W = 400 μm). Transfer characteristics of SWNT TFTs doped by (*B*) *o*-MeO-DMBI and (*C*) *N*-DMBI, at different concentrations at V_{SD} = 80V for n-type and V_{SD} = −80V for p-type. (*D*) Average threshold voltage change as a function of various *o*-MeO-DMBI and *N*-DMBI concentrations. Five devices were measured for each doping concentration, with error bars showing the SD from the average value.

n-doped $PC_{61}BM$ transistors (33, 34). Hence, while *N*-DMBI is an effective n-type dopant, it is difficult to independently control both threshold voltage and on/off ratio due to the high doping efficiency observed for *N*-DMBI dopants, thereby limiting its utility in digital circuits. However, *N*-DMBI could be very useful for analog or radio frequency applications, which require a high mobility but tolerate a much lower on/off ratio than digital circuits.

Fermi Level Shift upon n-Doping. The relationship between the shift of the threshold voltage and the electron carrier density of n-doped SWNTs was explored with PES. Specifically, the Fermi level shift was determined at different doping concentrations. From the PES spectra shown in Fig. 3*A*, we observed an increase in work function from the undoped to doped SWNT films. After doping with 1 mg/mL *o*-MeO-DMBI solution, the work function of SWNTs decreased from 4.98 eV for the undoped sample to 4.30 eV, indicating an effective interfacial electron transfer from *o*-MeO-DMBI to SWNTs. The doped SWNTs with 3-nm *o*-MeO-DMBI-I films showed a similar decrease of work function to 4.22 eV. At a higher doping concentration obtained with 25 mg/mL *o*-MeO-DMBI solution, the work function of the doped SWNTs was lower than 4.00 eV, demonstrating the strong increase in electron density with these n-type dopants. Although it has been reported that the shift of threshold voltage during potassium doping of individual SWNTs might be due to the modification of the metal contacts by lowering the Schottky barrier height for electron injection (28), the reduction in work function shown in our PES measurements indicates that it is indeed the doping of the SWNT films that caused the shift of the threshold voltage. The reduction in barrier thickness for electron injection with increase in n-doping is shown schematically in Fig. 3*B*.

Complementary Inverters with Inkjet Printed n-Dopant. The controlled tuning of the threshold voltage of SWNT TFTs by *o*-MeO-DMBI doping enabled the fabrication of robust complementary inverters with high noise margin. The fabrication processes of the inverters on the 300-nm silicon oxide dielectric is described in *Methods*, and the optimized concentration for the n-type inkjet-printed *o*-MeO-DMBI-doped SWNT TFTs was found to be 5 mg/mL. The trip voltage, defined as the input voltage V_{IN} when $V_{OUT} = V_{IN}$, in this case is 34 V (Fig. 4*A*), which is very close to $V_{DD}/2$ (the inverter structure and circuit diagram shown in Fig. 4*B*). The noise margin of the inverter is defined from the maximum equal criterion principle (47, 48), and was calculated by: (*i*) mirroring the input and output voltages in the voltage transfer curve (VTC) and (*ii*) determining the maximum size of the square that fits between both curves (shown in Fig. 4*A*). The inverter demonstrated a very high noise margin of 28 V at a supply voltage of 80 V (70% of $1/2V_{DD}$) and a gain of 85 (Fig. 4*C*), values that were not achieved for previously reported SWNT CMOS inverters (14, 30, 32). Our obtained noise margin value indicates that even if the noise causes the input voltage shift of 28 V at each direction, the inverter can still produce the correct output signal. The highest reported noise margin for a CMOS inverter based on an individual flexible semiconductor material is 65% of $1/2V_{DD}$ for an ambipolar polymer (49).

Flexible Complementary Circuit. Transistors and complementary inverters were also fabricated on flexible polyimide substrates using our doped and undoped SWNTs (see *Methods* and Fig. 5*A* for structure of the device). *o*-MeO-DMBI-I was vacuum deposited to n-dope the SWNTs. The undoped and n-doped transistor transfer curves are shown in *SI Appendix*, Fig. S11*A*. As with using the rigid substrate, excellent control over the threshold voltage was possible on flexible substrates (*SI Appendix*, Fig. S11 *A* and *B*). The flexible p-type sweep SWNT TFTs have a threshold voltage of 8.46 ± 0.48 V. Upon doping, the threshold voltage

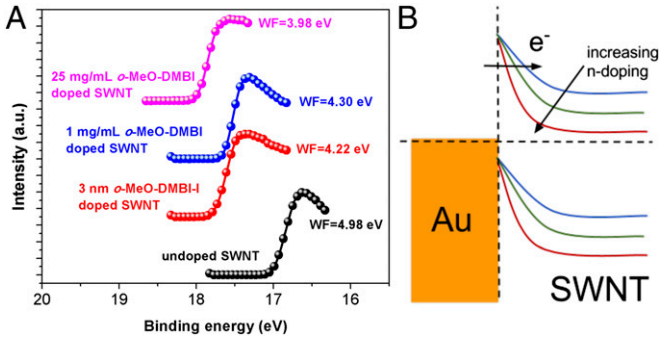

Fig. 3. (*A*) PES spectra of the secondary cutoff region of the undoped and doped SWNT films and their calculated work functions. (*B*) Schematic energy band diagram showing the electron injection barrier with increasing n-doping.

n-type sweep SWNT TFTs reduced continuously from -3.51 ± 0.66 V to -8.54 ± 0.48 V. The small SDs of threshold voltages at each doping concentration again demonstrate the accurate control of threshold voltage on the flexible substrate. The trend of the device performance and the morphology of the SWNTs were similar to those observed for the rigid devices (*SI Appendix*, Figs. S11 *C* and *D* and S12). Moreover, the on/off ratio also remained $>10^5$ at all doping concentrations studied.

To test the flexibility of the n-doped transistors, they were subjected to bending at different radii of curvature (Fig. 5*B*). The devices were held in the bent conformations for ~10 s at each radius of curvature in orientations both parallel and perpendicular to the channel length. We observed that there was no change in the transfer characteristics of the devices before, during, or after bending at various radii of curvature down to 2.5 mm, demonstrating the high flexibility of these devices. Our n-doping approach also enabled us to fabricate reliable and flexible complementary inverter, NAND, and NOR logic gates (Fig. 5 *C* and *D*). A standard V_{DD} value of 5 V was used to load the flexible inverter, NAND, and NOR gates. The inverter (Fig. 5 *E* and *F*) has a trip voltage of 2.6 V, which is extremely close to $1/2V_{DD}$ = 2.5 V, made possible by excellent control of the threshold voltage. As a result, the flexible inverter has a noise margin of 1.8 V at V_{DD} = 5 V (72% of $1/2V_{DD}$), which is among the highest ever reported noise margin for flexible CMOS inverters achieved by all materials. It also has a high gain of 18. The NAND gate consists of two n-type transistors in series and two p-type transistors in parallel, whereas the NOR gate consists of two p-type transistors in series and two n-type transistors in parallel (circuit diagrams and truth tables shown Fig. 5 *G* and *H*). The input voltage (A, B) of 5 V or 0 V are logic "1" and "0", respectively. The output voltage (V_{OUT}) is plotted for the NAND and NOR gates in Fig. 5 *G* and *H*. A full voltage swing of 5 V has been reached for these logic gates, with the output "1" at 5 V and the output "0" at 0 V, which has not been previously achieved (14, 50–53). The static state current (I_{DD}) in our logic gates is also very low, as plotted as in Fig. 5 *G* and *H*. In combination with a V_{DD} = 5 V, the static power consumption is estimated to be subnanowatt for most of the states. This is one of the lowest values that have been achieved for digital circuits made from any flexible materials. We attribute both the rail-to-rail voltage swing and low static power consumption to the low off-current in our SWNT TFTs.

Discussion

It was previously stated that threshold voltage control is the main obstacle preventing high-performance carbon nanotube integrated circuits from being realized (54). Here, we demonstrated the continuous and reliable threshold voltage tuning of carbon nanotube transistors using molecular n-doping over a wide range. This is unprecedented for SWNT TFTs. Previous works mainly allowed shifting of threshold voltages toward a discrete value (14); they did not offer the degree of tuning or the reliable control achieved using our methods. Our continuous, large-range, accurate tuning of both the p-type and n-type transistors enabled robust CMOS circuits.

The shifting of threshold voltages has been demonstrated in other flexible materials (e.g., organic transistors) using self-assembled monolayers (55) or gate electrode metals (56). However, there were relatively large SDs of threshold voltages. Additionally, because fully continuous tuning of threshold voltages over a wide range could not be realized, the inverters had low noise margins (56). In comparison, our SWNT TFTs have excellent uniformity (very small SD in threshold voltages) at different doping concentrations on both rigid and flexible substrates; therefore, they become promising flexible materials for large-scale CMOS circuits.

Precise control of threshold voltage enabled us to fabricate robust CMOS circuits based on SWNTs in this work. A CMOS inverter with an optimum trip voltage and noise margin (72%) was fabricated on a flexible substrate, the highest noise margin for a CMOS circuit based on a single flexible semiconductor material achieved to date. The highest previously reported noise margin organic CMOS inverter was 80% on a rigid substrate, using both p-type (pentacene) and n-type (F_{16}CuPc) semiconductors (18). However, the channel width of one of the transistors had to be 10 times larger than the other, which increases the size of the whole circuit. Our threshold voltage tuning method is advantageous because the continuous tunability of the threshold voltage allows the best matching of electron and hole currents for p-type and n-type devices with the same channel dimensions, as well as under different required environments (e.g., flexible substrates, dielectrics, contact metals, gate metal). The threshold voltage tuning will also allow a better-customized circuit to be designed for specific requirements of supply voltage, speed, noise margin, or power consumption.

In summary, we have demonstrated effective and controllable n-doping of polymer sorted SWNT films using DMBI derivatives. By varying the amount of deposited n-dopants, we were able to effectively tune the carrier density of SWNT films, which in turn shifted the threshold voltages of the SWNT TFTs over a wide range. Our PES measurement results confirmed that the n-type doping shifted the Fermi level of the SWNTs closer to the conduction band edge. Inkjet printing was subsequently used to n-dope SWNT films to fabricate complementary inverters, which were observed to exhibit an unprecedented noise margin at 70% of $1/2V_{DD}$ and a gain of 85. In addition, n-type doping was demonstrated for devices fabricated on a flexible polyimide substrate.

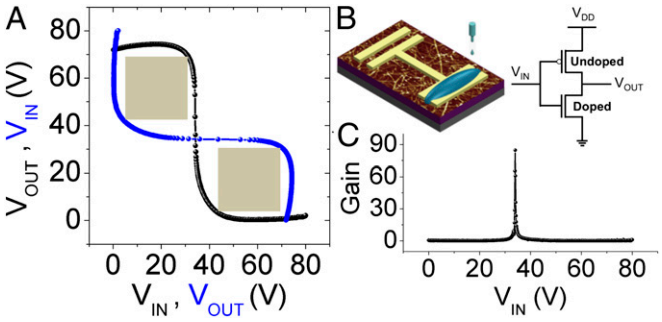

Fig. 4. (*A*) VTC and noise margin extraction of *o*-MeO-DMBI doped SWNT complementary inverters at V_{DD} = 80 V as prepared by inkjet printing. (*B*) The structure and circuit diagram of the inverter. (*C*) The gain of the inverter at the same V_{IN} range.

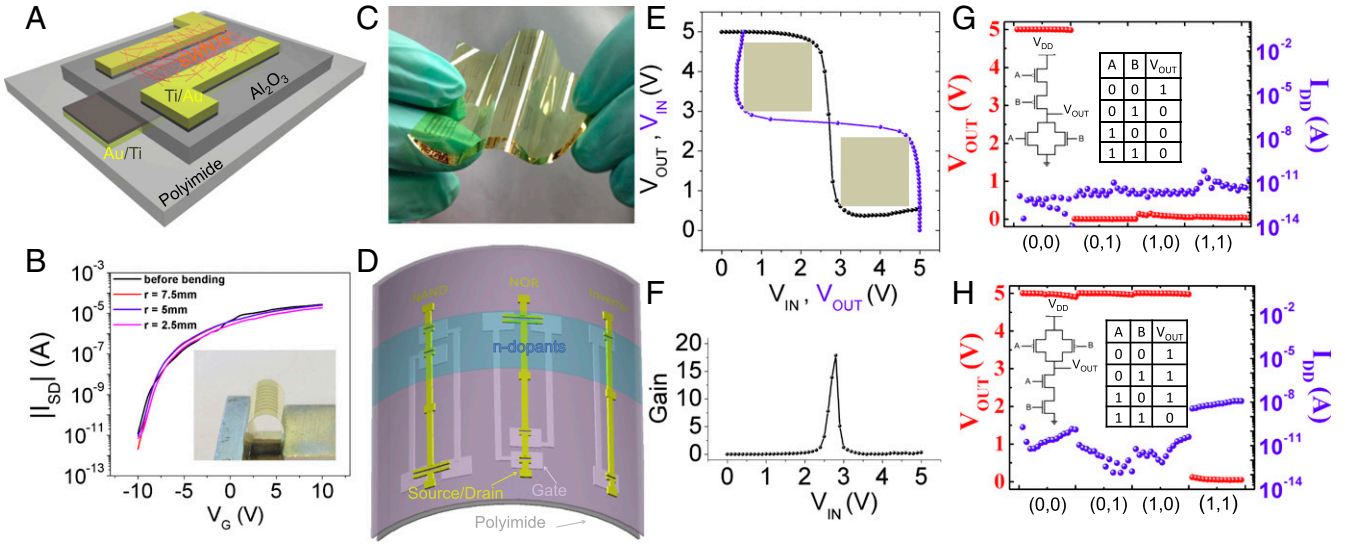

Fig. 5. Flexible SWNT device and circuit. (*A*) Schematic showing the structure of the flexible devices (L = 20 μm, W = 400 μm). (*B*) Transport characteristics of an n-doped device before bending and after bending at different radii of curvatures. *Inset* shows a digital photograph of the flexible device/circuit bent in a bending tester. (*C*) A digital photograph of a carbon nanotube circuit fabricated on a flexible polyimide substrate. (*D*) Schematic diagram of the circuit design of the flexible inverter, NAND, and NOR logic gates. (*E*) VTC and noise margin extraction of *o*-MeO-DMBI-I doped flexible SWNT complementary inverters at V_{DD} = 5 V. (*F*) The gain of the inverter at the same V_{IN} range. Output characteristics, static state currents, circuit diagrams, and truth tables of *o*-MeO-DMBI-I doped flexible (*G*) CMOS NOR and (*H*) CMOS NAND logic gates, at V_{DD} = 5 V.

These doped, flexible transistors were able to retain their original device characteristics when bending to a radius of curvature as small as 2.5 mm. Subsequently, SWNT CMOS inverters, NAND, and NOR logic gates were fabricated on the flexible substrates. The flexible CMOS inverter again exhibited an excellent noise margin of 72% of $1/2V_{DD}$ and a gain of 18 whereas the flexible CMOS inverter, NAND, and NOR logic gates all exhibited rail-to-rail voltage swings and subnanowatt static power consumption. The strategy presented here to efficiently tune the threshold voltage of ambipolar SWNT TFTs by molecular dopants provides a versatile approach for realizing large scale SWNT CMOS technologies on flexible substrates.

Materials and Methods

Synthesis of Dopants. The schemes for the synthesis of the dopants are shown in *SI Appendix*, Fig. S1. *o*-MeO-DMBI-I was prepared according to ref. 34 and *N*-DMBI was synthesized according to ref. 39. *o*-MeO-DMBI were prepared according to the following method: A suspension of *o*-MeO-DMBI-I (12 g, 31.56 mmol) in methanol was cooled with an ice water bath (200 mL) followed by the slow addition of NaBH4 (2.39 g, 63.12 mmol) with vigorous stirring. The solution was allowed to warm to room temperature; the solution cleared briefly, after which a white solid precipitated. The solid was collected by vacuum filtration, recrystallized from methanol, and dried in vacuo to give a colorless crystalline product that was consistent with published spectra (5.2 g, 65%) (39).

Fabrication of P3DDT-Sorted SWNTs Devices. The SWNT dispersion was prepared via the following steps similar to our previously reported procedures (1): 5 mg of HiPco SWNTs (Unidym Inc.) and 5 mg rr-P3DDT (Sigma-Aldrich Inc.) were mixed into 25 mL toluene (2). The solution was sonicated using an ultrasonicator (Cole-Parmer 750-Watt Ultrasonic Processor) at an amplitude level of 70% for 30 min (3). The solution was centrifuged for 1 h at 42,000 × *g* (4). The supernatant in the centrifuge tube was carefully extracted and placed into a separate vial to obtain a sorted SWNT solution. The solution was diluted in toluene (1:10), and the device substrate was soaked in this solution for 8 h to deposit a SWNT network. The devices were bottom gated by the highly doped silicon substrate.

Controlled Doping of SWNT Devices. For doping by evaporation, the evaporator system was first evacuated to 10^{-6} Pa. After heating at a power of 2% for 900 s, a temperature between 148 °C and 162 °C is achieved. An evaporation rate 0.02 A/s was maintained around. The thickness of dopants is controlled by deposition times. For doping by spin coating, the dopants were dissolved in ethanol solutions with different concentrations, filtered with 0.2-μm filters and spin-coated from solution onto the SWNT devices at 1,000 rpm (Laurell's WS-400-6NPP-LITE spin coater) for 1 min. Before measurement, the doped devices were annealed on a hotplate in a N_2 glovebox for 60 min at 100 °C.

PES Measurements. Both sorted SWNT films and *o*-MeO-DMBI dopants were coated on 1 cm × 1 cm native oxide silicon substrates (materials coating process same as for devices). PES measurements were performed using a modified VG ESCA Lab system, having an ultrahigh vacuum (UHV) system equipped with a He discharge lamp. The base pressure of the spectrometer chamber was typically 8×10^{-11} torr. The PES spectra were recorded by using unfiltered He I (21.2 eV) excitation as the excitation source. The sample was biased at −5.00 V to observe the low-energy secondary cutoff. The UV light spot size on the sample was about 1 mm in diameter. The typical instrumental resolution for PES measurements is 0.1 eV.

Fabrication of Printed Inverters on Rigid Substrates. First, SWNTs were deposited onto a SiO_2 (300 nm)/Si substrate, followed by the deposition of a patterned Au (40 nm) as the source/drain electrodes through a shadow mask. Devices had channel lengths of 400 μm and channel widths of 20 μm. Then, 5 mg/mL *o*-MeO-DMBI solutions in ethanol were selectively deposited onto the n-channel regions of the complementary inverters by inkjet printing (Fujifilm Dimatix). The nozzle size of the print head was 21.5 μm, and the gap between nozzles was 254 μm. There are 16 nozzles on one print head (Dimatix 11610).

Fabrication of Flexible Transistors and Circuit. Polyimide solution (HD MicroSystems) was first spread over a 4-inch wafer at 500 rpm (Headway PWM32 Spinner) for 30 s and then allowed to rest undisturbed for 1 min. The wafer was then rotated at 1,200 rpm (Headway PWM32 Spinner) for 1 min to form a film. Next, the wafer was annealed at 90 °C for 90 s and then at 115 °C for another 90 s. The wafer was then heated from room temperature to 350 °C at a ramp rate of 2 °C/min and held at 350 °C for 30 min. The patterned gate electrode consisting of 40 nm of Au and 5 nm of Ti, both were then thermally evaporated onto the polyimide. The Ti layer was used to provide nucleation sites for 30 nm of Al_2O_3, which was deposited by ALD at 150 °C onto the gate. The 5-nm Ti and 40-nm Au source/drain electrodes were then patterned by a standard lithography process. The device was then soaked in a solution of rr-P3DDT dispersed semiconducting SWNTs for 14 h and blow-dried with N_2 gas. The SWNTs outside the channel region were etched by oxygen plasma. The dopants were then evaporated on the selected region of the SWNT circuits with filter paper covering the rest of the substrate.

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1. Minhun J, et al. (2010) All-printed and roll-to-roll-printable 13.56-MHz-operated 1-bit RF tag on plastic foils. *Electron Devices. IEEE Transactions on* 57(3):571–580.
2. Dodabalapur A (2006) Organic and polymer transistors for electronics. *Mater Today* 9(4):24–30.
3. Gelinck GH, et al. (2004) Flexible active-matrix displays and shift registers based on solution-processed organic transistors. *Nat Mater* 3(2):106–110.
4. Rogers JA, et al. (2001) Paper-like electronic displays: Large-area rubber-stamped plastic sheets of electronics and microencapsulated electrophoretic inks. *Proc Natl Acad Sci USA* 98(9):4835–4840.
5. Myny K, et al. (2012) An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil. *IEEE J Solid-State Circuits* 47(1):284–291.
6. Wang H, et al. (2010) High-performance field effect transistors from solution processed carbon nanotubes. *ACS Nano* 4(11):6659–6664.
7. Park S, Vosguerichian M, Bao Z (2013) A review of fabrication and applications of carbon nanotube film-based flexible electronics. *Nanoscale* 5(5):1727–1752.
8. Chae SH, et al. (2013) Transferred wrinkled Al_2O_3 for highly stretchable and transparent graphene-carbon nanotube transistors. *Nat Mater* 12(5):403–409.
9. Lipomi DJ, et al. (2011) Skin-like pressure and strain sensors based on transparent elastic films of carbon nanotubes. *Nat Nanotechnol* 6(12):788–792.
10. Lau PH, et al. (2013) Fully printed, high performance carbon nanotube thin-film transistors on flexible substrates. *Nano Lett* 13(8):3864–3869.
11. Wang C, et al. (2012) Extremely bendable, high-performance integrated circuits using semiconducting carbon nanotube networks for digital, analog, and radio-frequency applications. *Nano Lett* 12(3):1527–1533.
12. Sun DM, et al. (2011) Flexible high-performance carbon nanotube integrated circuits. *Nat Nanotechnol* 6(3):156–161.
13. Cao Q, et al. (2008) Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* 454(7203):495–500.
14. Lee SY, et al. (2011) Scalable complementary logic gates with chemically doped semiconducting carbon nanotube transistors. *ACS Nano* 5(3):2369–2375.
15. Weste NHE Harris, DM (2010) *CMOS VLSI Design: A Circuits and Systems Perspective* (Addison-Wesley, Boston) 4th Ed, pp 241–284.
16. De Vusser S, Genoe J, Heremans P (2006) Influence of transistor parameters on the noise margin of organic digital circuits. *IEEE Trans Electron Devices* 53(4):601–610.
17. Bode D, et al. (2010) Noise-margin analysis for organic thin-film complementary technology. *IEEE Trans Electron Devices* 57(1):201–208.
18. Zschieschang U, et al. (2010) Mixed self-assembled monolayer gate dielectrics for continuous threshold voltage control in organic transistors and circuits. *Adv Mater* 22(40):4489–4493.
19. Martel R, et al. (2001) Ambipolar electrical transport in semiconducting single-wall carbon nanotubes. *Phys Rev Lett* 87(25):256805.
20. Ding L, et al. (2009) Y-contacted high-performance n-type single-walled carbon nanotube field-effect transistors: Scaling and comparison with Sc-contacted devices. *Nano Lett* 9(12):4209–4214.
21. Zhang Z, et al. (2007) Doping-free fabrication of carbon nanotube based ballistic CMOS devices and circuits. *Nano Lett* 7(12):3603–3607.
22. Wang C, Ryu K, Badmaev A, Zhang J, Zhou C (2011) Metal contact engineering and registration-free fabrication of complementary metal-oxide semiconductor integrated circuits using aligned carbon nanotubes. *ACS Nano* 5(2):1147–1153.
23. Zhang J, Wang C, Fu Y, Che Y, Zhou C (2011) Air-stable conversion of separated carbon nanotube thin-film transistors from p-type to n-type using atomic layer deposition of high-κ oxide and its application in CMOS logic circuits. *ACS Nano* 5(4): 3284–3292.
24. Shim M, Javey A, Kam NW, Dai H (2001) Polymer functionalization for air-stable n-type carbon nanotube field-effect transistors. *J Am Chem Soc* 123(46): 11512–11513.
25. Zhou CW, Kong J, Yenilmez E, Dai HJ (2000) Modulated chemical doping of individual carbon nanotubes. *Science* 290(5496):1552–1555.
26. Javey A, et al. (2005) High performance n-type carbon nanotube field-effect transistors with chemically doped contacts. *Nano Lett* 5(2):345–348.
27. Derycke V, Martel R, Appenzeller J, Avouris P (2002) Controlling doping and carrier injection in carbon nanotube transistors. *Appl Phys Lett* 80(15):2773–2775.
28. Klinke C, Chen J, Afzali A, Avouris P (2005) Charge transfer induced polarity switching in carbon nanotube transistors. *Nano Lett* 5(3):555–558.
29. Kim SM, et al. (2009) Reduction-controlled viologen in bisolvent as an environmentally stable n-type dopant for carbon nanotubes. *J Am Chem Soc* 131(1):327–331.
30. Kang BR, et al. (2009) Restorable type conversion of carbon nanotube transistor using pyrolytically controlled antioxidizing photosynthesis coenzyme. *Adv Funct Mater* 19(16):2553–2559.
31. Siddons GP, Merchin D, Back JH, Jeong JK, Shim M (2004) Highly efficient gating and doping of carbon nanotubes with polymer electrolytes. *Nano Lett* 4(5):927–931.
32. Geier ML, et al. (2013) Subnanowatt carbon nanotube complementary logic enabled by threshold voltage control. *Nano Lett* 13(10):4810–4814.
33. Wei P, Oh JH, Dong G, Bao Z (2010) Use of a 1H-benzoimidazole derivative as an n-type dopant and to enable air-stable solution-processed n-channel organic thin-film transistors. *J Am Chem Soc* 132(26):8852–8853.
34. Wei P, et al. (2012) 2-(2-Methoxyphenyl)-1,3-dimethyl-1H-benzoimidazol-3-ium iodide as a new air-stable n-type dopant for vacuum-processed organic semiconductor thin films. *J Am Chem Soc* 134(9):3999–4002.
35. Wei P, et al. (2013) Tuning the Dirac point in CVD-grown graphene through solution processed n-type doping with 2-(2-methoxyphenyl)-1,3-dimethyl-2,3-dihydro-1H-benzoimidazole. *Nano Lett* 13(5):1890–1897.
36. Lee HW, et al. (2011) Selective dispersion of high purity semiconducting single-walled carbon nanotubes with regioregular poly(3-alkylthiophene)s. *Nat Commun* 2:541.
37. Park S, et al. (2012) Highly effective separation of semiconducting carbon nanotubes verified via short-channel devices fabricated using dip-pen nanolithography. *ACS Nano* 6(3):2487–2496.
38. Liyanage LS, et al. (2012) Wafer-scale fabrication and characterization of thin-film transistors with polythiophene-sorted semiconducting carbon nanotube networks. *ACS Nano* 6(1):451–458.
39. Naab BD, et al. (2013) Wafer-scale fabrication and characterization of thin-film transistors with polythiophene-sorted semiconducting carbon nanotube networks. *J Am Chem Soc* 135(40):15018–15025.
40. Sze SM (1981) *Physics of Semiconductor Devices* (Wiley, New York).
41. Takenobu T, et al. (2005) Control of carrier density by a solution method in carbon-nanotube devices. *Adv Mater* 17(20):2430–2434.
42. Li F, Werner A, Pfeiffer M, Leo K, Liu X (2004) Leuco crystal violet as a dopant for n-doping of organic thin films of fullerene C_{60}. *J Phys Chem B* 108(44):17076–17082.
43. Maennig B, et al. (2001) Controlled p-type doping of polycrystalline and amorphous organic layers: Self-consistent description of conductivity and field-effect mobility by a microscopic percolation model. *Phys Rev B* 64:195208.
44. Cao Q, et al. (2007) Gate capacitance coupling of singled-walled carbon nanotube thin-film transistors. *Appl Phys Lett* 90:023516.
45. Jin SH, et al. (2012) Sources of hysteresis in carbon nanotube field-effect transistors and their elimination via methylsiloxane encapsulants and optimized growth procedures. *Adv Funct Mater* 22(11):2276–2284.
46. Kim W, et al. (2003) Hysteresis caused by water molecules in carbon nanotube field-effect transistors. *Nano Lett* 3(2):193–198.
47. Hauser JR (1993) Noise margin criteria for digital logic circuits. *IEEE Trans Educ* 36(4): 363–368.
48. Gelinck G, Heremans P, Nomoto K, Anthopoulos TD (2010) Organic transistors in optical displays and microelectronic applications. *Adv Mater* 22(34):3778–3798.
49. Kronemeijer AJ, et al. (2012) A selenophene-based low-bandgap donor-acceptor polymer leading to fast ambipolar logic. *Adv Mater* 24(12):1558–1565.
50. Hur SH, Park OO, Rogers JA (2005) Extreme bendability of single-walled carbon nanotube networks transferred from high-temperature growth substrates to plastic and their use in thin-film transistors. *Appl Phys Lett* 86:243502.
51. Cao Q, Xia M-G, Shim M, Rogers JA (2006) Bilayer organic-inorganic gate dielectrics for high-performance, low-voltage, single-walled carbon nanotube thin-film transistors, complementary logic gates, and p-n diodes on plastic substrates. *Adv Funct Mater* 16(18):2355–2362.
52. Moriyama N, Ohno Y, Suzuki K, Kishimoto S, Mizutani T (2010) High-performance top-gate carbon nanotube field-effect transistors and complementary metal-oxide-semiconductor inverters realized by controlling interface charges. *Appl Phys Express* 3:105102.
53. Maehashi K, Kishimoto T, Ohno Y, Inoue K, Matsumoto K (2012) Complementary voltage inverters with large noise margin based on carbon nanotube field-effect transistors with SiNx top-gate insulators. *J Vac Sci Technol B* 30:03D108.
54. Avouris P, Chen Z, Perebeinos V (2007) Carbon-based electronics. *Nat Nanotechnol* 2(10):605–615.
55. Kobayashi S, et al. (2004) Control of carrier density by self-assembled monolayers in organic field-effect transistors. *Nat Mater* 3(5):317–322.
56. Kergoat L, et al. (2012) Tuning the threshold voltage in electrolyte-gated organic field-effect transistors. *Proc Natl Acad Sci USA* 109(22):8394–8399.