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Single-Chip CMUT-on-CMOS Front-End System for Real-Time Volumetric IVUS and ICE Imaging

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Abstract

Intravascular ultrasound (IVUS) and intracardiac echography (ICE) catheters with real-time volumetric ultrasound imaging capability can provide unique benefits to many interventional procedures used in the diagnosis and treatment of coronary and structural heart diseases. Integration of CMUT arrays with front-end electronics in single-chip configuration allows for implementation of such catheter probes with reduced interconnect complexity, miniaturization, and high mechanical flexibility. We implemented a single-chip forward-looking (FL) ultrasound imaging system by fabricating a 1.4-mm-diameter dual-ring CMUT array using CMUT-on-CMOS technology on a front-end IC implemented in 0.35-μm CMOS process. The dual-ring array has 56 transmit elements and 48 receive elements on two separate concentric annular rings. The IC incorporates a 25-V pulser for each transmitter and a low-noise capacitive transimpedance amplifier (TIA) for each receiver, along with digital control and smart power management. The final shape of the silicon chip is a 1.5-mm-diameter donut with a 430-μm center hole for a guide wire. The overall front-end system requires only 13 external connections and provides 4 parallel RF outputs while consuming an average power of 20 mW. We measured RF A-scans from the integrated single-chip array which show full functionality at 20.1 MHz with 43% fractional bandwidth. We also tested and demonstrated the image quality of the system on a wire phantom and an ex-vivo chicken heart sample. The measured axial and lateral point resolutions are 92 μm and 251 μm, respectively. We successfully acquired volumetric imaging data from the ex-vivo chicken heart with 60 frames per second without any signal averaging. These demonstrative results indicate that single-chip CMUT-on-CMOS systems have the potential to produce real-time volumetric images with image quality and speed suitable for catheter based clinical applications.

Keywords

Ultrasound imaging; CMUT-on-CMOS; IVUS; ICE

Introduction

Generating true volumetric ultrasound images in front of a flexible catheter would be beneficial in the diagnosis and treatment of arterial diseases such as chronic total occlusions (CTOs) and complex transcatheter interventions in the heart [1]. Several different approaches have been developed for implementing volumetric IVUS and ICE catheters based on mechanical rotation [2, 3]. 2-D Solid state arrays provide a more robust and compact solution. Ring-shaped annular arrays that allow a center opening for a guide-wire for IVUS applications and a port for interventional devices in case of ICE, are especially suitable for forward-looking (FL) volumetric imaging for guiding interventions [4, 5]. The first attempt on realization of these arrays used a single ring piezoelectric transducer array [6]. This structure combined side-looking (SL) IVUS ring array with FL-IVUS by utilizing different vibration modes of the piezoelectric elements and relied on the same integrated electronics as the SL-IVUS system. The small sizes of the transducer elements, strong cross coupling, and difficulties in reliable fabrication have limited the success of this approach. More recent piezo based ring arrays may have similar issues [7]. Capacitive micromachined ultrasonic transducer (CMUT) technology has potential to overcome most of these limitations as it offers flexibility to fabricate arrays of different shapes and sizes [4, 5, 8–10]. In addition, it enables monolithic or flip-chip-bonding-based electronics integration [11–14]. Single-ring 64-element annular CMUT arrays operating at 15.5 MHz, 19 MHz and 13.5 MHz have been demonstrated for FL-IVUS [4, 5, 15]. A 64–element 10 MHz single-ring CMUT array was integrated in a multi-chip, flip-chip-bonded package for FL-ICE [10, 16]. More recently, a single ring array was connected to a commercial ultrasound system to demonstrate and compare its imaging capabilities in different modes including full phased array and synthetic aperture processing with spatially coded excitation for high frame rate imaging with improved SNR, respectively [17]. These systems use the same array of elements for both transmit (Tx) and receive (Rx) which results in a suboptimal noise performance because of the protection/switching circuits [18]. Furthermore, since each element is still connected to the outside system, the number of cables in the catheter is quite large.

Dual-ring annular CMUT arrays with separate Tx and Rx rings enable separate optimization of Tx and Rx element geometry and electronics for higher SNR with negligible loss in resolution [18–20]. For successful realization of FL-IVUS imaging catheters with small sized elements, close integration of front-end electronics and the transducer array within the catheter is very critical. Compared to a multi-chip integration scheme that requires many chip-to-chip interconnects, a system that integrates the transducer array with Tx and Rx electronics on a single chip has several advantages. This approach can significantly mitigate the interconnection complexity and reduces the required steps in the manufacturing of the FL-IVUS probe. In addition to these manufacturing advantages, one can multiplex receive channels after front-end pre-amplification, and thus the ultimately miniaturized single-chip FL-IVUS system can be as thin as 1 mm with ~10 cables. This, along with a through-silicon via for each electrical connection, can lead to a flexible catheter tip for easy navigation through tortuous arteries as shown schematically in Fig. 1. FL-ICE catheters should also enjoy similar benefits with more relaxed size constraints.

We recently realized a single-chip volumetric imaging system using monolithic CMUT-on-CMOS integration where dual-ring CMUT arrays were fabricated directly on top of pre-processed custom designed CMOS wafers and presented some initial results in conferences [21, 22]. Here, we present the design, testing and quantitative characterization of the overall single-chip front-end system suitable for volumetric IVUS and ICE imaging.

The paper is organized as follows: Section II briefly describes the monolithically fabricated dual-ring CMUT arrays. We present the design and characterization of integrated front-end electronics in section III. Then we describe the imaging setup and present detailed results on array characterization in Section IV. We demonstrate volumetric imaging results and provide quantitative analysis in section V. Finally we discuss the results and future improvements in Section VI.

II. Design and Fabrication of Dual-Ring CMUT-on-CMOS Array

Monolithic fabrication of CMUT arrays on top of pre-processed CMOS wafers reduces parasitic capacitances [11, 18], and reduces the complexity of design while optimizing the use of silicon area. The 0.35-μm CMOS electronics for the system are fabricated by TSMC (Taiwan Semiconductor Manufacturing Company) foundry on 200 mm silicon wafers which contain 48 repeating dies per wafer. The wafers are subsequently diced into 6 rectangular reticles approximately 4 cm by 7 cm (3 × 2 die) to allow for CMUT fabrication using standard micromachining tools designed for 100 mm (4 inch) wafers. The picture of the CMOS wafer with custom designed IC's is shown in Fig. 2. To fabricate CMUT arrays on the CMOS electronics, a low temperature process is used. Detailed information about the particular CMUT-on-CMOS fabrication process can be found in [11].

The dual-ring arrays used in this study consist of 56 Tx (outer ring) and 48 Rx (inner ring) elements with 1.31 mm and 1.13 mm center diameters, respectively. The device was first fabricated as full rectangular pieces and then etched to form a donut shape which is suitable for guide wires (Fig. 3-right). In the particular array the Tx and Rx elements are identical. Each element contains 4 individual membranes and is approximately 70 μm × 70 μm in size. The CMUT element capacitance is calculated to be 90 fF. Table I summarizes the physical parameters of the fabricated CMUT array. The membrane thickness and lateral size are determined by the center frequency and the trade off between the coupling coefficient and fractional bandwidth, which is well balanced with a 50% fractional bandwidth in this case [23]. With a gap thickness of 120 nm, chosen for ease of fabrication, a collapse voltage is 140V is obtained. Overall, these geometrical parameters are not optimized in terms of overall CMUT performance, but provides a good balance between bandwidth, coupling coefficient and ease of fabrication.

III. Single-Chip System for FL-IVUS

To implement the necessary receive and transmit electronics in a single chip we custom designed an 8-inch wafer reticle in 0.35-μm CMOS process. The ICs in this wafer are custom designed for monolithic integration of FL-IVUS array with 1.4 mm diameter. Fig. 3-left shows a micrograph of the IC designed for FL-IVUS dual-ring array. This IC incorporates 48 low-noise receiver amplifiers and 56 pulsers, dedicated to receive and

transmit elements in the array, respectively. The chip also includes buffers and a digital control circuitry that is designed to synchronize transmitting and receiving sequence during the data acquisition.

Fig. 3-right shows the external electrical connections to the imaging device. The RF data from 4 receive channels (*Out1-Out4*) are collected in parallel. The *Clk* input has two functionalities. Its main function is to increment the counter in the digital control circuitry, which synchronizes the chip. It is also used to generate the pulse trigger signal that is routed to the active pulser circuitry. *Clr_ctr* is the clear signal for the digital counter. *V_pulse* voltage input controls the magnitude of the high-voltage pulse. *Ctrl1* and *Ctrl2* are the two control voltages used in the preamplifiers. Two separate CMUT bias signals (*V_Rx* and *V_Tx*) are provided for the separate receive and transmit CMUT rings.

Note that this single-chip system requires only 13 external connections with the *vdd* and *gnd* connections. This figure can be reduced to 8 while still keeping 4 parallel RF outputs. This would be achieved by generating the CMUT and transmit pulser DC levels on-chip from a single DC bias input, and eliminating the amplifier tuning capability which was included for testing purposes. Considering that the current 64-element SL-IVUS catheter [24] requires more than 200 chip-to-chip and chip-to-transducer electrical interconnect bonds and only provides a single output channel, the enormous advantage of this novel single-chip approach can be better appreciated.

Note that some areas in the center and the perimeter of the IC are left free of any metal traces or active CMOS circuitry to enable etching through the silicon substrate to create the final donut shape suitable for placement on a tip of a circular catheter. The diameter of the gap at the center reserved for the guide wire is 430 μm. All the active circuitry and the CMUT array fit under a 1.5-mm-diameter silicon donut. The connection areas outside the diameter of the CMUT array are placed for initial testing of the IC with wire-bonding and would be omitted in the final catheter implementation.

In catheter-based applications the power requirement is tight to prevent over-heating of the dense single-chip system. For instance, in [25], the average power budget for solid-state IVUS catheters is noted as 100 mW to make sure that the temperature of the catheter does not increase to damaging levels when the catheter is powered and allowed to dry. In this work, the power requirement is addressed from two different angles. Primarily, to reduce the power consumption, a power on-off capability is added to the receive amplifier. The amplifiers that are not actively used are biased off by the digital logic and at any given time only four of the amplifiers that are connected to the outputs are kept active. Concurrently, to further reduce the chip power consumption, the receive amplifiers are designed with a low power consumption (0.8 mW) without significantly compromising their performance.

A. Preamplifier Design

To measure RF echo signals from CMUTs integrated with FL-IVUS front-end chips, we designed two different low-noise receive amplifiers based on two different architectures, namely the resistive-feedback transimpedance amplifier (TIA) architecture and the capacitive feedback TIA architecture. The resistive feedback TIA implemented here is a

revised version of the amplifier that was presented in [18]. A detailed discussion of the modifications, gain, and bandwidth and noise performance of this amplifier design was given in [26, 27]. For brevity, here we only discuss the details of the capacitive-feedback TIA design (Fig. 4).

This capacitive-feedback architecture TIA employs a current amplification to generate I_{OUT}, which gets multiplied by R_D to obtain a voltage output [28]. This architecture is especially promising for low-noise detection because it does not involve a noisy resistor in the feedback network. The total input capacitance including the amplifier input capacitance ($C_{IN,\,AMP}$), any parasitic interconnect capacitance (C_{PAR}) and the CMUT capacitance (C_{CMUT}) is referred as C_{IN} in the following expressions.

Assuming $C_1A_0 \gg C_{IN} + C_1$ and $C_2 \gg C_1$ the transfer function of the feedback system in Fig. 4 yields the following transfer function:

$$\frac{V_{OUT}}{i_{IN}}(s)=\frac{\left(1+\frac{C_2}{C_1}\right)R_D\left(1+\frac{s}{\frac{C_2}{C_1}A_0\omega_0}\right)}{1+\frac{s}{\omega_N Q}+\frac{s^2}{\omega_N^2}}, \quad (1)$$

where

$$\omega_N^2=\frac{C_1A_0\omega_0 g_{m1}}{(C_1+C_{IN})C_2} and\, Q=\frac{\omega_N}{\omega_0+g_{m1}/C_2}. \quad (2)$$

In these expressions, s is the complex frequency (Laplace variable); g_{m1} is the transconductance of M_1; A_0 and ω_0, respectively, are the open-loop voltage gain and radian frequency bandwidth of the core amplifier consisting M_2 and M_3. The transfer function in (1) exhibits a zero but it is at a relatively high frequency and can be neglected. To analyze the behavior of this second-order system assume a dominant-pole case where the transfer function is written as

$$\frac{i_{OUT}}{i_{IN}}(s)=\frac{1}{\frac{s^2}{\omega_{dom}\omega_2}+\frac{s}{\omega_{dom}}+1} \quad (3)$$

where

$$\omega_{dom}=\frac{C_1A_0\omega_0 g_{m1}}{C_2(C_{IN}+C_1)\left(\omega_0+\frac{g_{m1}}{C_2}\right)} and\, \omega_{dom}\omega_2=\frac{C_1A_0\omega_0 g_{m1}}{(C_{IN}+C_1)C_2}. \quad (4)$$

In this expression ω_{dom} represents the dominant pole and ω_2 is the second (non-dominant) pole of the closed-loop system. Further assuming that $\omega_0 \gg g_{m1} / C_2$, the 3-dB bandwidth and the non-dominant pole of the system can be given as

$$\omega_{dom}=\omega_{-3dB}=\frac{C_1 A_0}{(C_{IN}+C_1)}\frac{g_{m1}}{C_2},\omega_2=\omega_0 \quad (5)$$

It should also be noted that to ensure stability, $\omega_0 > \frac{2C_1A_0}{(C_{IN}+C_1)}\frac{g_{m1}}{C_2}$.

In this work, the simulated open-loop voltage gain (A_0) and the bandwidth of the core amplifier is 44 and 380 MHz, respectively. The simulated transconductance of M_1 is g_{m1}=10 μS; the total input capacitance is C_{IN} = 150 fF which includes the CMUT capacitance, C_{CMUT} = 90 fF, and the input capacitance of the core amplifier, C_{IN_AMP} = 60 fF. The effective C_1 includes the drawn capacitance, which is 25 fF, and the drain-to-source capacitance of M_5, which is around 30 fF. Therefore, in this implementation, the effective C_1 is around 55 fF.

The input referred spectral density of the current noise is expressed as:

$$\overline{i_{in}^2}=\frac{1}{\left(1+\frac{C_2}{C_1}\right)^2}\left(\frac{4kT}{R_D}+i_{dbias}^2\right)+\omega^2(C_{IN}+C_1)^2\frac{\overline{i_d^2}}{g_m^2}, \quad (6)$$

where g_m is the transconductance, and i_d^2 is the spectral density of the current noise square of the input transistor of the core amplifier that dominates the core amplifier noise. Similarly, i_{dbias}^2 represents the spectral density of the current noise square of the current bias circuitry that provides the bias current (I_{bias}) for M_1. Although, not shown in (6) explicitly, M_1 also contributes some noise. However, the voltage noise at the gate of M_1 gets divided by the large A_0 value while getting referred to input and therefore noise of M_1 can be neglected. From (6) it can be seen that the current noise terms of the bias circuitry and the load resistance (R_D) gets divided by the current gain when referred to input, which is advantageous to get a low input-referred noise. Note that the input DC node floats when the feedback network only contains capacitances. Therefore a method is required to apply a DC bias to the input node. In this implementation, a MOS-bipolar device (M_5) is used in parallel with the feedback capacitance [29]. This acts as a very large value (on the order of a Giga-Ohm) pseudo-resistor and provides a DC path to the input node. Due to its very high effective resistance value, the noise of M_5 is negligible. The design consumes a 25 × 55 μm^2 area and the simulated power consumption is 240 μA. Note that most of the current is consumed by the core amplifier (M_2–M_3).

B. Buffer Design

Each receiver set contains a buffer to drive the interconnect cable and scope capacitances. The designed buffer is a push-pull buffer including two source follower stages. The buffer is designed to have a wide bandwidth that is higher than 50 MHz with a 50-Ω resistive load. With a 50-Ω load (i.e. the case when driving a 50-Ohm input of a network analyzer), the gain of the buffer stage is around 0.28 V/V. Note that a buffer gain value that is less than unity does not have a negative effect on system SNR because both signal and noise are

scaled by this gain. The buffer consumes 1.2 mA of DC current and covers an area of 35 μm × 50 μm.

C. Measured Amplifier Characteristics

To measure the transimpedance characteristics of the design amplifier we used the setup shown in Fig. 5. For gain testing, the CMUT element itself was utilized to mimic an on-chip high impedance to convert the test voltage input to a current input into the amplifier. The details of this method of testing an integrated TIA-CMUT couple can be found in [18]. To extract the TIA gain from the overall voltage gain measurement, a 90-fF is used as the CMUT capacitance. Fig. 6 shows the gain measurement of the designed capacitive-feedback amplifier. The measurement result demonstrates a transimpedance gain of 200 KΩ with a 40-MHz bandwidth. The simulated closed-loop transimpedance gain is 160 KΩ and the bandwidth is 90 MHz on nominal process parameters. On a slow process corner, the simulated bandwidth drops to 35 MHz. Therefore, the measured 40-MHz bandwidth is within the simulated range.

To measure the noise characteristics of the designed TIA, we connected one of the outputs of the post processed IC to an Agilent 4395A in spectrum analyzer mode. To measure the front end electronics noise only, we did not apply any bias to the receiver CMUT. The input noise value of the capacitive-feedback TIA was obtained by dividing the measured output noise value by the buffer gain and the TIA gain (Fig. 7). Table II outlines the measured characteristics of the capacitive feedback preamplifier design. The measured 310-fA/√Hz input-referred noise level at 20-MHz agrees with the simulation results. Note that the measured input-referred current noise level of the amplifier is on the order of the thermal-mechanical noise of the CMUT elements, critical for the SNR of the system [18, 30]. It should also be noted that the input-referred current noise performance of this particular design is limited by the available area. The noise level can be significantly improved with a more relaxed area requirement, which enables increasing the values of C_2 and R_D.

D. High-Voltage Pulser

The breakdown voltages of regular devices in the standard 0.35 μm CMOS technology that the wafer is fabricated in are less than 10 V. To achieve higher pulse voltages, a high-voltage NMOS based on an “Extended Drain” design approach is used [31]. Fig. 8 shows the pulser circuit implemented on-chip based on this high-voltage NMOS design. The resistor (R) is implemented with a poly resistor. The pulser converts the 3.3-V unipolar input pulse into a unipolar high-voltage pulse. The width of the output pulse is controlled by the width of the low-voltage trigger pulse. To reduce the power consumption, the steady state voltage of the output pulser is kept at high voltage. The output switches from high to low when the input trigger pulse arrives.

To eliminate a dedicated external connection, the low-voltage pulse trigger signal is generated through the *Clk* input. The *Clk* signal is internally delayed for around 10 ns and then routed to the active pulser circuitry with the digital logic. The 10-ns delay is long enough for the switching transient to settle, which ensures that the intended pulser to which the trigger signal needs to be routed is properly selected. Note that, the pulse width of the

low-voltage *Clk* input determines the width of the output pulse. Each pulser consumes 35 × 50 μm^2 area.

E. Digital Control and Power Management

A digital control block is designed to synchronize the operation of the transmitter and receiver elements in the array. During the initial pulsing stage a single transmitter pulses and during the receive sequence four receive amplifiers are connected to the outputs. The digital block controls which of the four amplifiers are the active receivers and also which particular pulser is the active transmitter at any given time. It changes the active elements during the data collection with a single clock and the whole imaging process is completed in 1024 clock cycles.

For development and testing purposes, we have fabricated arrays with different element counts up to 64 Tx and 64 Rx elements. To use the front-end IC for such different array sizes we designed the electronics for array sizes of 64 elements as Tx and Rx. In this design, the control circuitry does not reset the pulse repetition. However, one can reconfigure the design for fixed size array configuration.

Fig. 9 shows a simulated timing diagram depicting the operation flow for the power control. Transmit trigger signal is generated approximately 10 ns after the receiver is enabled. In this figure, the pulse repetition rate is 20 μs and the pulse width is 20 ns, similar to normal operating conditions. A small signal is applied to the TIA input to show that the output is generated only when the power is turned on. When receive amplifier bias voltage is switched to “On” position, it takes around 100 ns for the amplifier output to settle down to proper operation range. A peaking occurs during the transition of the amplifier output but it stays within the safe voltage limits of the transistors. With only 4 TIAs active at any time, and with negligible duty cycle of the transmit pulsers, the average power consumption of the chip is about 20mW, mainly dominated by the output buffers.

IV. System Characterization

A. Experimental Setup

To demonstrate imaging performance of the single chip dual ring CMUT-on-CMUT arrays, a custom data collection setup was constructed. The fabricated CMUT array was first wire-bonded to a ceramic dual inline package (DIP) chip holder with 13 connections and placed at the bottom of a small petri dish. The chip holder was placed in a custom PCB for data acquisition and control signal connections. The RF output channels were digitized using 2 dual-channel digitizer cards (Spectrum UltraFast M3i.4142) with 14-bit ADCs and 250 MS/s sampling rate. The clock signal for the digital control of the IC was generated by the external digital I/O of the digitizer card. During each clock signal a transmit element was fired and 4 parallel Rx output channels were digitized simultaneously. The acquired data were transferred from digitizer’s memory to the local hard drive for further data processing and image reconstruction.

B. Analysis of the Pulse-Echo Data

To characterize the performance of dual-ring array elements prior to the volumetric imaging experiments, we acquired pulse-echo data from an oil-air interface at nearly 10 mm above the array, where all RF A-scans from 56×48 Tx-Rx element combinations were collected. Both Tx and Rx arrays were operated in conventional mode and with the same DC bias at 90% of the collapse voltage. We used 25-V unipolar and 30-ns pulse width, which was experimentally optimized for maximum echo amplitude. We processed the raw RF A-scan data by a digital band-pass filter with a 10–30 MHz pass-band to eliminate out-of-band noise. Fig. 10 shows pulse-echo and frequency response of a single pair of array elements from oil-air interface indicating 20MHz center frequency and about 50% 6-dB fractional bandwidth. The spurious response following the main echo is 15 dB lower and is due to acoustic crosstalk in the array. A properly designed filter can clean spurious response which is low frequency in nature. The distribution of the center frequency and bandwidth for different Tx and Rx elements are shown in Fig. 11, where the 51^{st} and 9^{th} elements were the reference Tx and Rx elements, respectively. The average center frequency is 20.1 MHz with 2% standard deviation of the center frequency, where the average FBW is 43%, showing the uniformity suitable for array imaging.

The SNR A-scans calculated as the ratio of RMS amplitude in a time window including the echo signal from the plane reflector (oil-air interface) to the RMS amplitude in time window including no echo from the reflector, measured over transmit and receive array can be seen in Fig. 12. The average SNR for a single element pulse echo for the plane reflector at 10 mm away from the array is 19 dB without any averaging. In this particular array one of the transmit channels was not functional due to a missing connection in the CMOS electronics layout. All other system components worked with full functionality.

V. Volumetric Imaging Results

The current chip sequentially uses single Tx-Rx pairs, so that all Tx and Rx combinations are available for off-line processing of data for different synthetic aperture beamforming strategies. Despite this arrangement limiting the data collection speed, the imaging potential of the single-chip CMUT-on-CMOS dual-ring array was evaluated using a wire phantom and performing *ex vivo* imaging on a chicken heart sample. For image reconstruction all A-scans from 56×48 Tx-Rx combinations were collected to perform off-line processing and beamforming. Each A-scan was recorded for 25-μs with a sampling rate of 250 MS/s with 14 bit resolution and pulse repetition rate of 40 kHz. Note that sufficient amount of time was reserved for the successive firings to ensure the waves inside the medium were attenuated (~60 dB in oil and tissue). With 4 parallel RF channels, this results in 60 fr/sec data acquisition rate, suitable for real-time volumetric imaging.

A custom RF beamforming software was written to process A-scan data. Following band-pass filtering of data in the 10–30 MHz band, we applied synthetic phased array beamforming using standard delay-and-sum method to calculate the image intensity in each image voxel by using dynamic transmit and receive focusing [4, 32]:

$$I(u)=\sum_{i=1}^{N_t}\sum_{j=1}^{N_r} w_a(i,j)w_n(i,j)s_{ij}(m), \quad (7)$$

where u is the 3-D cartesian coordinates of the image voxel as (x,y,z); $s(.)$ is the sampled RF A-scan; m is the sample index corresponding to the total flight time in terms of number of sample; $w_a(.)$ is the apodization coefficient; $w_n(.)$ is the Norton's weightings coefficient for ring array apertures; the first and second sums are over the N_t transmit and N_r receive elements, respectively; f_s is the sampling frequency; and c is the sound velocity in oil. The sample index m is calculated as:

$$m=round\left\{(|u-u_i|+|u-u_j|)\cdot\frac{f_s}{c}\right\}, \quad (8)$$

where u_i and u_j are the 3-D position vectors of transmit and receive elements, respectively. To suppress the sidelobes in the reconstructed images, a cosine apodization function was applied radially on the aperture. In addition Norton's weighting function defined for ring arrays was applied to obtain full circular aperture resolution [5, 6, 33]. This expression is a direct realization of synthetic phased array image reconstruction, where the dynamic transmit and receive focusing delays were included in the flight times implicitly. For envelope detection, time-delayed sampling technique was used to extract the quadrature component from the received signal [34]. Following envelope detection, logarithmic compression for a desired display dynamic range was applied to produce the final image.

An imaging phantom of four 100-μm-diameter metal wires was used for quantitative testing of point resolution. The wires were immersed in oil and diagonally located on planes parallel to *xy* plane at different depths (4 mm, 5.2 mm, 6.6 mm and 8.2 mm). The reconstructed B-scan image for *xz* plane is shown with 40 dB dynamic range in Fig. 13-left. Simulated ideal 2-D PSFs for the wire target locations were produced with 50% FBW Gaussian pulses without any noise and plotted with 40-dB dynamic range in Fig. 13-right. The grating lobe artifacts for the first and second wire targets are seen at nearly 90 degrees angle in the B-scan. This is expected since the inter element distance of the array elements was 74 μm which is close to the wavelength for 20 MHz center frequency. It should be noted that the grating lobe level for the simulated PSFs is 45 dB and hence they are not observed in the simulated PSF image. The grating lobe artifacts for the first and second wire targets are seen at nearly 90 degrees angle in the B-scan. Since the inter-element distance for this 20-MHz test array was 74 μm, close to wavelength, such grating lobe artifacts spaced laterally approximately 90-degrees away from the targets were expected. These grating lobes can be avoided by implementing ring arrays with reduced inter-element spacing.

Fig. 14 compares experimental and simulated lateral (1-D) PSFs for the second wire target which was located on axis. The experimental lateral PSF was calculated by taking the axial average over a window covering the axial spreads. The experimental wire image and simulated PSF show close agreement around the main lobe. The noticeable differences between two PSFs are the multiple reflections on the axial direction and near peak sidelobe levels. The finite wire thickness and acoustic cross talk are the main reasons for this

structure. The axial multiple reflections are monotonically decreasing and measured as 20 dB lower than the main lobe peak which is consistent with the secondary echo level showed in the A-scan (Fig. 10). The peak sidelobe level in the experimental PSF is 5 dB higher as compared to the simulated PSF, whereas the far sidelobes remain under −30 dB in both PSFs. The experimental wire images also show asymmetry around the target due to the non-uniformity of array element responses. Table III summarizes the measured image parameters and compares them to the simulated values. The 100-μm wire target, larger than the wavelength (75 μm), does not ideally represent the point response. However, for the purpose of obtaining 2-D lateral resolution (PSF), which is ~250 μm for the 2nd wire (see Table III), it is adequate. Overall, the values are within ± 10% of each other in terms of resolution metrics.

We have computed experimental image SNR for the second wire target by calculating the ratio of rms values of image pixels within the 6-dB windows of the target main lobe to the rms of image pixels in a window near to the target without including any target echo. The image SNR for the nearest wire, which has the maximum image SNR as expected, is calculated as 48 dB. We also calculated an average image SNR by measuring the image SNR values of all four wire targets. As a result, the single-chip device produces 43-dB average image SNR for the wire phantom. The theoretical image SNR produced by synthetic phased array beamforming using RF data is expressed as [35]:

$$SNR_{Image}=20\log_{10}\left(\frac{\sum_{n=1}^{N_T}\sum_{m=1}^{N_R}a_{n,m}}{\sqrt{\sum_{n=1}^{N_T}\sum_{m=1}^{N_R}a_{n,m}^2}}\right)+SNR_{Ascan} \quad (9)$$

where $a_{n,m}$ is the channel gain corresponding to n^{th} transmit and m^{th} receive operation. Here, $a_{n,m}$ is estimated as the rms of RF A-scan data in a time window consisting the target echo by using the oil-interface data.

To demonstrate 3-D volumetric imaging on a medically relevant sample, we used an ex-vivo chicken heart phantom. The phantom was immersed in oil inside the Petri dish and placed approximately 2.5 mm above the array surface as shown in Fig. 15. We reconstructed cross-sectional B-scan images in xz and *yz* planes as well as 3-D rendered image from the chicken heart phantom without any signal averaging. The *xz* and *yz* plane B-scan images with 40-dB dynamic range are presented in Fig. 16. The image size is 10 mm in both dimensions. The brightest spot in the image is the reflection from the closest wall of chicken heart phantom to the array. Although the aperture size of the CMUT array is very small compared to the phantom, the apex of the phantom is clearly visible in the B-scan images. The computed experimental image SNR for the brightest location of the image is 44 dB. We also calculated the contrast-to-noise ratio (CNR) using the following expression

$$CNR=\frac{|\mu_B-\mu_S|}{\sigma_S}, \quad (10)$$

where μ_B is mean intensity in dB of bright spot of the chicken heart image, μ_S and σ_S are the mean and standard deviation of the intensity in dB within the speckle [32]. The measured CNR from the chicken heart image is 2.6. These images also show that 14 dB image SNR is

obtained after nearly 3 mm propagation in oil and 4 mm sound penetration in heart tissue at 20 MHz at an angle of 35 degrees.

VI. Discussion

The imaging results presented here were obtained using the first generation CMUT-on-CMOS single chip system. These results demonstrate the viability of the designed front-end system for volumetric FL-IVUS and ICE imaging. Several further improvements can be explored to enhance the image SNR and imaging speed. By reducing the gap thickness from 120 nm to 50 nm, the receive SNR can be improved by about 4 dB [36]. With the same 50 nm gap thickness and 25V available pulse amplitude, 5 dB improvement in output pressure is predicted based on a detailed non-linear model [37]. Further SNR improvements up to 14 dB should be possible using coded excitation schemes without increasing data collection time [38]. These SNR improvements can easily overcome a 16 dB diffraction loss when extending the imaging range from ~7 mm to 4 cm. Considering that the ultrasound attenuation in blood (0.2dB/(MHz.cm)) is about 5–7 times less than that of heart muscle [39–41], these front-end systems can be used for several ICE applications at 20MHz [3]. In addition, these improvements can be combined with the flexibility of CMUT-on-CMOS approach for placing array elements at any desired location on the CMOS electronics. Using this flexibility, instead of the dual-ring annular array the locations of the Tx and Rx elements can be determined to collect spatial information with less number of Tx-Rx combinations [20]. Using spatially and temporally coded signals, a powerful defocused Tx array can be implemented [32, 42]. These methods can be used to decrease the number of firings significantly for increasing imaging speed, especially for ICE applications. Finally, given the computational power offered by the latest GPUs, it seems quite feasible to implement a real-time 3D imaging system based on the CMUT-on-CMOS systems described here [43, 44].

VII. Conclusions

The objective of this work was to show a monolithic CMUT array and circuitry suitable for 3-D imaging FL-IVUS and FL-ICE catheters. We successfully implemented 20 MHz single-chip CMUT-on-CMOS front-end system with dual annular ring structure for this purpose. We successfully implemented a single-chip CMUT-on-CMOS front-end system with dual annular ring structure for FL-IVUS and FL-ICE imaging. This integrated front-end system includes both high-voltage pulser and low-noise receiver circuitry dedicated to each Tx and Rx array element on the array. The single-chip integration reduces the interconnect complexity significantly, enables separate Tx and Rx circuitry for low noise operation, and leads to the ultimate miniaturization. The front-end system, which can be further reduced in size, currently fits into a size of a 1.5-mm diameter, 300-μm thick donut shape suitable for placement at the tip of a catheter with only 13 external cables; its total power consumption is 20 mW. Overall system characterization indicates CMUT uniformity and performance suitable for real-time volumetric imaging.

Acknowledgments

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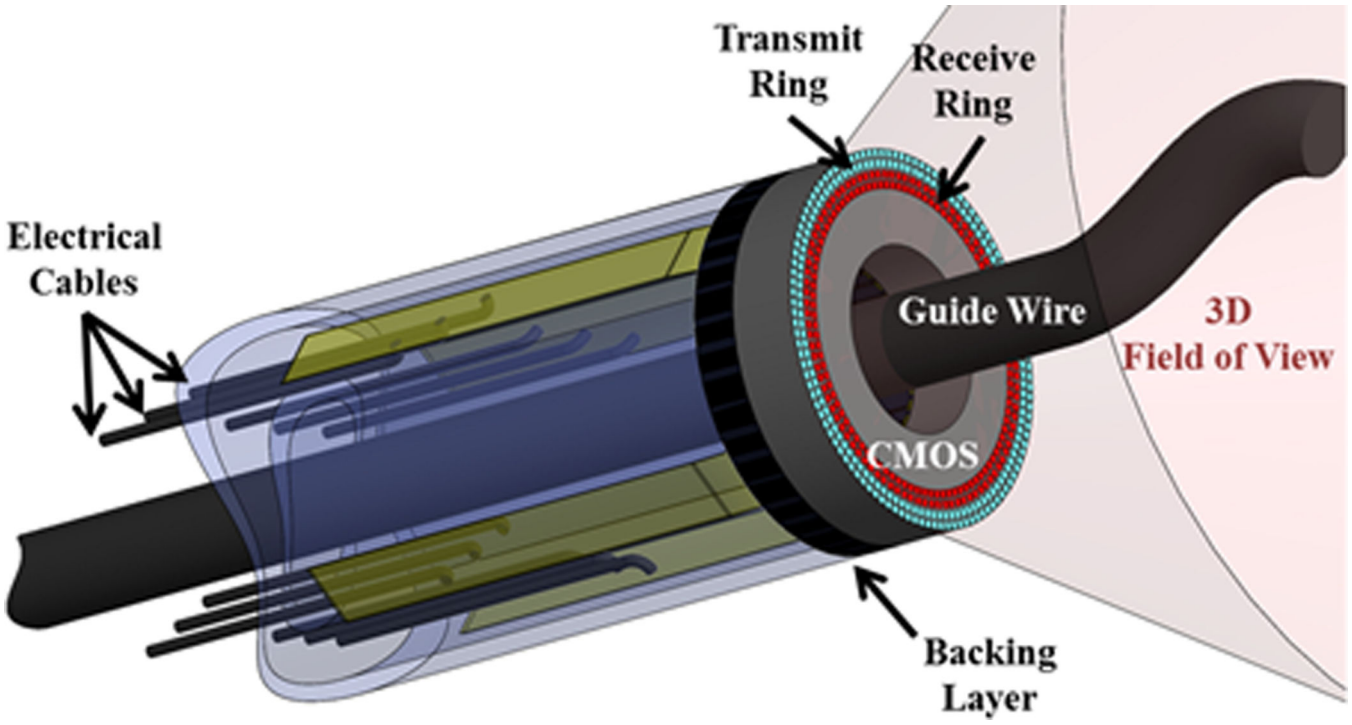

Fig. 1.

Conceptual drawing of a single-chip fully-integrated FL-IVUS imaging catheter based on a dual-ring CMUT array monolithically integrated with the complete front-end CMOS IC.

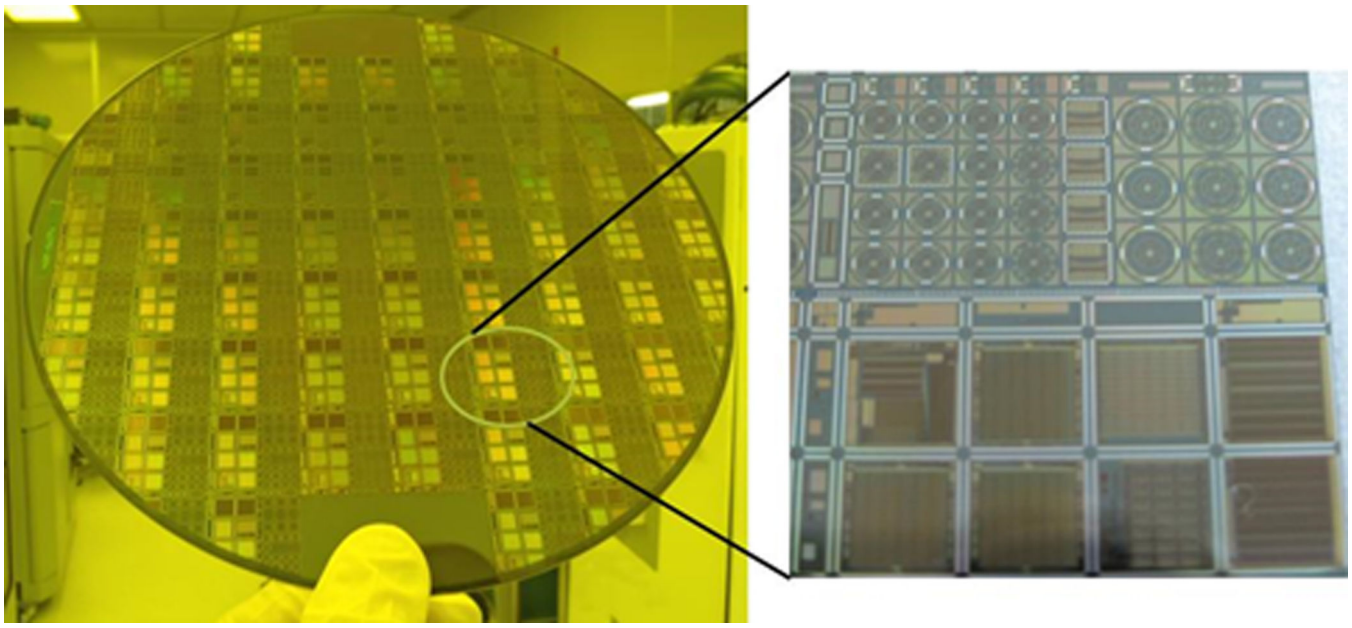

Fig. 2.
(Left) The picture of the 8-inch CMOS wafer fabricated in 0.35-μm CMOS. (Right) Picture of the reticle of the wafer that contains the custom-designed ICs

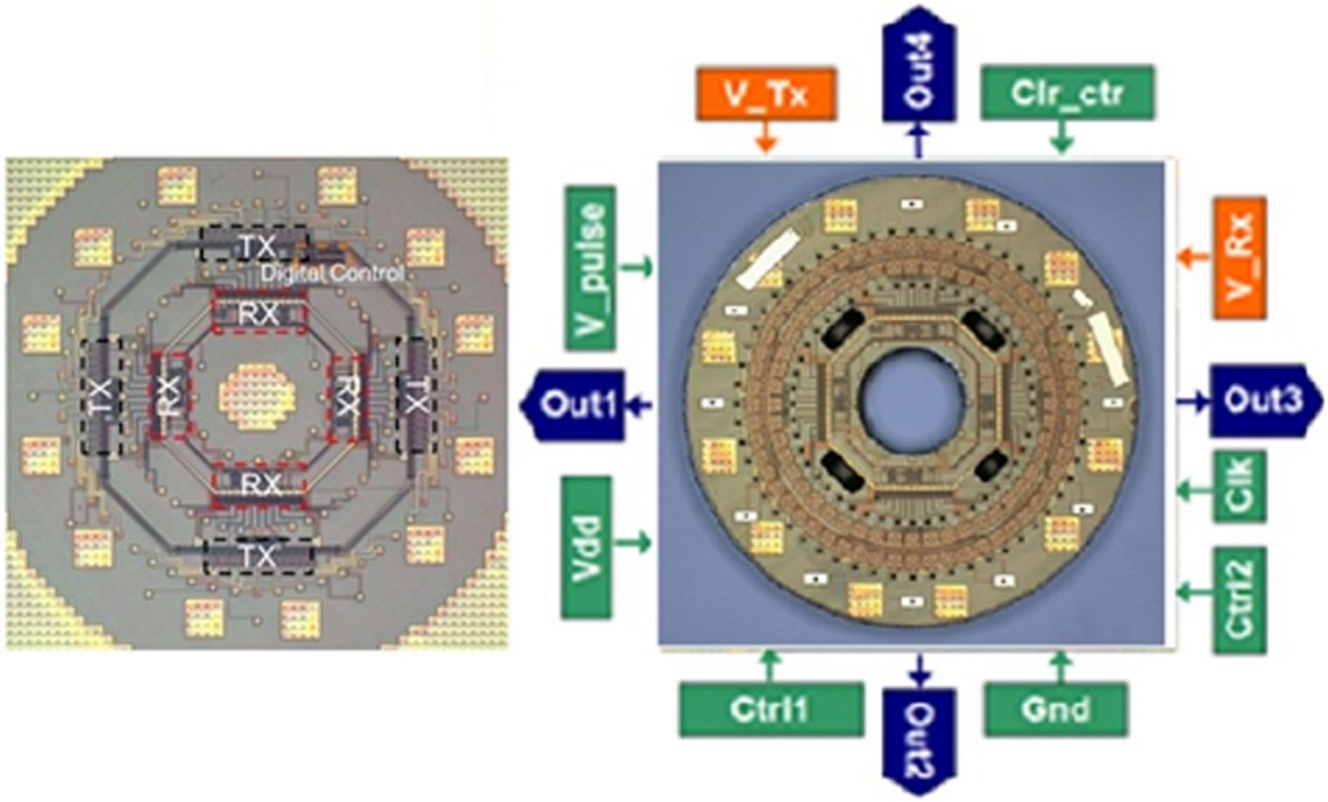

Fig. 3.

(Left) The micrograph of the IC designed for a 1.4-mm FL-IVUS dual-ring array with 56 Tx and 48 Rx elements. The IC includes 48 receive amplifiers, 56 pulser elements, corresponding multiplexers, digital control circuitry and buffers. All of the active circuitry fits into a size of 1.5-mm diameter donut area. Placement of receive and transmit electronics and the digital control circuitry are also shown in the picture. (Right) Micrograph of the same IC after monolithic CMUT array fabrication. The dual-ring CMUT array has a 1.4-mm diameter and includes 56 Tx and 48 Rx elements.

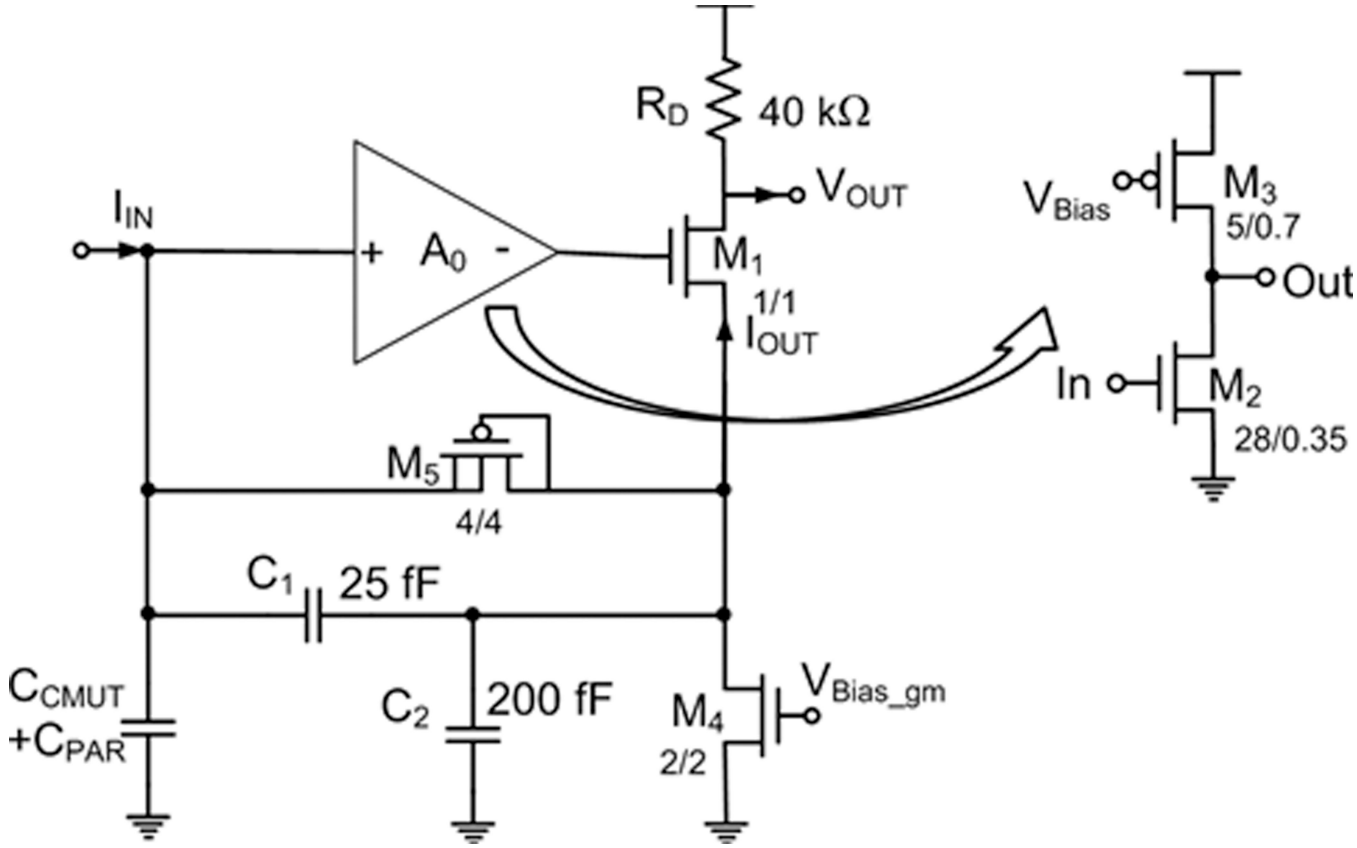

Fig. 4.

(Left) Schematic of the implemented capacitive-feedback TIA. (Right) The core amplifier

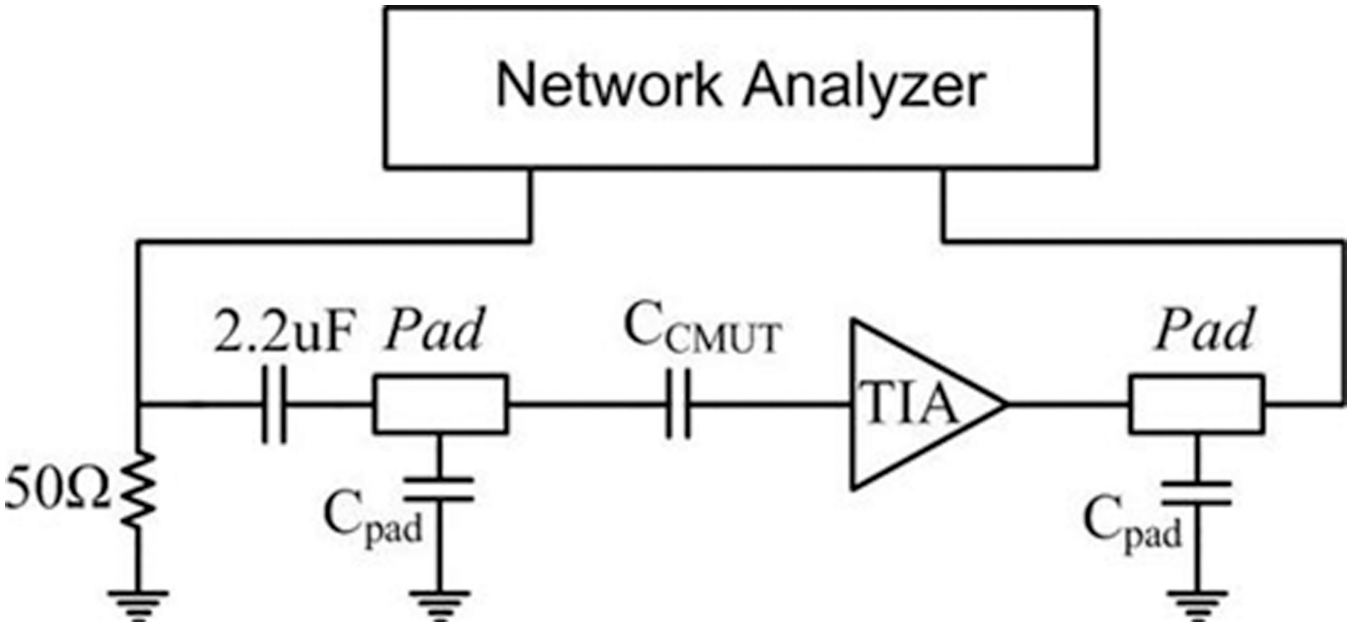

Fig. 5.
Setup for testing the TIA transimpedance characteristics [18].

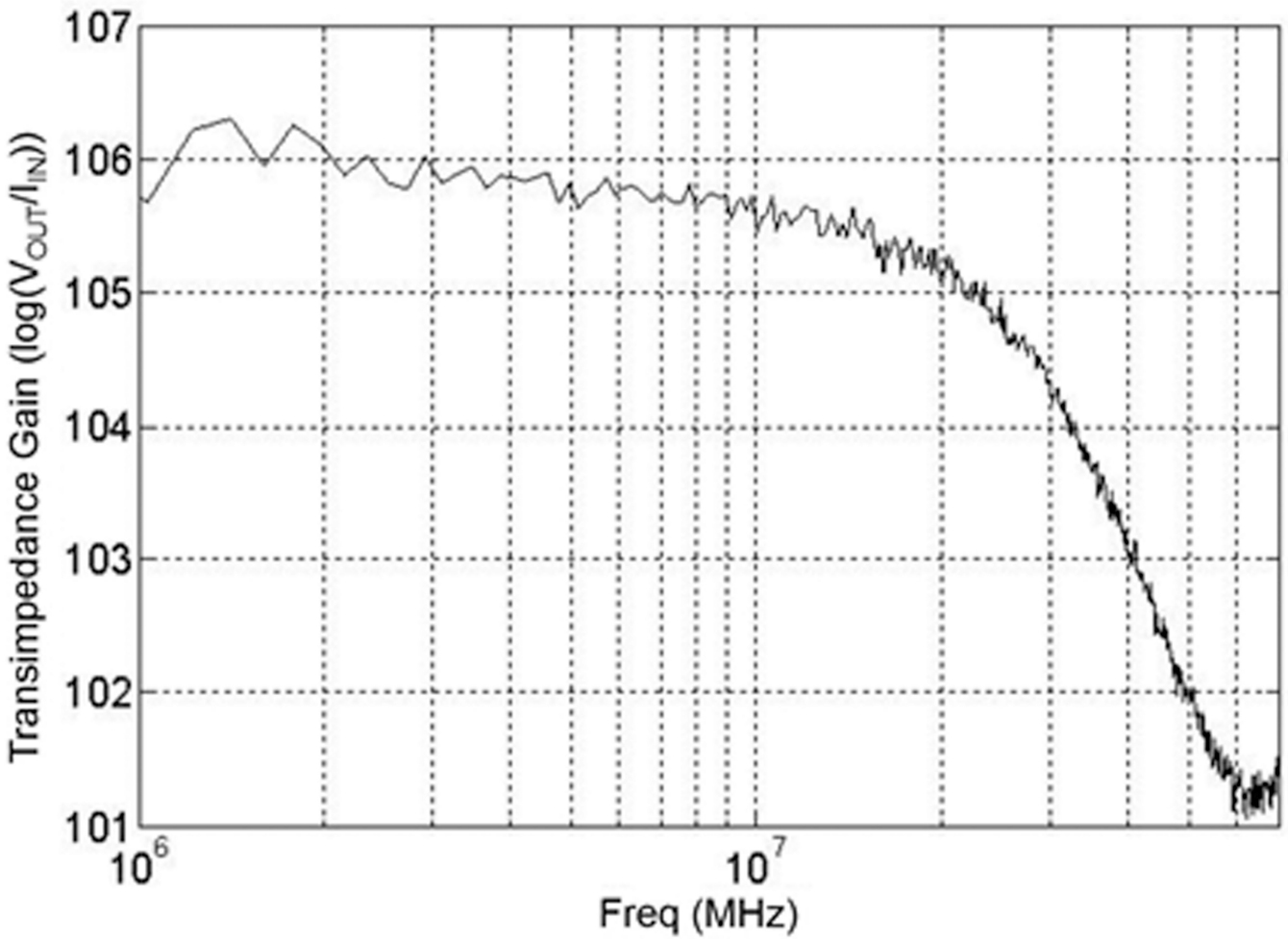

Fig. 6.

The measured transimpedance gain of the capacitive-feedback TIA show a 200-kΩ gain and 40-MHz bandwidth.

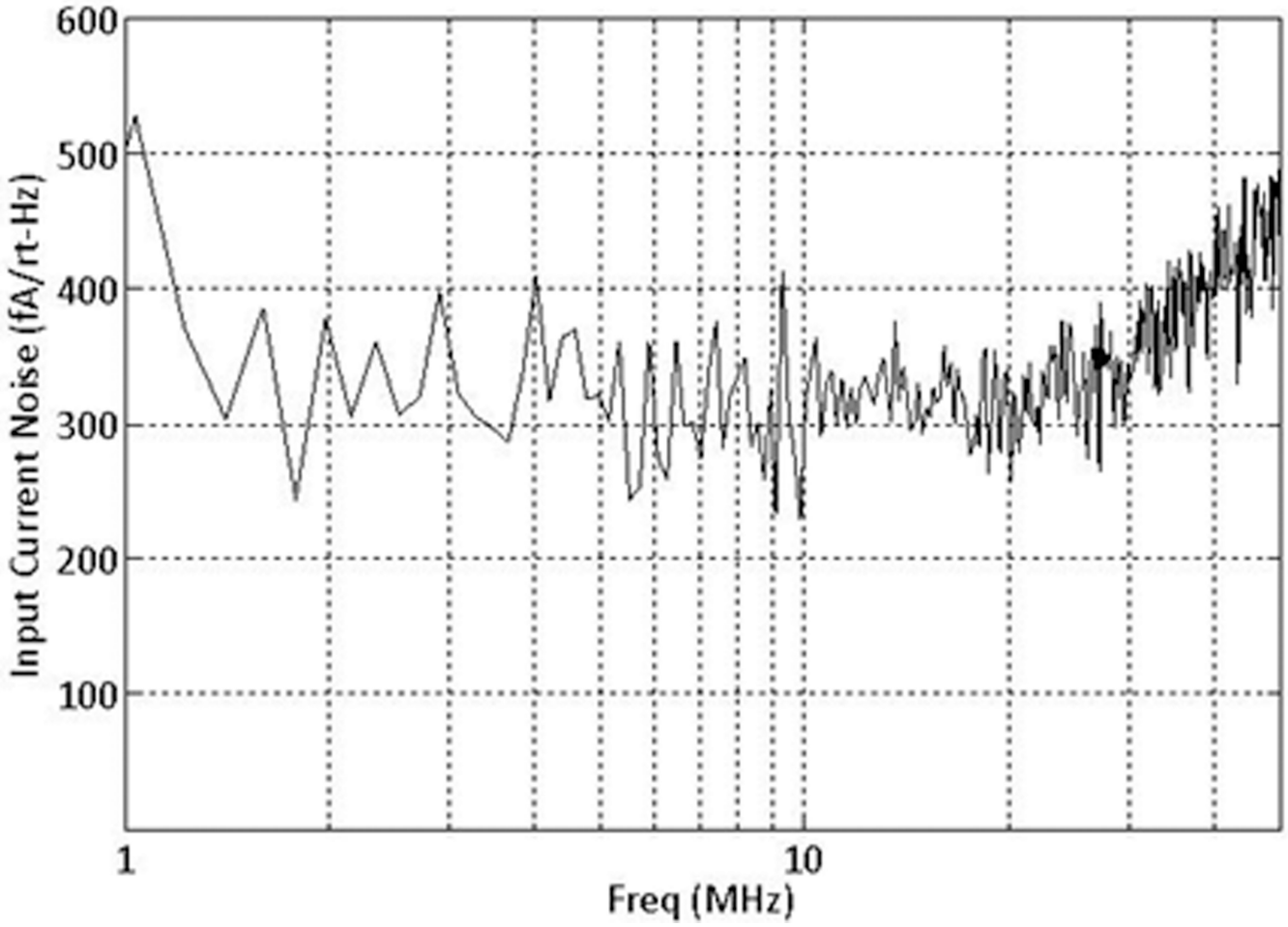

Fig. 7.

The measured input referred spectral density of the current noise of the capacitive-feedback TIA that is monolithically integrated to a forward-looking CMUT element.

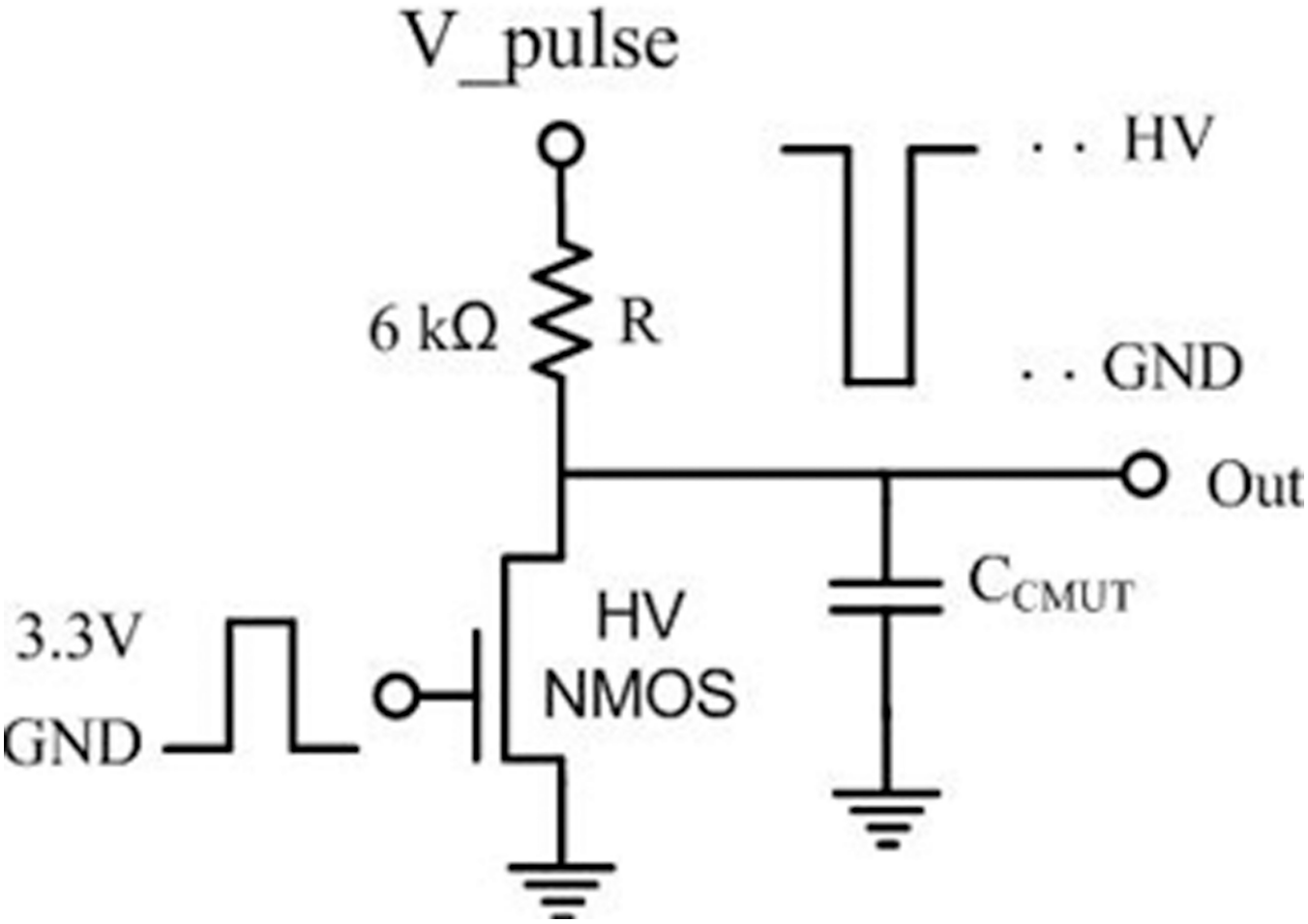

Fig. 8.

Pulser element that is capable of generating 25-V pulses as narrow as 2-ns with the 90-fF CMUT loading in a CMUT-on-CMOS implementation.

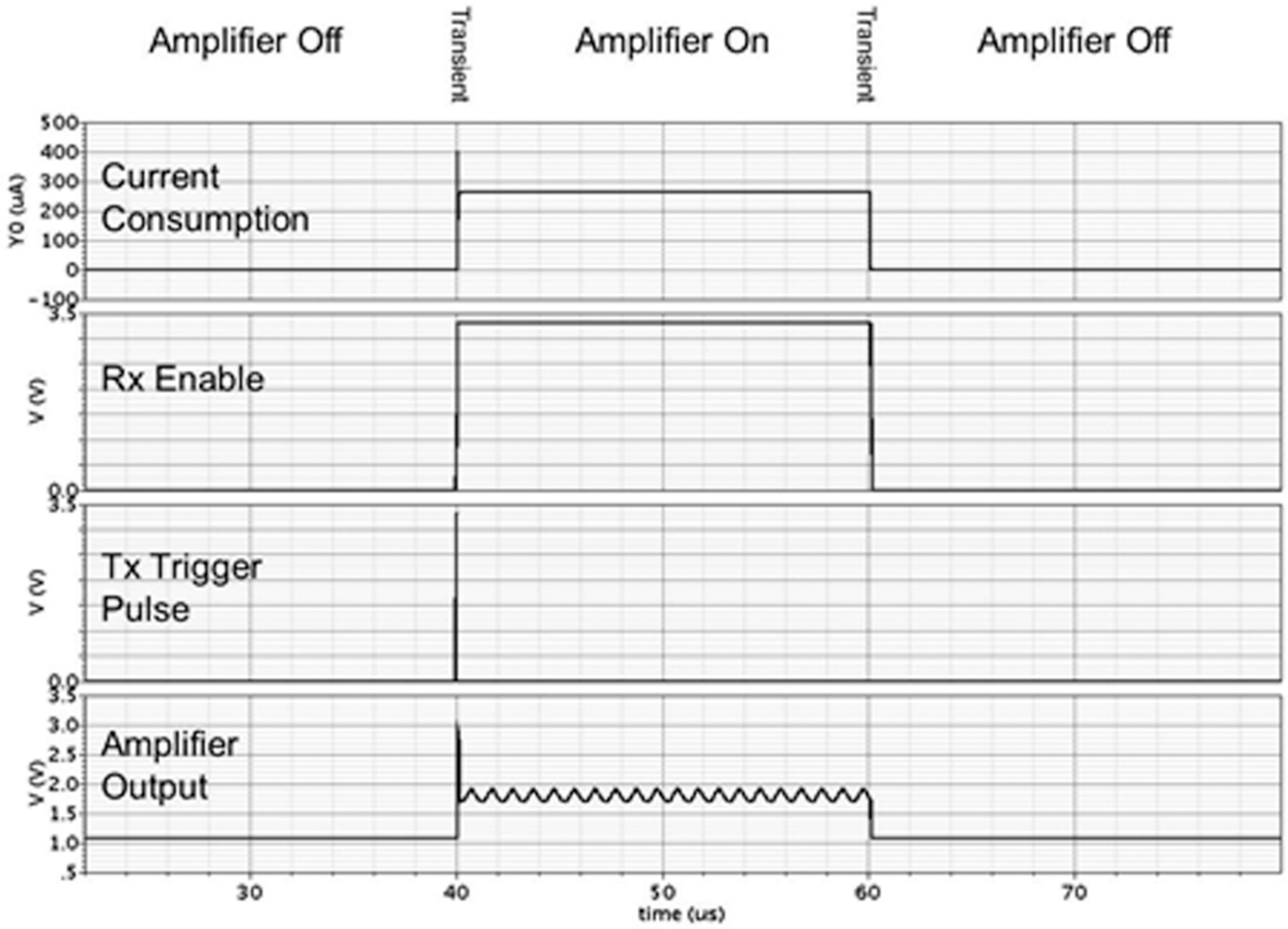

Fig. 9.

Circuit simulation results with a timing diagram that shows the Rx enable, which powers up the receiver circuitry, Tx trigger signal (delayed *Clk* input) and the amplifier current consumption. Note that the type of the receive amplifier that is used in this timing simulation is the resistive-feedback TIA design.

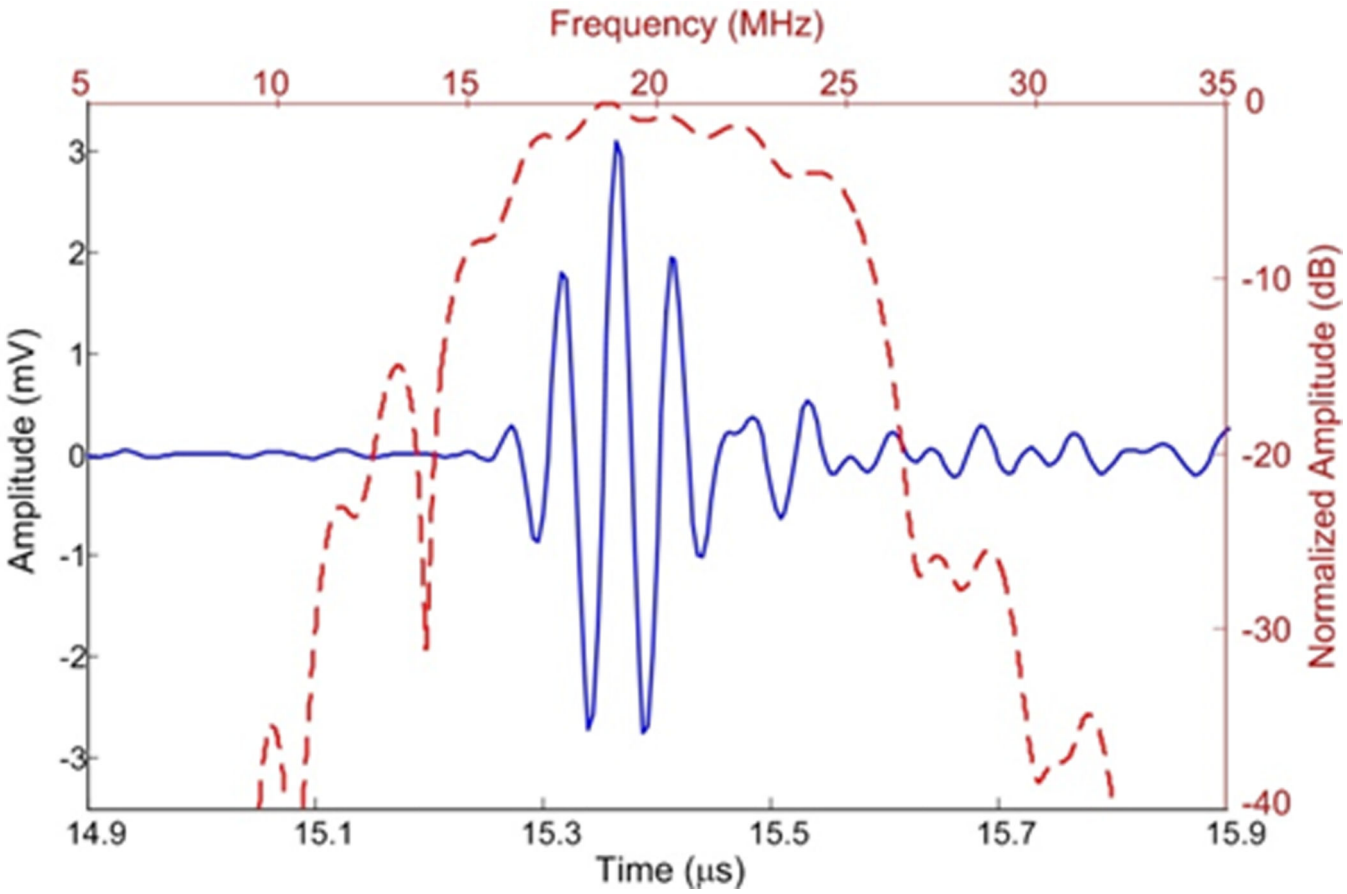

Fig. 10.
Pulse-echo and frequency response of a single A-scan.

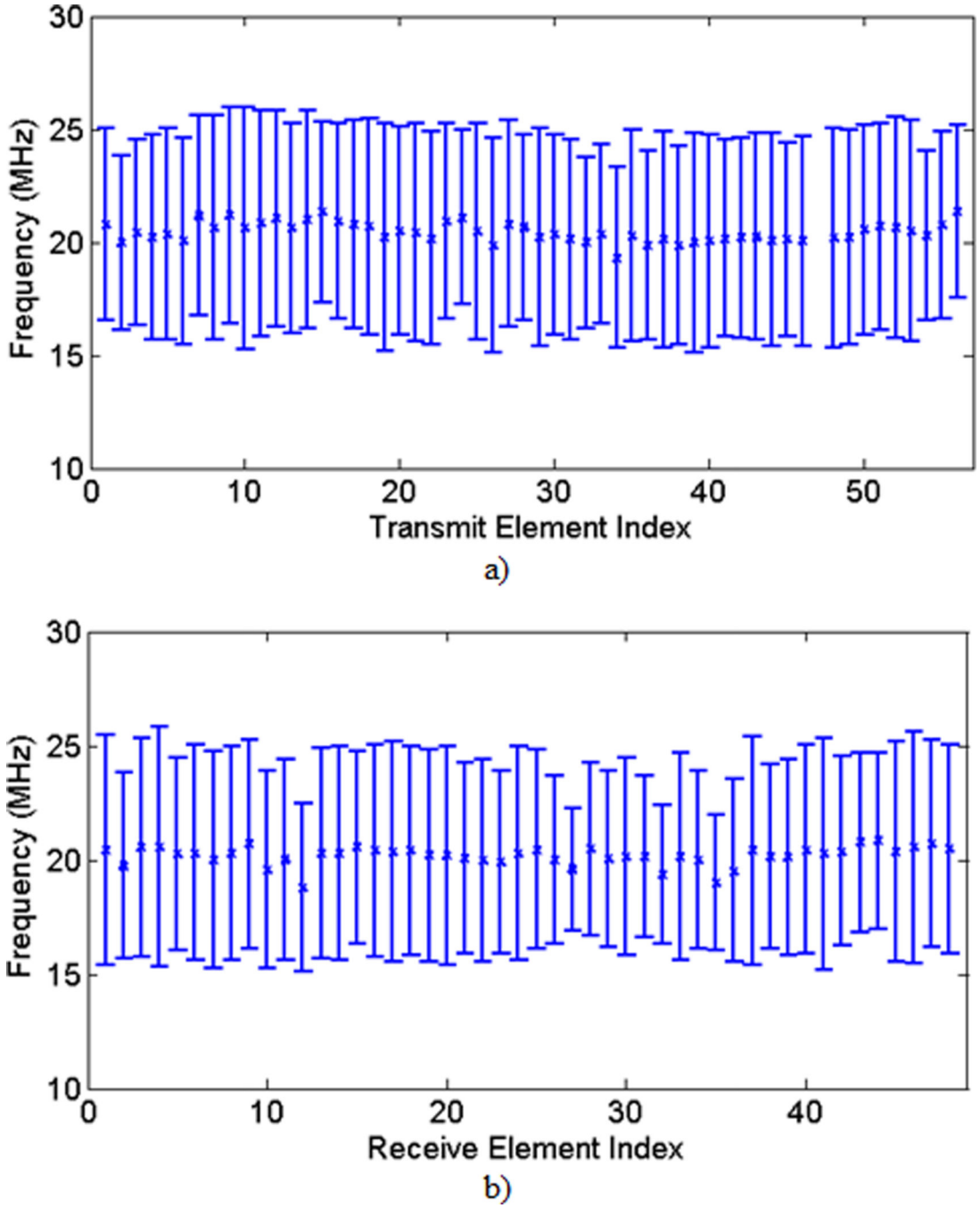

Fig. 11.

The uniformity of the center frequency and 6-dB bandwidth across a) the transmit and b) the receive elements.

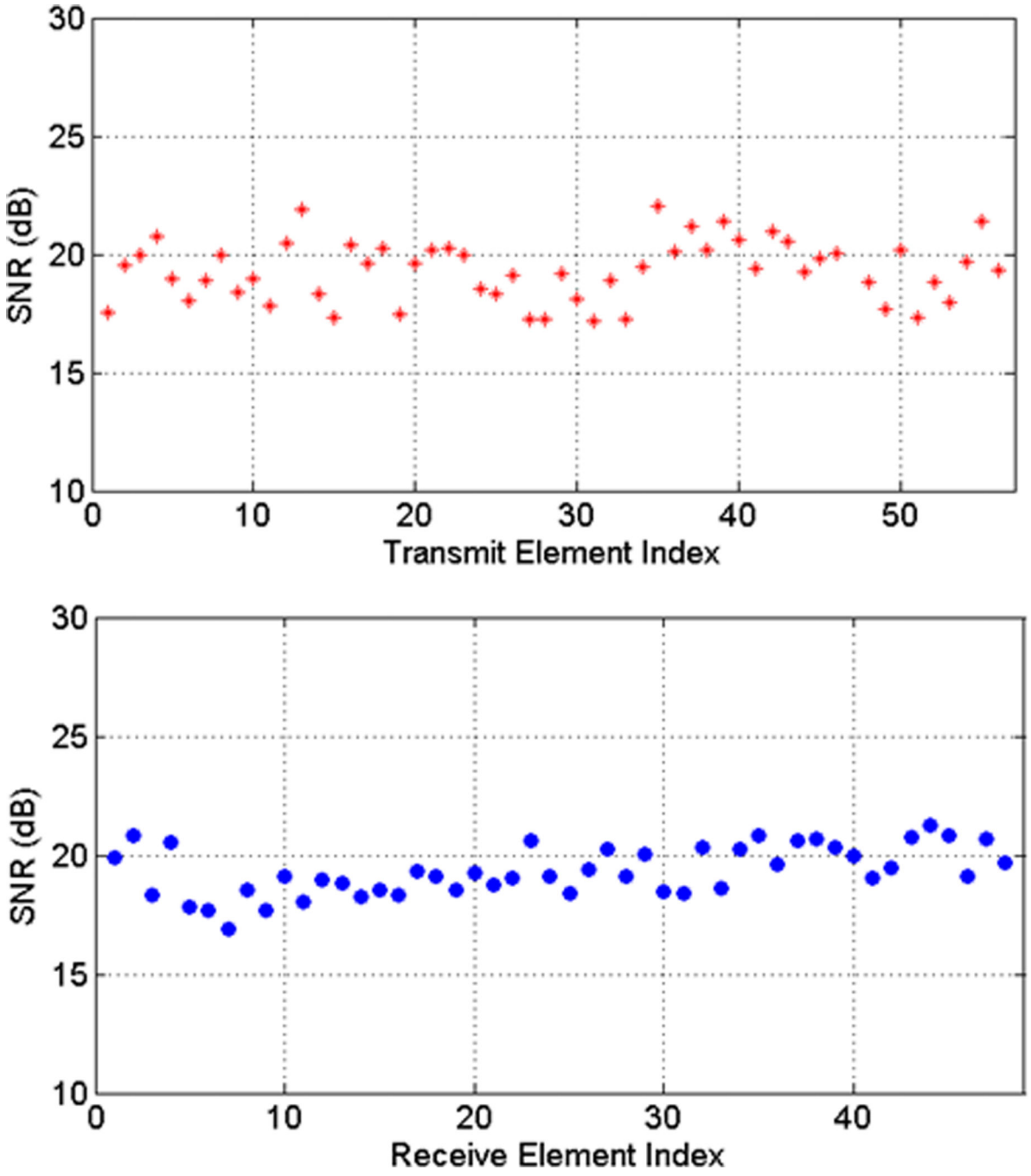

Fig. 12.
Pulse-echo SNR distribution over transmit (top) and receive (bottom) array.

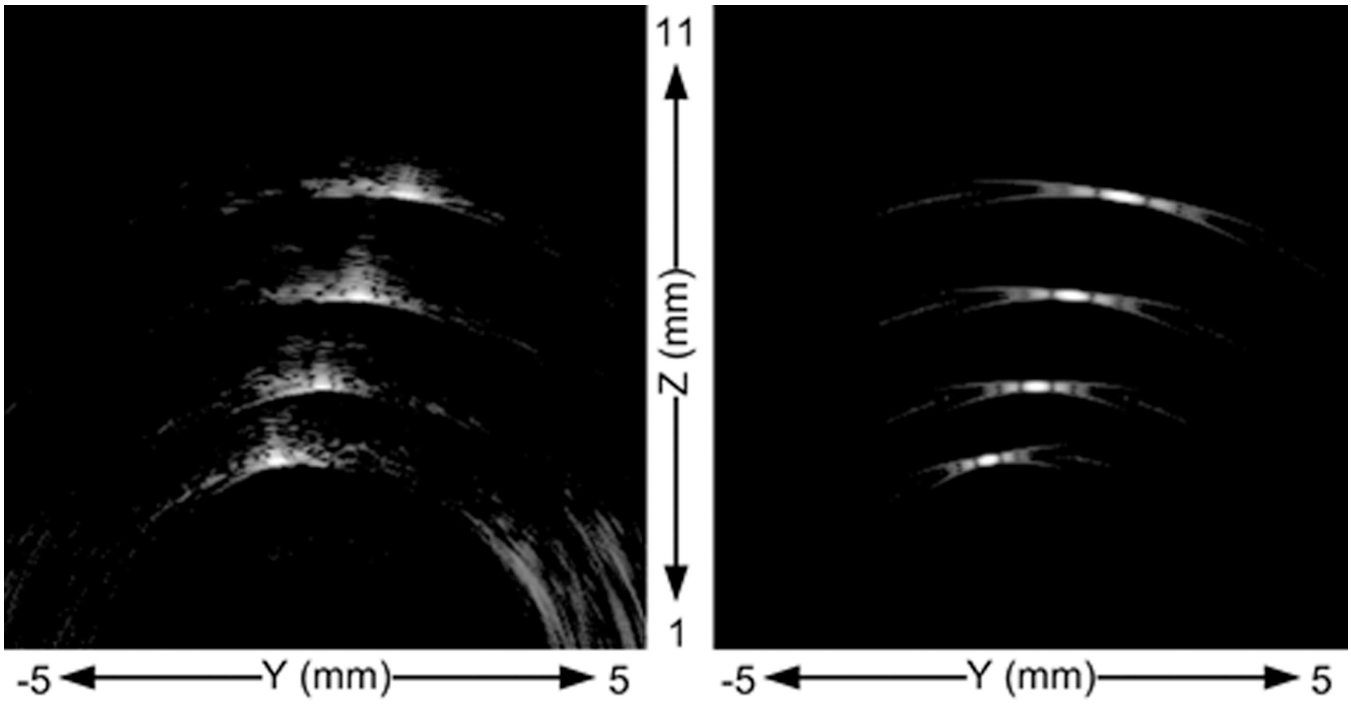

Fig. 13.

B-scan image of the wire phantom on yz plane using experimental RF data (left) and the corresponding simulated PSF (right). The display dynamic range is 40 dB.

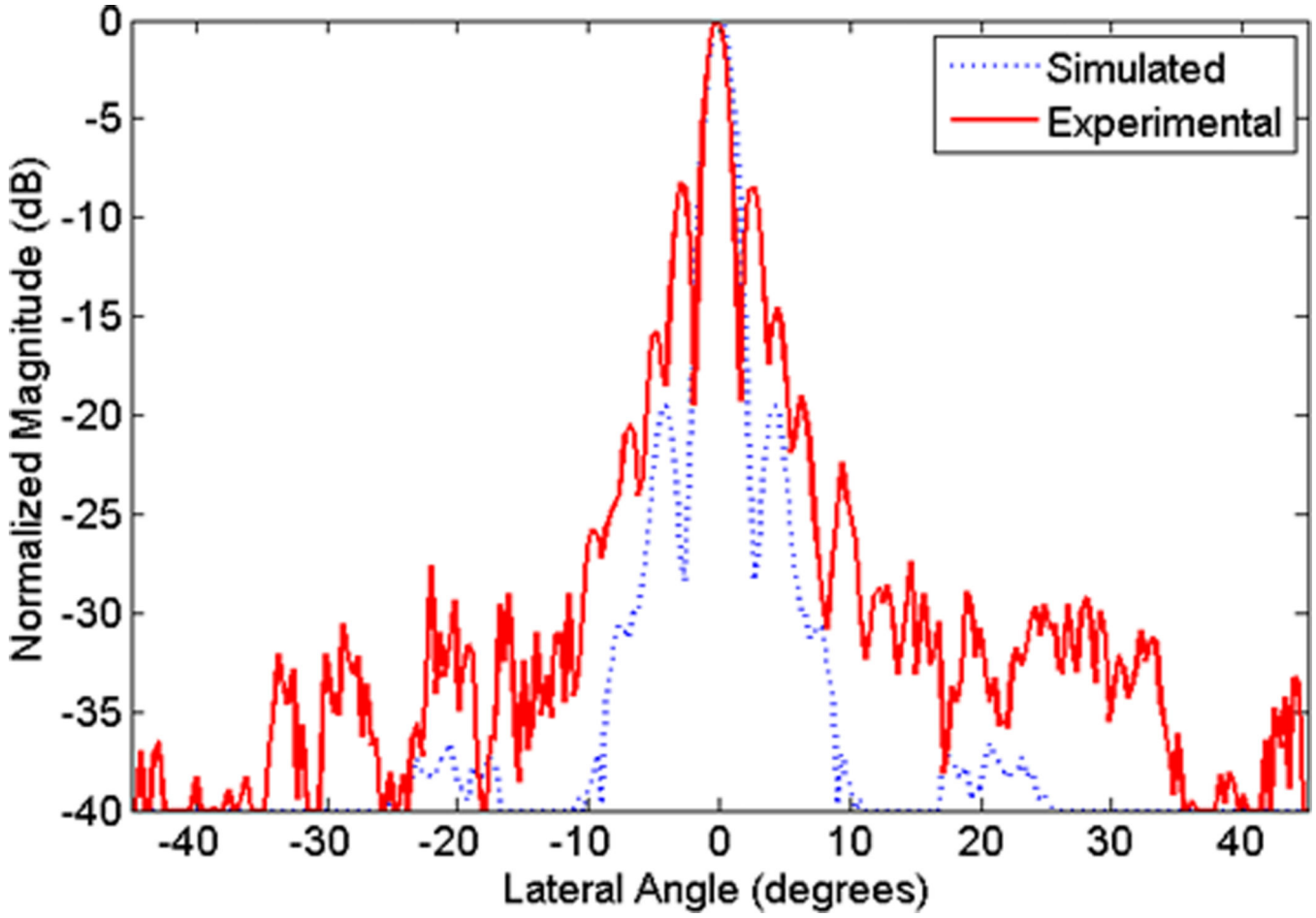

Fig. 14.
1-D comparison of experimental and simulated lateral PSF of the 2nd wire target.

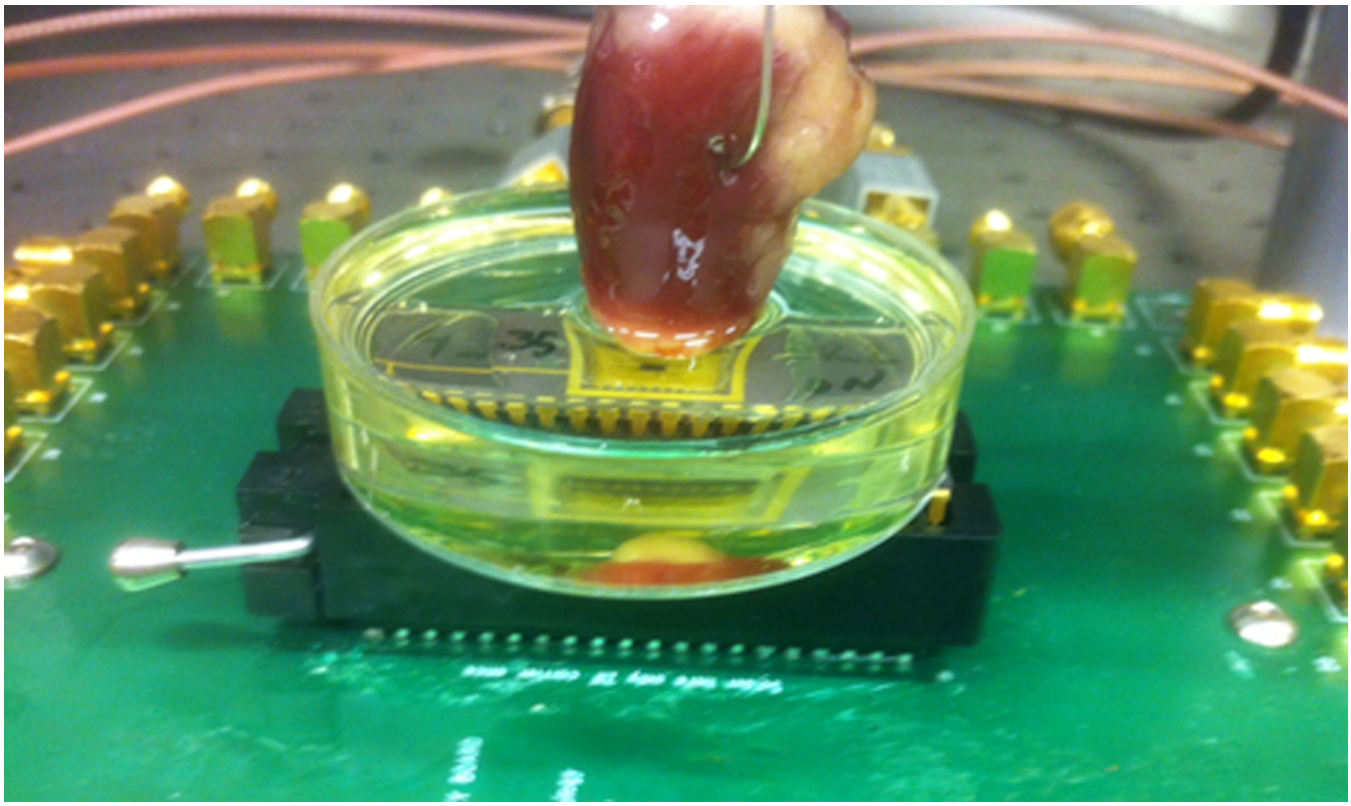

Fig. 15.
Experimental setup of wire-bonded CMUT array in a chip holder combined with a modified Petri dish for imaging chicken heart phantom.

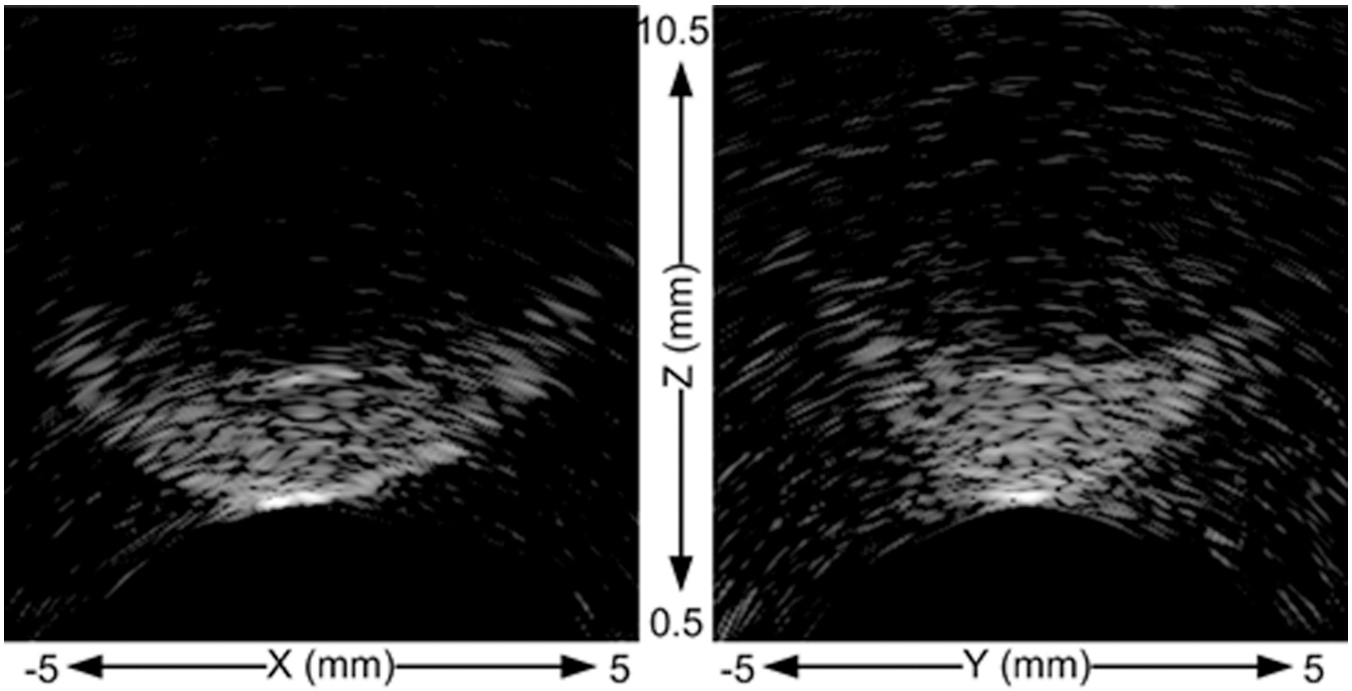

Fig. 16.

2-D Cross-sectional images of the chicken heart phantom in xz (left) and yz (right) plane. The display dynamic range is 40 dB.

TABLE I

Fabricated CMUT Array Parameteres

Number of Elements	56 Tx − 48 Rx
Outer Diameter, *mm*	1.4
Center Frequency, MHz	20
Element Size, μm^2	70 × 70
Membrane size, μ*m*	25 × 25
Element Pitch, μ*m*	74
Number of membranes per element	4
Insulation Layer Thickness, μ*m*	0.21
Total Membrane Thickness, μ*m*	2.3
Gap Thickness, μ*m*	0.12
Electrode Coverage, %	64

TABLE II

Measured Characteristics of the Designed Receive TIA Amplifier

Technology	0.35 μm CMOS
Power Supply	3.3 V
Power Consumption	0.8 mW
Area	$25 \times 55\ \mu m^2$
Transimpedance Gain	200 kΩ
Bandwidth	40 MBz
Dynamic Range	50 dB
Input Referred Noise @ 20 MHz	310 fA/√Hz

TABLE III

Quantitative Experimental Results

	Experimental	Simulated
Axial Resolution, μ*m*	92	84
Lateral Resolution, μ*m* (2nd wire)	251	225
Average Image SNR, *dB*	43	-
Maximum Image SNR, *dB* (closest wire)	48	-