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Comparison of resistive switching characteristics using copper and aluminum electrodes on GeO_x/W cross-point memories

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Abstract

Comparison of resistive switching memory characteristics using copper (Cu) and aluminum (Al) electrodes on GeO_x/W cross-points has been reported under low current compliances (CCs) of 1 nA to 50 μA. The cross-point memory devices are observed by high-resolution transmission electron microscopy (HRTEM). Improved memory characteristics are observed for the Cu/GeO_x/W structures as compared to the Al/GeO_x/W cross-points owing to AlO_x formation at the Al/GeO_x interface. The RESET current increases with the increase of the CCs varying from 1 nA to 50 μA for the Cu electrode devices, while the RESET current is high (>1 mA) and independent of CCs varying from 1 nA to 500 μA for the Al electrode devices. An extra formation voltage is needed for the Al/GeO_x/W devices, while a low operation voltage of ±2 V is needed for the Cu/GeO_x/W cross-point devices. Repeatable bipolar resistive switching characteristics of the Cu/GeO_x/W cross-point memory devices are observed with CC varying from 1 nA to 50 μA, and unipolar resistive switching is observed with CC >100 μA. High resistance ratios of 10^2 to 10^4 for the bipolar mode (CCs of 1 nA to 50 μA) and approximately 10^8 for the unipolar mode are obtained for the Cu/GeO_x/W cross-points. In addition, repeatable switching cycles and data retention of 10^3 s are observed under a low current of 1 nA for future low-power, high-density, nonvolatile, nanoscale memory applications.

Keywords: Memory; Resistive switches; GeO_x; Copper; Aluminum; Solid electrolyte

Background

Recently, resistive switching memory devices involving different materials such as $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) [1], NiO_x [2], $SrTiO_3$ [3,4], TaO_x [5-8], HfO_x [9,10], TiO_2 [11], ZrO_2 [12], $Na_{0.5}Bi_{0.5}TiO_3$ [13], and AlO_x [14-16] are widely reported to replace conventional flash memory. On the other hand, conductive bridging resistive random access memory (CBRAM) involving the migration of cations (Ag^+ or Cu^{z+}, $z = 1, 2$) in solid electrolytes such as Ge_xSe_{1-x} [17-20], GeS_2 [21], Ta_2O_5 [22], ZrO_2 [23-25], TiO_x/ZrO_2 [26], $GeSe_x/TaO_x$ [27], HfO_2 [28], $CuTe/Al_2O_3$ [29], Ti/TaO_x [30], ZnO [31], SiO_2 [32], and GeO_x [33] is also reported. In this case, the mobile Ag^+ or Cu^{z+} ions play an important role in the formation and dissolution of metallic filament in the solid electrolytes. Although memory characteristics using different solid electrolytes have been reported, GeO_x-based CBRAM devices in the cross-point structure are also a beneficial choice. Memory characteristics using GeO_x film in a Cu/GeO_x/Al structure were first reported by Beynon and El-Samanoudy in 1987 [34]. Their extended work was published in 1991 using a Cu/GeO_x/Au structure [35]. Resistive switching memory using GeO_x material in different structures such as Ni/GeO_x/$SrTiO_x$/TaN [36] and Pt/$SiGeO_x$/SiGeON/TiN [37] has also been reported for future nonvolatile memory applications. On one hand, Schindler et al. [38] has reported a GeO_x layer for the Cu (Ag) diffusion barrier layer in a Cu (Ag)/GeSe/Pt structure. On the other hand, cross-point structures using different switching materials have been reported by several groups [6,39-42] to have a high-density memory for future applications. It is known that resistive switching memories in cross-point architecture possess several attractive features and have attracted considerable attention in recent years because of the multilayer stacking of three-dimensional (3D) architecture, simplicity of their manufacturing, and the simplest interconnection configuration. Furthermore, resistive switching memory devices

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with low-current operation (<100 μA) are also an important issue. To mitigate those specifications, a cross-point memory using a Cu/GeO_x/W structure has been compared with that using an Al/GeO_x/W structure for the first time.

In this study, the memory characteristics using Cu and Al top electrodes (TEs) on GeO_x/W cross-points have been compared. The cross-point structures were observed by high-resolution transmission electron microscopy (HRTEM). The Cu/GeO_x/W cross-point memory devices have shown improved bipolar resistive switching characteristics as compared to the Al/GeO_x/W cross-points, owing to the AlO_x layer formation at the Al/GeO_x interface. The RESET current deceases with the decrease of current compliances (CCs) from 50 μA to 1 nA for the Cu/GeO_x/W devices, while the RESET current was independent (>1 mA) of CC in the range of 500 μA to 1 nA for the Al/GeO_x/W cross-point memories. High resistance ratios of 10^2 to 10^4 under bipolar and approximately 10^8 under unipolar modes are observed for the Cu/GeO_x/W cross-point memory devices. Repeatable switching cycles and data retention of approximately 10^3 s under a low CC of 1 nA were obtained for the Cu TE devices, which are very useful for low-power operation of high-density nonvolatile nanoscale memory applications.

Methods

A silicon dioxide (SiO_2) layer with a thickness of approximately 200 nm was grown by wet oxidation process on 4-in. p-Si wafers after the Radio Corporation of America (RCA) cleaning method. The horizontal furnace consisted of a quartz tube on a carrier made of quartz glass in the middle; the wafers were placed in the quartz tube. The temperature of the furnace was maintained at 900°C during the oxidation process. To avoid cracks or warping, the wafers were placed inside the furnace at 600°C. The furnace was heated slowly with a ramp rate of +13°C/min. During the oxidation process, hydrogen and oxygen gases were used with flow rates of 4 and 2.5 standard liters per minute (SLM), respectively. The oxidation time was 90 min. Then, W metal as a bottom electrode (BE) with a thickness of approximately 200 nm was deposited by radio frequency (RF) sputtering on SiO_2/Si wafers. The deposition parameters of the W layer were shown in Table 1. Then, the BE was defined and patterned by standard photolithography and wet chemical etching processes. The following parameters were used for the photolithography process. The wafer is initially heated at 120°C for 10 min in the oven to drive off any moisture that may be present on the wafer surface. A liquid 'adhesion promoter' such as hexamethyldisilazane or HMDS was applied to promote adhesion of the photoresist to the wafer. A spin coater was used to coat the HMDS on the wafer. The spin coating was run at initially 3,000 rpm for 10 s and then 5,000 rpm for 20 s. Following the same process, an AZ6112 positive photoresist (AZ Electronic Materials, Branchburg, NJ, USA) was spun on the wafer to create the pattern. The photoresist-coated wafer was then prebaked to drive off excess photoresist solvent at 90°C for 2 min. After prebaking, the sample was placed on a vacuum substrate of an optical lithography system (ABM Sales Service, San Jose, CA, USA). Then, mask 1 was placed over the sample. The photoresist was exposed to ultraviolet (UV) light for 4 s. Before developing, a postexposure bake (PEB) was performed at 90°C for 1 min to reduce the standing wave phenomena caused by the destructive and constructive interference patterns of the incident light. The wafer was immersed into the AZ330 developer (AZ Electronic Materials) for 15 s to remove the exposed photoresist and then rinsed by deionized (DI) water. The resulting wafer was then 'hard-baked' to harden the final resist at 120°C for 15 min. The wet chemical etching process was used to etch the uncovered W metal layer and form the W BE. A commercially available tungsten etchant (Sigma-Aldrich) was used, and the wafer was dipped into the solution for 2 to 3 min. The same photolithography process was repeated to design the 1×1 to 10×10 arrays. To pattern the switching material and TE, mask 2 was placed over the samples using a mask aligner. After the masking process, the GeO_x switching material with a thickness of approximately 10 nm was deposited by the same RF sputtering system. Following this, Cu as a TE with a thickness of approximately 40 nm was deposited using a thermal evaporator. Then, the aluminum (Al) layer with a thickness of approximately 160 nm was deposited *in situ* by the thermal evaporator. The deposition conditions of GeO_x, Cu, and Al were shown in Table 1. Finally, a lift-off process was performed to get the final Al/Cu/GeO_x/W (device S1) memory device, i.e., called Cu/GeO_x/W structure hereafter. Similarly, an Al/GeO_x/W (device S2) memory device without a Cu layer was also prepared for comparison. Table 2 shows the structures of the fabricated memory devices. A schematic illustration of the fabricated GeO_x-based cross-point memory device is shown in Figure 1a. The GeO_x solid electrolyte is sandwiched between Cu or Al TE and W BE. An optical micrograph (OM) of 4×5

Table 1 Deposition parameters of different materials

Materials	Target/granules	Methods	Vacuum (Torr)	Ar gas (SCCM)	Power (Watt)	Deposition rate
W	W target	RF sputtering	1×10^{-5}	25	150	12 nm/min
GeO_x	Ge target	RF sputtering	2×10^{-5}	25	50	5.3 nm/min
Cu	Cu granules	Thermal evaporator	8×10^{-6}	-	-	2-3 Å/s
Al	Al granules	Thermal evaporator	8×10^{-6}	-	-	2-3 Å/s

Table 2 Structures of the cross-point resistive switching memory devices

Devices	BE ~ 200 nm	Switching layer (10 nm)	TE	
			Cu ~ 40 nm	Al ~ 160 nm
S1	W	GeO_x	√	√
S2	W	GeO_x	×	√

cross-points is shown clearly in Figure 1b. All cross-points are clearly observed.

The cross-point structure and thicknesses of all materials were evaluated from a HRTEM image. HRTEM was carried out using a FEI Tecnai (Hillsboro, OR, USA) G2 F-20 field emission system. Memory characteristics were measured using an HP4156C semiconductor parameter analyzer (Agilent Technologies, Santa Clara, CA, USA). For electrical measurements, the bias was applied to the TE while the W BE was grounded.

Results and discussion

Figure 2 shows the TEM image of the Cu/GeO_x/W structure (device S1). The area of the cross-point is approximately 1.2 × 1.2 μm^2 (Figure 2a). Films deposited layer by layer are clearly observed in the HRTEM image, as shown in Figure 2b. The thickness of the SiO_2 layer is approximately 200 nm. The thicknesses of W, Cu, and Al metals are approximately 180, 38, and 160 nm, respectively. The thickness of the GeO_x solid electrolyte is approximately 8 nm, as shown in Figure 2c. The formation of a thin (2 to 3 nm) WO_x layer is observed at the GeO_x/W interface. The HRTEM image of the Al/GeO_x/W cross-point memory devices is also shown in Figure 3a. It is interesting to note that the AlO_x layer with a thickness of approximately 5 nm at the Al/GeO_x interface is observed (Figure 3b). The Gibbs free energies of the Al_2O_3, GeO_2, CuO, and Cu_2O films are −1,582, −518.8, −129.7, and −149 kJ/mol at 300 K, respectively [43]. Therefore, the formation of AlO_x at the Al/GeO_x interface will be the easiest as compared to those of other materials. For example, the AlO_x layer at the Al/Ta_2O_5 interface was also observed even though the Al layer was deposited on a Ta_2O_5 film (not shown here). This suggests that Al is a metal reactive with oxygen, and it is hard to control the reaction at the Al/oxide interface. However, the AlO_x film will have more defects, which may have resistive switching phenomena. The resistive switching memory characteristics using Cu and Al

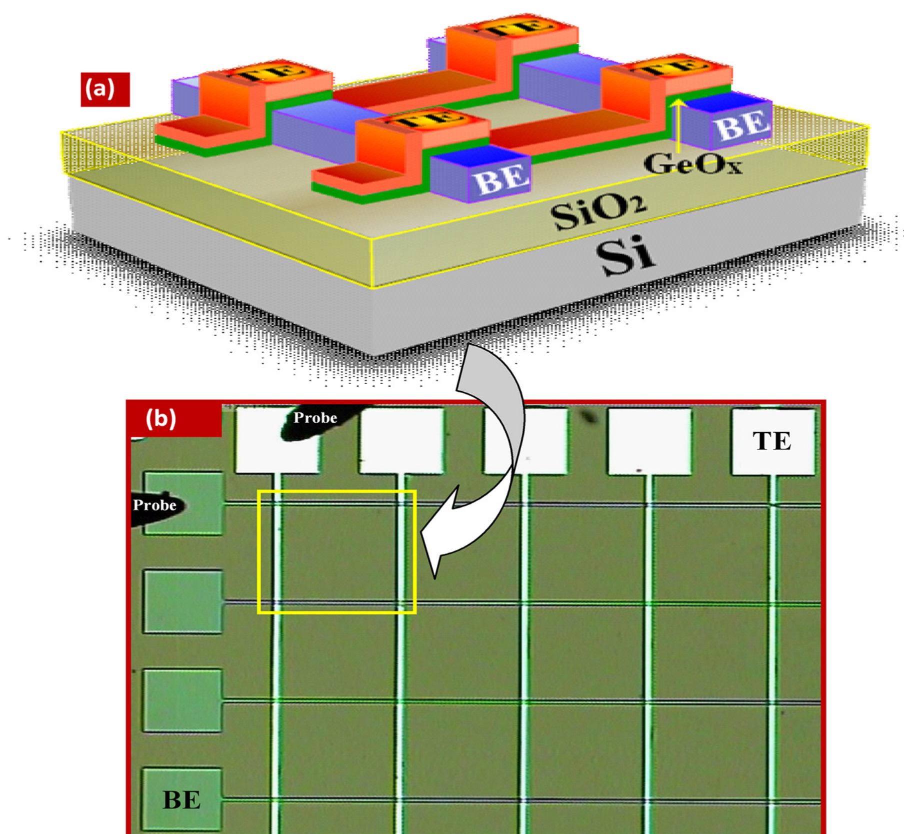

Figure 1 Schematic illustration and optical image of the Cu/GeO_x/W cross-point memories. (a) Schematic illustration and **(b)** optical image of our fabricated cross-point memory devices. Active area of the cross-point memory is approximately 1 × 1 μm^2. The thickness of the GeO_x solid electrolyte film is approximately 10 nm.

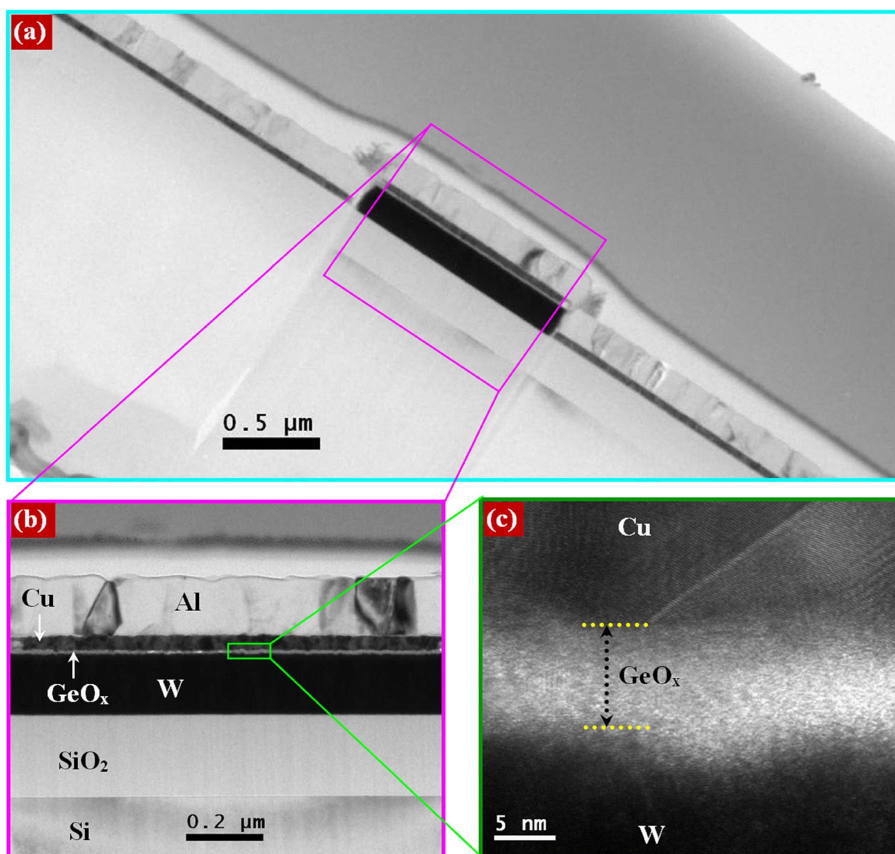

Figure 2 TEM images of the cross-point memories using Cu electrode. (a) TEM image of a Cu/GeO_x/W cross-point memory. HRTEM image with scale bars of **(b)** 0.2 μm and **(c)** 5 nm. Films deposited layer by layer are clearly observed by HRTEM imaging.

top electrodes on GeO_x/W cross-point memories are discussed below.

Typical *I-V* hysteresis with CCs of 1 nA to 50 μA when using the Cu/GeO_x/W cross-point memory is shown in Figure 4a. Initially, all memory devices were in high-resistance state (HRS), and positive sweeping voltage was applied. A slightly high voltage of approximately 1 V is necessary to switch the memory device from HRS to low-resistance state (LRS) under a CC of 500 nA, which is shown in the first cycle. This will form a Cu filament in the GeO_x solid electrolyte. After the formation process, the device shows normal bipolar resistive switching behavior. The memory device can be operated at a low CC of 1 nA, and a Cu cylindrical-type filament can be expected to form because the currents at HRS are the

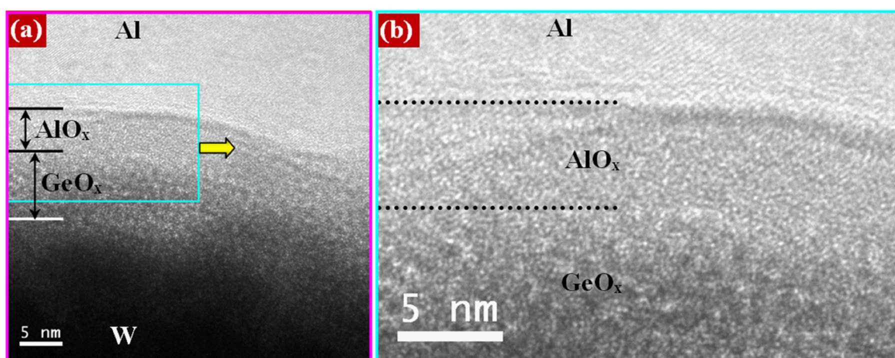

Figure 3 TEM images of the device using Al electrode. (a) HRTEM image of an Al/GeO_x/W cross-point memory. **(b)** Formation of an AlO_x film with a thickness of approximately 5 nm at the Al/GeO_x interface is observed.

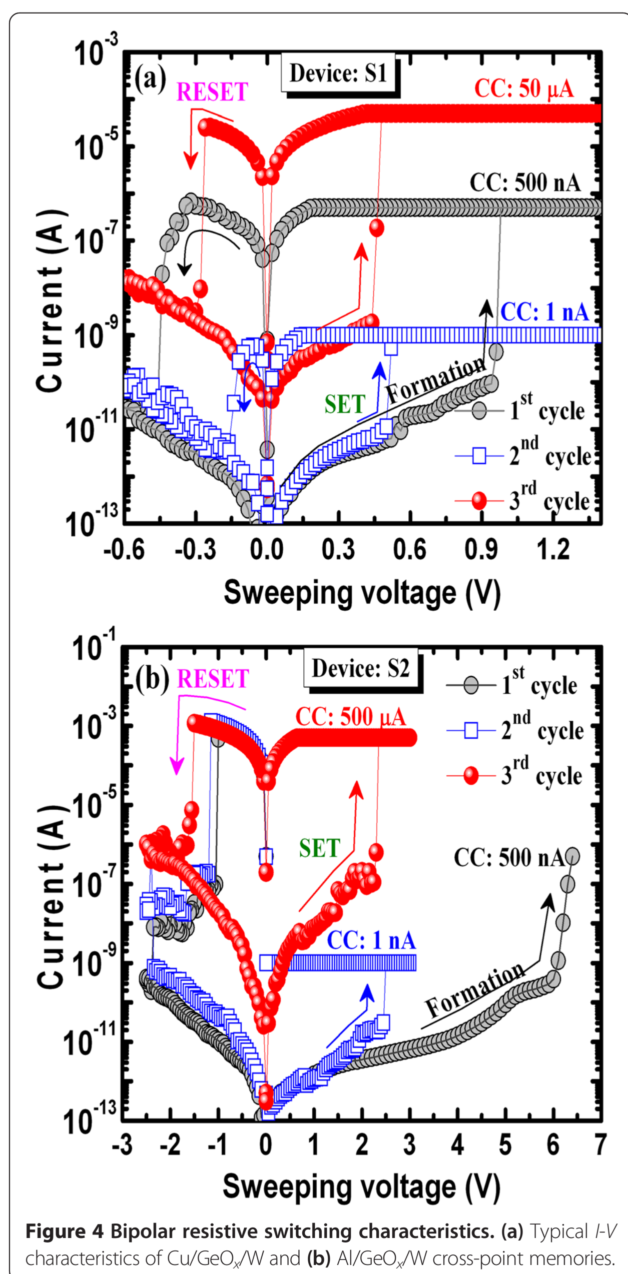

Figure 4 Bipolar resistive switching characteristics. (a) Typical *I-V* characteristics of Cu/GeO$_x$/W and **(b)** Al/GeO$_x$/W cross-point memories.

same after RESET operation for CCs of 1 to 500 nA [33]. A current change at HRS (approximately 1 pA to 1 nA at 0.1 V) is observed at a CC of 50 μA. At a higher CC of 50 μA, the filament diameter increased and the shape of the filament will be conical type [27]. This implies that the Cu filament remains at the GeO$_x$/W interface after RESET operation. On the other hand, a high formation voltage of approximately 6 V is needed for the Al TE, as shown in the first cycle (Figure 4b). In this case, the memory device can be operated at a low CC of 1 nA, but a high RESET current of >1 mA is needed to rupture the conducting filaments. A current change at HRS is observed at a high CC of 500 μA owing to the remaining filament even with a higher RESET current of >1 mA. *I-V* measurements for pristine devices S1 and S2 are shown in Figure 5a,b. The average leakage currents at 0.1 V of the S2 devices are higher than those of the S1 devices (4.4 pA versus 0.4 pA) owing to the formation of the approximately 5-nm-thick AlO$_x$ layer at the Al/GeO$_x$ interface. The formation voltages for the S1 devices are 0.8 to 1.4 V, while they are 3 to 9 V for the S2 devices, which is due to the thicker switching material for the Al TE than the Cu TE (8 + 5 = 13 nm versus 8 nm). This is also beneficial to the Cu TE (device S1) than the Al TE (device S2).

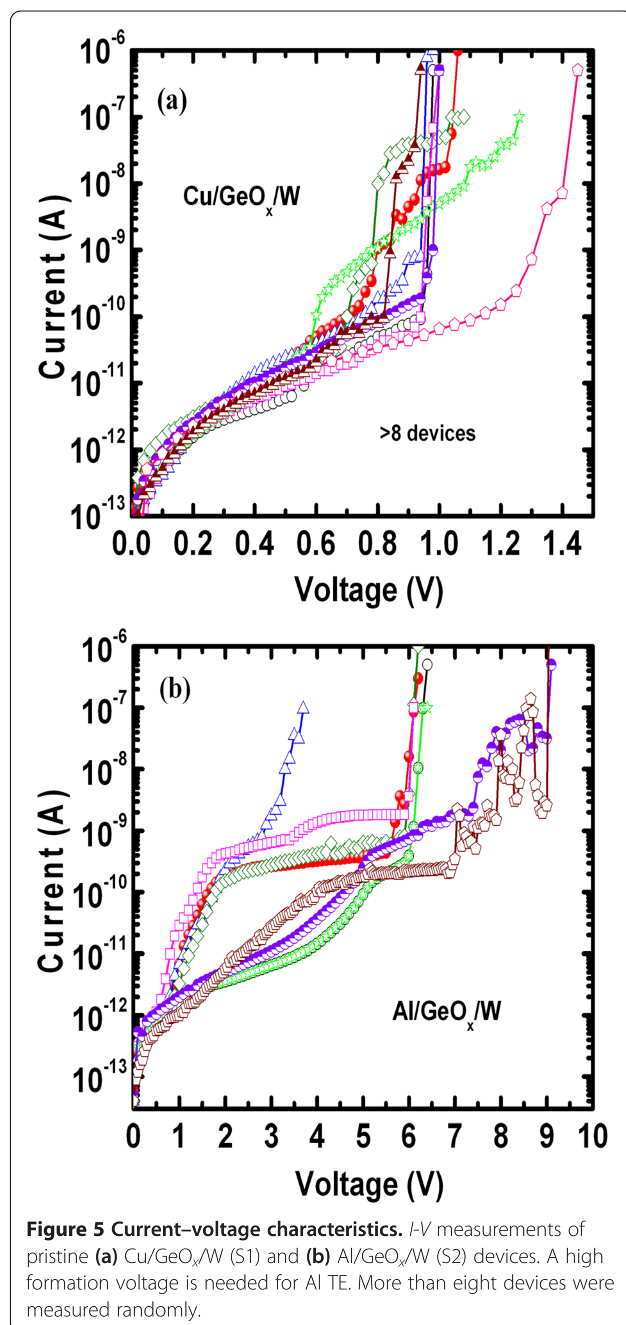

Figure 5 Current–voltage characteristics. *I-V* measurements of pristine **(a)** Cu/GeO$_x$/W (S1) and **(b)** Al/GeO$_x$/W (S2) devices. A high formation voltage is needed for Al TE. More than eight devices were measured randomly.

Further, the RESET current is independent of CCs from 1 nA to 1 mA for the Al/GeO_x/W cross-point memory device, as shown in Figure 6. This suggests that the RESET current scalability as well as device scaling is difficult for the Al TE devices, which form larger filament diameter (or many conducting filaments) even at a small CC of 1 nA. This is due to a strong current overshoot effect in the Al/GeO_x/W cross-point memory devices. It is noted that the diameters of the conducting filaments are the same at all CCs from 1 nA to 2 mA, which is due to the defective AlO_x layer at the Al/GeO_x interface or unstable interface. A high RESET current of >20 mA was also reported by Kato et al. using Al TE [44]. Lin et al. [12] also reported a high RESET current for Al_2O_3-based resistive switching memory using a Ti/Al_2O_3/Pt structure. According to several reported results, using Al electrode or Al_2O_3-based resistive memory devices requires higher operation voltages as well as high RESET currents [12,44,45]; however, a few results were reported on low-current operation [6-8,14]. As we can see, the formation voltage of the Al/GeO_x/W device is higher than that of the Cu/GeO_x/W device. It seems that the parasitic capacitance [46] of the Al/GeO_x/W device as well as the current overshoot effect is higher. Even if the SET voltage is lower, the RESET current is still very high or the same with the RESET current of formation. This suggests that the current overshoot effect is not due to the higher operation voltage but to the AlO_x formation at the Al/GeO_x interface or unstable interface. This is a very important difference between these Al and Cu TEs. An excellent scaling of the RESET current is observed for the Cu/GeO_x/W cross-point memory devices with CCs from 1 nA to 50 μA. Furthermore, the RESET current is lower than the SET current, which proves no current overshoot effect even in the 1R configuration or no parasitic effect [46]. The formation and dissolution of Cu nanofilament under SET and RESET are responsible for the switching mechanism of the Cu/GeO_x/W cross-point memory devices. The Cu ions will migrate through the defects into the GeO_x film and start to grow first at the GeO_x/W BE under SET operation by reduction process ($Cu^{z+} + ze^- \rightarrow Cu^o$). The Cu nanofilament will start to dissolve at the Cu/GeO_x interface under RESET operation by oxidation process ($Cu^o \rightarrow Cu^{z+} + ze^-$). In the case of the Al/GeO_x/W cross-point memory, oxygen vacancy filament formation and oxidation are responsible for the switching mechanism. When the applied bias voltage is higher than the SET voltage on the Al TE, the Ge-O bonds will break and O^{2-} ions as negative charge will migrate from the GeO_x layer towards the Al/GeO_x interface, resulting in an oxygen vacancy conducting filament formation. The RESET will occur when the applied negative bias on the Al TE is lower than the RESET voltage and the O^{2-} ions will migrate from the Al/AlO_x interface and oxidize the conducting filament. Due to the defective AlO_x layer formation at the Al/GeO_x interface and Joule heating, uncontrolled oxygen vacancy filament formation and oxidation by O^{2-} ion migration can be assumed under SET and RESET operations, which make reduction of the RESET current as well as scaling of the device difficult. This suggests that the Cu nanofilament diameter can be controlled by external CCs for the Cu/GeO_x/W cross-point memories.

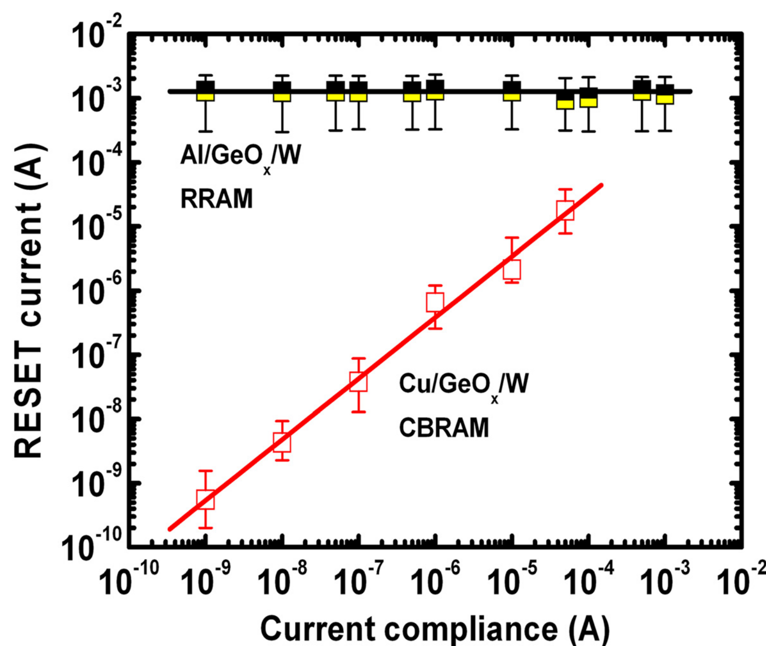

Figure 6 Unipolar resistive switching characteristics. Unipolar resistive switching characteristics of the Cu/GeO_x/W cross-point memory device. A high resistance ratio of $>10^8$ was also obtained using the cross-point architecture.

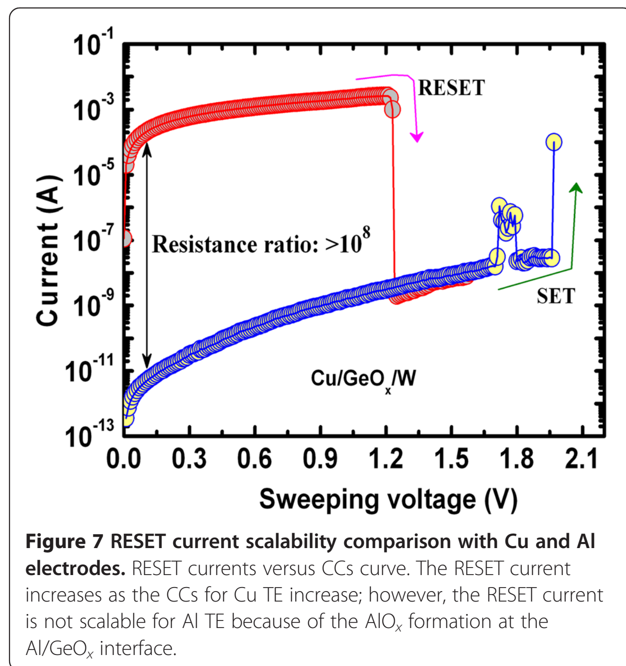

Figure 7 RESET current scalability comparison with Cu and Al electrodes. RESET currents versus CCs curve. The RESET current increases as the CCs for Cu TE increase; however, the RESET current is not scalable for Al TE because of the AlO_x formation at the Al/GeO_x interface.

In addition, unipolar resistive switching characteristics are also observed, as shown in Figure 7. In this case, the Cu filament is formed under SET and the filament is dissolved by Joule heating under RESET. A high resistance ratio of $10^8$was obtained from unipolar switching. Guan et al. [47] have also reported a high resistance ratio of approximately 10^6using a Cu/ZrO_2:Cu/Pt structure. This suggests that our new $Cu/GeO_x/W$ cross-point memory is useful for future multilevel cell (MLC) applications.

Figure 8 shows the dependence of LRS on CCs ranging from 1 nA to 50 μA for the $Cu/GeO_x/W$ cross-point memories. The LRSs decreased linearly with increase of the CCs from 1 nA to 50 μA, which is applicable for MLC operation. By changing CCs (1 nA to few microamperes), more than four orders of magnitude of the LRS is shifted over the same range. If we consider that 3 resistance states per decade can be distinguished [3], the resistive memory using the $Cu/GeO_x/W$ structure will allow at least 12 states for the storage. The relationship between LRS and CC is related to the following equation:

$$\mathrm{LRS} = \frac{0.25}{\mathrm{CC}} \quad (1)$$

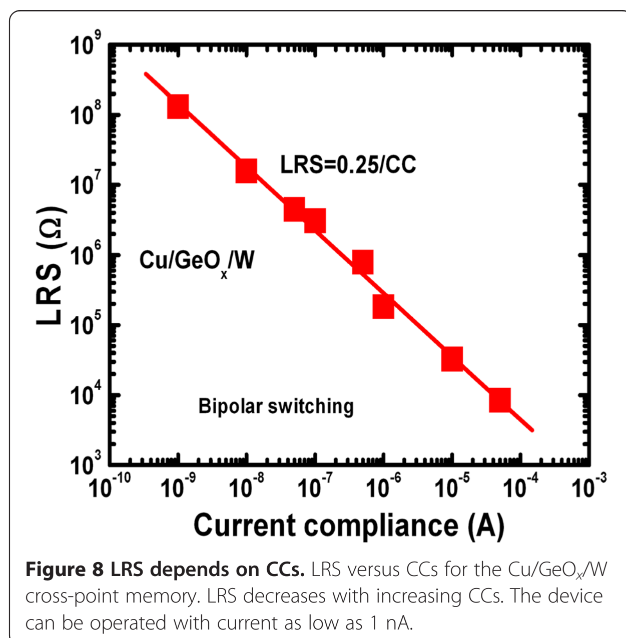

Figure 8 LRS depends on CCs. LRS versus CCs for the $Cu/GeO_x/W$ cross-point memory. LRS decreases with increasing CCs. The device can be operated with current as low as 1 nA.

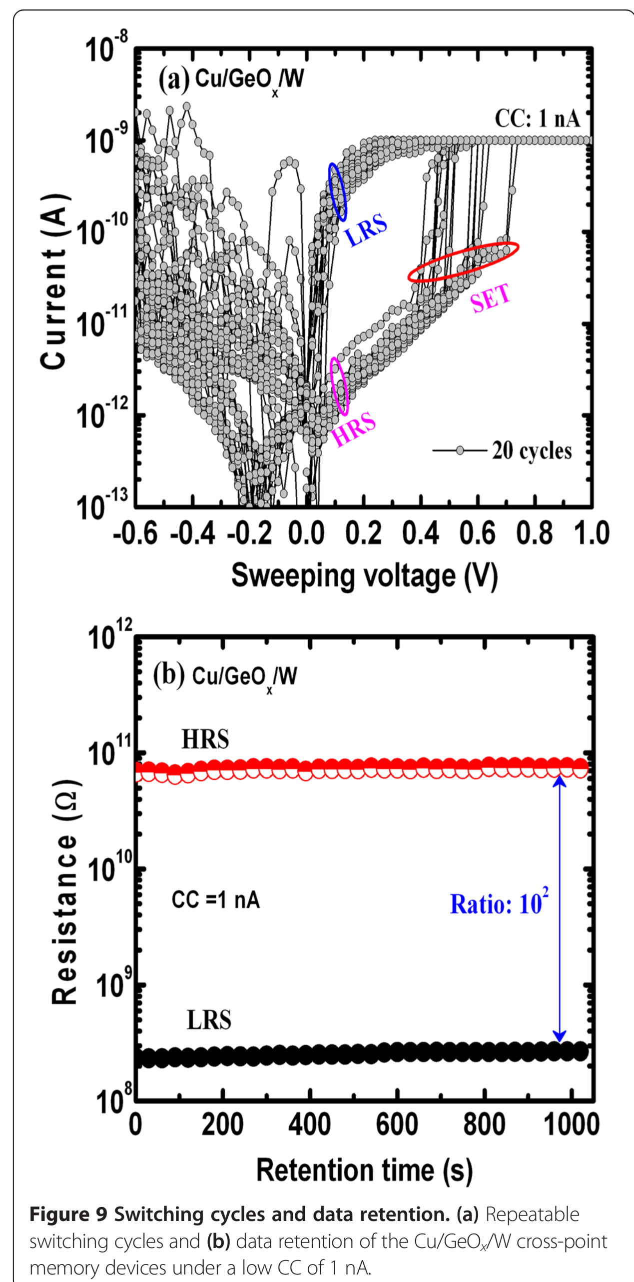

Figure 9 Switching cycles and data retention. (a) Repeatable switching cycles and **(b)** data retention of the $Cu/GeO_x/W$ cross-point memory devices under a low CC of 1 nA.

From Equation 1, the average LRS is 0.251/CC, which is close to the reported value of 0.250/CC for metallic filament [33,48]. Therefore, the CBRAM device can be designed easily for low-power MLC operation.

Figure 9a shows repeatable 20 DC switching cycles at a low CC of 1 nA. The SET voltages are varied from 0.4 to 0.8 V, and the RESET current increased after few cycles, which confirms a filament formation after few cycles [20,30]. The data retention of approximately 10^3 s is also observed under a low operation current of 1 nA (Figure 9b). The resistance ratio is approximately 10^2. Further study is needed to improve the cross-point resistive switching memory characteristics under low-current operation. In addition, the read pulse endurances of LRS and HRS are more than 10^5 cycles with a large resistance ratio of $>10^4$, and both resistance states are very stable without significant resistance variation for a retention test of more than 10^4 s under a CC of 50 μA (not shown here), which can be applicable for future low-power high-density nonvolatile memory applications.

Conclusions

Resistive switching memory characteristics using Cu and Al TEs on the GeO_x/W cross-point memory devices have been compared. Improved memory characteristics of the Cu/GeO_x/W structures under low current varying from 1 nA to 50 μA and a low voltage operation of ±2 V are observed as compared to those of the Al/GeO_x/W structures. These cross-point memory structures are observed by HRTEM. The formation of AlO_x layer with a thickness of approximately 5 nm at the Al/GeO_x interface is observed, which is unstable to control the resistive switching phenomena. The RESET current scalability is observed for Cu TE, while it is high (>1 mA) and independent for the Al TE with CCs varying from 1 nA to 500 μA. Superior resistive switching memory performances in terms of high resistance ratio (10^2 to 10^4 under bipolar and approximately 10^8 under unipolar modes), long pulse endurance of $>10^5$ cycles under a CC of 50 μA, and good scalability potential are observed for the Cu/GeO_x/W cross-point memory devices. Repeatable switching cycles and data retention of 10^3 s are also observed under a low CC of 1 nA. This study is important for high-density low-power 3D architecture in the future.

Competing interests

The authors declare that they have no competing interests.

Authors' contributions

SZR fabricated and measured the cross-point memory devices under the instruction of SM. SM arranged and finalized the manuscript. Both authors contributed to the preparation and revision of the manuscript and approved it for publication.

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