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# Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters


**Woo Jong Yu**[1], **Zheng Li**[1], **Hailong Zhou**[1], **Yu Chen**[2], **Yang Wang**[2], **Yu Huang**[2,3], and **Xiangfeng Duan**[1,3,*]

[1]Department of Chemistry and Biochemistry, University of California, Los Angeles, California 90095, USA

[2]Department of Materials Science and Engineering, University of California, Los Angeles, California 90095, USA

[3]California Nanosystems Institute, University of California, Los Angeles, California 90095, USA


## Abstract


The layered materials such as graphene have attracted considerable interest for future electronics. Here we report the vertical integration of multi-heterostructures of layered materials to enable high current density vertical field-effect transistors (VFETs). An n-channel VFET is created by sandwiching few-layer molybdenum disulfide ($MoS_2$) as the semiconducting channel between a monolayer graphene and a metal thin film. The VFETs exhibit a room temperature on-off ratio $>10^3$, while at same time deliver a high current density up to 5,000 A/cm$^2$, sufficient for high performance logic applications. This study offers a general strategy for the vertical integration of various layered materials to obtain both p- and n-channel transistors for complementary logic functions. A complementary inverter with larger than unit voltage gain is demonstrated by vertically stacking the layered materials of graphene, $Bi_2Sr_2Co_2O_8$ (p-channel), graphene, $MoS_2$ (n-channel), and metal thin film in sequence. The ability to simultaneously achieve high on-off ratio, high current density, and logic integration in the vertically stacked multi-heterostructures can open up a new dimension for future electronics to enable three-dimensional integration.


The layered materials such as graphene are of considerable interest as potential electronic materials for future electronics[1–8]. However, the lack of a bandgap in graphene has limited the on-off current ratio of graphene based transistors for logic applications. The approaches to address this challenge include the induction of transport gap in graphene nanostructures[9–13] or bilayer graphene[14–19], and the design of innovative device

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*Corresponding xduan@chem.ucla.edu.

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architectures such as vertical tunnelling transistors[20,21] and barristors[22]. These approaches have proven successful in improving the on-off ratio of the resulting devices, but often at a severe sacrifice of the deliverable current density. Here we report the vertical integration multi-heterostructures of layered materials (e.g. graphene, molybdenum disulfide $MoS_2$, or cobaltites $Bi_2Sr_2Co_2O_8$) to enable high current density vertical field-effect transistors (VFETs). We show that an n-channel VFET with a room temperature on-off ratio $>10^3$ can be created by vertically sandwiching semicoducting few-layer $MoS_2$ between a monolayer graphene and a metal thin film. Importantly, with an Ohmic contacted metal top-electrode and an ultrathin layered $MoS_2$ semiconductor channel, the VFET can deliver a high current density of 5,000 $A/cm^2$, about 2–5 orders of magnitude larger than the recently reported vertical tunnelling transistors or barristors[20,22], while retaining a high on-off ratio. Taking a step further, we demonstrate a complementary inverter with voltage gain can be created by vertically stacking the layered materials of graphene, $Bi_2Sr_2Co_2O_8$ (p-channel), graphene, $MoS_2$ (n-channel), and metal thin film in sequence. Our study demonstrates a general strategy for the integration of various layered materials to achieve functional circuits in the vertical direction, and can open up a new dimension for future electronics to enable three-dimensional integration.

The fabrication procedures for the VFET are schematically illustrated in Figure S1. In brief, monolayer graphene is first grown by the chemical vapor deposition (CVD) approach and transferred onto a silicon wafer with 300 nm $SiO_2$[23]. The graphene was patterned into strips of 10 μm width and 50 μm length by oxygen plasma etching through a photo resist mask for a bottom electrode. The micromechanical cleavage[24] was used to exfoliate few-layer $MoS_2$ onto the patterned graphene as a semiconductor material. The top metal electrode was patterned on the $MoS_2$ to overlap with the bottom graphene electrode by e-beam lithography and e-beam deposition of Ti/Au (50/50 nm). The current flows between the bottom graphene electrode and the top metal electrode through the semiconducting $MoS_2$ channel, which is modulated by the silicon back gate (Fig. 1a,b). Because of the finite density of states and weak electrostatic screening effect by monolayer graphene, the applied back gate electric field can effectively penetrate through graphene to modulate the energy band of $MoS_2$.

Figure 2a shows an optical image of our typical VFETs. The 10 μm strip of monolayer graphene is located inside of the doted lines. An $MoS_2$ flake and three top metal electrodes of variable areas overlap on top of the graphene. The thicknesses of $MoS_2$ flake were determined by atomic force microscope (AFM) to be 30 nm (Fig. S2). The total channel area is defined by overlapping area of graphene and top metal electrode. Two separate pairs of electrodes were formed on graphene and $MoS_2$ in the non-overlapping region to characterize the planar electrical performance. Cross-sectional TEM image was used to study the overall integration of graphene-$MoS_2$-top-electrode vertical stack. The complete stack of $SiO_2$/graphene/$MoS_2$/Ti/Au could be readily seen in the low magnification cross-section TEM image (Fig. 2b). A high-resolution TEM image of the $SiO_2$/graphene/$MoS_2$/Ti interface shows that the graphene layers are intimately integrated with the $MoS_2$ layers without any obvious gap or impurities between them (Fig. 2c). The layer spacings are 0.65 nm and 0.34 nm in $MoS_2$ layer and graphene layer, respectively. A TEM image of multilayer graphene device is shown here because of the difficulties in visualizing monolayer graphene device due to severe electron-beam damage while conducting TEM studies. Together, these studies

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clearly demonstrate that the physical assembly approach can effectively integrate layered graphene and $MoS_2$ to form intimate contact.

Electrical transport studies of the vertical transistors and planar transistors were carried out in ambient condition at room temperature. We have first measured the output characteristics of the vertical transistor (Fig. 3a). The vertical transistor in this study has 36 nm of channel length ($MoS_2$ thickness) as determined by AFM measurement. The current was normalized by overlapping area of graphene and top metal electrode to obtain current density. The output characteristics at various back gate voltages show clearly that the current density decreases with increasing negative gate potential, demonstrating that the electrons are the majority charge carriers in this vertical transistor, which is consistent with the typical n-type semiconducting characteristics observed in $MoS_2$ materials previously[25,26]. In the negative source-drain voltage ($V_{sd}$) regime, clear on and off current modulation can be achieved with the gate bias modulation. On the other hand, in the positive $V_{sd}$ regime, a much smaller gate modulation is observed. This difference can be attributed the asymmetrical contact at source and drain end, and will be further discussed in Figure 4.

Figure 3b shows the transfer characteristics ($I_{sd}$-$V_g$ curves) for the same device at $V_{sd}$ = −0.1, −0.2 and −0.5 V. Overall, the device shows a room temperature on-off current ratio of ~1,500 at all $V_{sd}$ values, which is about 1–2 orders of magnitude better than typical graphene devices at room temperature, and is already sufficient for typical logic device applications. The device delivers a large on-current density of 2,600 A/cm$^2$ at $V_{sd}$ = −0.5 V and $V_g$ = 60 V. In general, the maximum on-current density in an optimized VFET device can readily exceed 5,000 A/cm$^2$ at $V_{sd}$ = −1.0 V. It is particularly important to note that this current density is about 3–5 orders of magnitude larger than the recently reported vertical tunneling transistors[20,21] and barristor[22] at the same source-drain bias. Higher current density has been achieved in tunneling device with ultrathin boron nitride tunneling barriers (e.g. 1–3 layers)[21] and in barristor with larger bias[22], but typically with rather weak gate modulation. With our VFET structure, a high current density and a high on-off ratio are simultaneously achieved for the first time, which is essential for high performance logic transistors. Furthermore, the maximum on-current density in our VFET device can readily exceed 350,000 A/cm$^2$ at $V_{sd}$ = −4 V without consideration of on-off ratio, which is about two orders of magnitude larger than maximum current density of 5,000 A/cm$^2$ at $V_{sd}$ = 4V of the recent reported barristors (Fig. S3).

To further confirm the vertical charge transport in the VFETs, electrical characteristics of the planar transistors with few-layer $MoS_2$ as the planar channel are characterized as a control. Figure 3c shows the output characteristics of the planar transistor with non-overlapping bottom graphene and top metal source-drain electrodes, and Figure 3d shows the output characteristics of planar transistors between two top metal source-drain electrodes, as shown schematically in the insets of the respective figures. In these output characteristics, the current is normalized by the channel width. Although it is not necessarily accurate to compare area current density vs. line current density, it is still important to note that the actual current of our VFETs is at least more than 20 times larger than those of planar transistors with similar dimension. This striking difference in current amplitude between the vertical and planar devices confirms the charge transport in the vertical direction indeed

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dominates the vertical stacked devices. Additionally, studies on vertical devices with variable area in the range of 6–15 μm$^2$ result in comparable normalized area current densities (Fig. S4), further demonstrating the vertical charge transport is the dominant mechanism for the current flow in the vertical devices.

Figure 3a shows that the vertical transistor exhibits directionally dependent current flow and asymmetrical gate modulation, in which the output characteristics of the VFET were different under negative and positive source-drain biases. Clearly, under negative $V_{sd}$, the device has a large gate modulation exceeding 3 orders of magnitude, whereas under positive $V_{sd}$, the device shows a much smaller gate modulation. These results can be explained by using the band diagrams shown in Figure 4b and c, depicting the cases of negative and positive $V_{sd}$, respectively. The gate electric field is applied between silicon back gate and grounded top metal electrode. The graphene-$MoS_2$ barrier height and the $MoS_2$ Fermi level can be effectively modulated near the graphene-$MoS_2$ contact (Fig. 4a) because of limited density of states and weak electrostatic screening effect of graphene (Fig. 4b). In contrast, the $MoS_2$ Fermi level near the $MoS_2$-metal contact is effectively pinned can barely be modulated by the gate potential due to strong screening effect of the top-metal electrodes (Fig. 4c). As a result, an asymmetric gate modulation is expected between positive and negative $V_{sd}$.

The application of a negative $V_{sd}$ across the device makes electrons to flow from graphene to top electrode. In this case, the Schottky barrier at the contact between graphene-$MoS_2$ plays a dominant role in current modulation (Fig 4b), similar to the recent reported barristors[22]. A positive gate voltage effectively reduces the graphene- $MoS_2$ Schottky barrier height as well as the depletion width in $MoS_2$ layer, allowing electrons to readily overcome the Schottky barrier via thermionic emission or thermionic field emission processes, and therefore enhances the charge transport characteristics of the vertical device. In contrast, a negative gate voltage increases the Schottky barrier height and depletion width and suppresses the electron transport across the vertical stack. In this way, the device essentially operates as an n-type field-effect transistor in the negative $V_{sd}$ regime where the application of the gate voltage can effectively modulate the charge transport across the $MoS_2$ layer to result in a large on-off ratio in the vertical devices. On the other hand, under positive $V_{sd}$ conditions across the device, electrons are injected into $MoS_2$ through the top-metal electrode and roll downhill in $MoS_2$ to the bottom graphene electrodes. Therefore, the top metal-$MoS_2$ contact plays the primary role in determining the current modulation (Fig 4c). With the electrostatic screening effect of the top metal electrode, the weak gate modulation on the barrier at the top electrode-$MoS_2$ contact thus leads to a much smaller on-off ratio.

To further probe the charge transport through grahene-$MoS_2$-metal VFETs, we have carried out temperature dependent studies. A family of $I_{sd}$-$V_g$ plots ($V_{sd}$ = −0.1 V) obtained at different temperature demonstrates that the on-current exhibits relatively small temperature dependence while the off-current decreases exponentially with decreasing temperature, with the on-off ratio increased from 60 at 290 K to 15000 at 150 K (Fig. 4d). The variable temperature transport measurements can allow us to determine the Schottky barrier heights across the graphene-$MoS_2$ junction. According to the thermionic emission theory, the diode saturation current is related to the Schottky barrier height by the following equation:

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$$I_{sat}=AA^{*}T^{2}\exp\left(-\frac{q\varphi_{B}}{k_{B}T}\right) \quad (1)$$

where A is the area of the Schottky junction, $A^{*}=4\pi qm^{*}k_{B}{}^{2}h^{-3}$ is the effective Richardson constant, q is the elementary charge, $k_B$ is the Boltzmann constant, T is the temperature, m* is effective mass, and $h$ is plank constant[22]. The saturation current was determined from a plot of the logarithmic of the forward-bias current (Fig. S5). The ideality factor of the graphene-$MoS_2$ diode can also be determined from this plot to be 3–4.5. The deviation from an ideal diode may be attributed to graphene-$MoS_2$ interface defects and also likely the electrostatic screening effect of top $MoS_2$-metal contact due to the very small $MoS_2$ channel thickness (length). Based on the relation in equation (1), the Schottky barrier height can then be estimated from the slope of the $\ln(I_{sat}/T^2)$ vs. $q/k_BT$ plots (Fig. 4e). The derived Schottky barrier shows a clear dependence on the gate voltage ($V_g$): changing from 260 meV to 33 meV as the $V_g$ is increased from −60 V to 60 V. This change in Schottky barrier height can be largely attributed to modulation of graphene work function[22]. It is also important to note that the Schottky barrier height is hardly changed at large negative and large positive gate voltage points when Fermi level ($E_F$) of graphene is located far from Dirac point because of relatively high density of states at these points. However, the Schottky barrier height is dramatically changed near 0 V gate bias when $E_F$ is located near the Dirac point in graphene because of a much lower density of states. The Schottky barrier height at $V_g$ = 0 V is 150 meV, which is much smaller than the 400 meV value as expected from the energy level difference between the work function of graphene (4.5 eV) and the electron affinity of $MoS_2$ (~4.1 eV). This difference may be attributed to electrostatic screening effect of top metal electrode that could effectively reduce the bottom Schottky barrier height (and width) due to the ultra-short channel length (~20 nm).

It is important to note that our VFET is fundamentally different from the recently reported vertical tunnelling transistors in that the $MoS_2$ layer in our device functions as a true semiconducting channel instead of an insulating tunnelling barrier[20], which has allowed us to achieve a much larger vertical current flow while retaining a high on-off ratio. In general, our device exhibits a unipolar behaviour with electrons as the majority carriers (dictated by n-type $MoS_2$ layer) instead of bipolar characteristics in vertical tunnelling transistors with the carrier type determined by the gate modulated graphene. To further understand the difference between out VFETs and the reported vertical tunnelling transistors, we have considered three different device configurations including graphene-$MoS_2$-graphene tunnelling barrier (GMG TB) (Fig. S6a), graphene-$MoS_2$-graphene schottky barrier (GMG SB) (Fig. S6b), and graphene-$MoS_2$-metal (Ti) schottky barrier (GMM SB) (Fig. S6c) with variable $MoS_2$ thickness and calculated the corresponding current density (see Supplementary Information for details) for each configuration.

For the GMG stack with very thin $MoS_2$ layer (< 4nm), the Fermi level in $MoS_2$ are effectively pinned by both the bottom and top junctions and can barely be modulated by the back gate (Fig. S6a). The tunnelling current is the dominant component in charge transport (blue line in Fig. 4f, S7). Our calculation shows that high current density ($>10^1$ A/cm$^2$) can be achieved by using 1–4 layers of $MoS_2$ tunneling barrier but typically with a rather weak

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gate modulation (< $10^2$); and a rather large on-off current ratio can be achieved by using 5–7 layer $MoS_2$ (~2.5–4 nm) tunneling barrier, but with relatively small current density (<1 A/cm$^2$) (see, Fig. S7, as also confirmed by ref. 20). For even thicker $MoS_2$ layers (> 4 nm), the thermionic emission through the Schottky barrier becomes the dominant component in charge transport. The calculated thermionic emission current shows a rather weak dependence on the $MoS_2$ thickness in the range of 4–40 nm, likely due to a complete depletion of the semiconductor layer and downhill charge transport after crossing the barrier. It is important to note that there is substantial difference between GMM (Ti) SB and GMG SB device, the calculated current density of GMM (Ti) SB (black line in Fig. 4f) is about 3 orders of magnitude larger than that of GMG SB configuration (red line in Fig. 4f).

We have experimentally investigated a large number of GMM (Ti) SB devices with variable $MoS_2$ thickness and device sizes. The overall on-current density is typically in the range of $10^3$~$10^4$ A/cm$^2$ with a weak dependence on the $MoS_2$ layer thickness (black square symbols in Fig. 4f), matching well with calculated current density. Studies on GMG SB devices with variable $MoS_2$ thickness have also be done as a control experiment (Fig. S8). The obtained on-current in GMG SB devices (red dot symbols in Fig. 4f) is about 2–3 orders magnitude smaller than that of GMM(Ti) SB devices, consistent with theoretical calculations. This consistent difference observed in theoretical modeling as well as experimental studies clearly demonstrate our GMM SB device is fundamentally distinct from the GMG SB structure. In the GMG SB with thick $MoS_2$ layer, two Schottky barriers are formed at both $MoS_2$-graphene contacts with the bottom-one strongly modulated and top-one weakly modulated by the back-gate in the opposite direction (Fig. S6b). Even though the electrons can be effectively injected through the bottom barrier at on-state, the top Schottky barrier can suppress the overall current flow to result in a lower current density. In contrast, for GMM SB configuration, the top Schottky barrier height is minimized and can hardly be modulated by using a low work function metal (Ti) to make a nearly Ohmic contact with $MoS_2$ (Fig. S6c). In this way, the charge transport is dominated by the bottom graphene-$MoS_2$ Schottky barrier height and width, which can be effectively modulated by the back-gate voltage to allow for highly efficient injection and transportation of the electrons through the $MoS_2$ layer, enabling a very large current density that is about 3 orders of magnitude larger than that of the GMG TB or GMG SB devices with similar on-off ratios. Additionally, comparing the recently reported barristors with bulk silicon as the semiconductor layer to our GMM SB device, the charge transport through thick bulk silicon (>> 10 μm Si) and the thick depletion layer at graphene-Si junction can severely limit the overall current flow to result in a current density that is also about 2–3 orders of magnitude smaller than our GMM SB VFETs reported here[22].

Figure 4g shows the room temperature on-off current ratios of the VFETs. The on-off ratios are strongly dependent on the $MoS_2$ thickness. In general, it is found that the room temperature on-off ratio of the vertical transistors can exceed 3 orders of magnitude with relatively thick $MoS_2$ layer (e.g. 30–40 nm), and gradually decreases to 3 when the $MoS_2$ thickness is reduced to 9 nm or so. This trend can be explained by a short channel effect. With decreasing $MoS_2$ thickness, the potential of entire channel (including graphene-$MoS_2$ contact) is becoming more and more dominated by the electric field of top metal electrodes, which can reduce the bottom off-state Schottky barrier height and width to result in a

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smaller on-off ratio (Fig. 4g insets). The room temperature on-off ratio of $>10^3$ achieved in our devices is about two order of magnitude smaller than the best on-off ratio achieved in recently reported barristors[22], which might be attributed to the presence of interface defects at the graphene-$MoS_2$ interface, and can be improved to $>10^4$ upon cooling (as demonstrated by our low temperature studies, see Fig. 4b) or with cleaner interfaces in future studies.

This strategy of vertical integration is general and can be readily extended to various layered materials to obtain vertically stacked devices with both n- and p-channel characteristics. For example, layered transition metal oxides such as cobaltites $Bi_2Sr_2Co_2O_8$ (BSCO)[29,30] can be exfoliated into single or few layer materials and exhibit p-channel characteristics (Fig. S9). Taking a step further, multiple layers of layered materials can be vertically stacked to enable more complicated device functions. To this end, we have demonstrated a complementary inverter by vertically stacking multi-heterostructures of the layered materials including, graphene, $Bi_2Sr_2Co_2O_8$ (BSCO) (p-channel), graphene, $MoS_2$ (n-channel), and metal thin film on Si/$SiN_x$ (20 nm) substrate (Fig. 5a,b, and Fig. S10). In this complementary inverter, the vertically stacked BSCO layer functions as a p-channel VFET, and the $MoS_2$ layer functions as the n-channel VFET. Supply voltage was applied to bottom layer graphene and top metal electrode was connected to the ground. Output voltage was measured on the intermediate layer graphene as a function of input voltage on silicon back gate. Electrical measurement shows the vertically stacked BSCO layer with both bottom- and top-graphene contacts shows clear p-channel characteristics (Fig. 5c). More importantly, the top stack of n-channel $MoS_2$ VFET retains excellent switching characteristics (Fig. S11), demonstrating the bottom-gate electrical field can readily penetrate through the entire bottom p-channel device to effectively modulating the top n-channel VFET. In this way, the vertically stacked multi-heterostructures forms a complementary inverter with a large than unit voltage gain (1.7) (Fig. 5d).

In conclusion, we have demonstrated that vertical integration of heterostructures of layered materials can enable a new design of graphene based transistors simultaneously with both high on-off current ratio and high current density at room temperature, to satisfy two critical requirements for high performance logic applications. With the use of ultrathin layered semiconductor channel and the Ohmic contacted top metal-electrode, our VFETs can deliver an unprecedented current density that is 2–5 orders magnitude larger than that of the recently reported graphene based vertical tunnelling transistors and barristors[20,22], while retaining a the room temperature on-off current ratio exceeding 3 orders of magnitude. It should be noted that the achievement of high current density is central to the performance of a transistor since the intrinsic delay of a transistor ($\tau$=CV/I) is inversely proportional to the deliverable current density. With similar device geometry, higher current at the same bias can be directly translated into higher device speed. Taking a step further, we have also demonstrated that the vertical integration of multi-heterostructures of layered materials can be used to effectively create more complicated device functions including a complementary inverter with more than unit voltage gain. A striking point that we demonstrate here is the electrical field can readily penetrate through first layer of p-FET to effectively modulate the second layer n-FET, making the vertical integration of multi-heterostructures possible and meaningful for functional devices. Our study demonstrates, for the first time, the feasibility to implement the vertically stacked devices for useful logic functions with gain. This is

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fundamentally different the recently reported logic functions achieved from the lateral integration of p- and n-type barristors[22], which is largely similar to the conventional planar electronics. Our study demonstrates a general strategy to integrate layered materials in the vertical direction to enable functional devices and circuits, and can open up a new dimension for high density integration of function devices in the limited circuit area.

## Methods

### Synthesis and characterization

The graphene was grown by chemical vapor deposition on copper foil at 1050 °C with methane as the carbon-containing precursor. After growth, the graphene was transferred onto silicon/silicon oxide substrate and patterned into 50 by10 μm strips by oxygen plasma etching. The molybdenum disulfide flakes ($MoS_2$) were then exfoliated onto the graphene strips using a micromechanical cleavage approach. The top metal electrode was patterned on the $MoS_2$ to overlap with graphene by e-beam lithography and e-beam deposition of Ti/Au (50/50 nm).

### Microscopic and electrical characterization

The cross section TEM sample was prepared by a focused ion beam cutting and was characterized by a TF20 TEM operating at 300 kV. Tapping-mode AFM was carried out with a Veeco 5000 system. SEM imaging was performed on a JEOL 6700F unit operated at 5 kV. The D.C. electrical transport studies were conducted with a probe station at room temperature under ambient conditions with a computer-controlled analogue-to-digital converter.

## Supplementary Material

Refer to Web version on PubMed Central for supplementary material.

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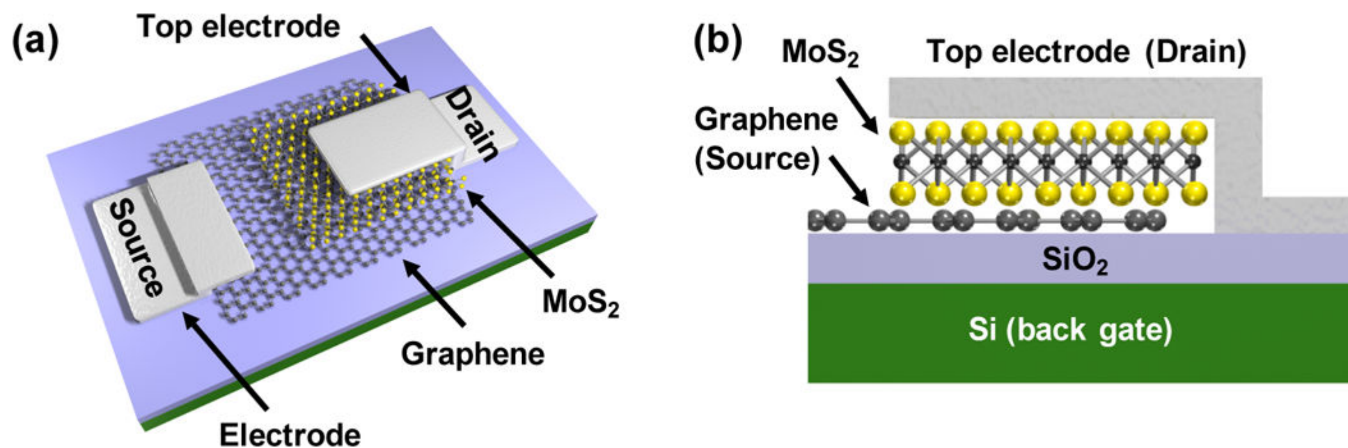


**Figure 1. Schematic illustration of the vertically stacked graphene-$MoS_2$-metal field-effect transistors**

**a,** A schematic illustration of the three-dimensional view of the device layout. **b,** A schematic illustration of the cross-sectional view of the device, with the graphene and top metal thin film functioning as the source and drain electrodes, the $MoS_2$ layer as the vertically stacked semiconducting channel and its thickness defines the channel length. Silicon back gate is used with 300-nm $SiO_2$ dielectric layer.

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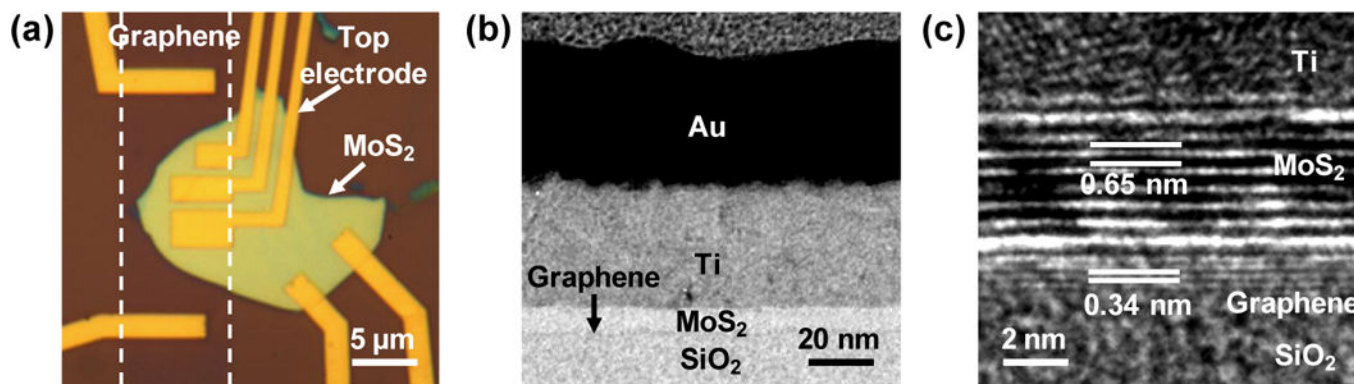


**Figure 2. Fabrication and structural characterization of the vertical transistor**

**a,** An optical image of a typical vertical transistor device. Bottom graphene electrode is shaped to stripes of 10 μm width. Multi-layer $MoS_2$ is located on the graphene electrode and top metal electrode is located on $MoS_2$ to overlap with bottom graphene electrode to enable vertical current flow. **b,** A cross-sectional TEM image of a vertical transistor. **c**, A cross-sectional HRTEM image of the interface between multi-layer graphene, multi-layer $MoS_2$ and top electrode of Ti. A TEM image of multilayer graphene device is shown here for better illustration because it is difficult to visualize the monolayer graphene electrode due to significant electron-beam damage while conducting the TEM studies.

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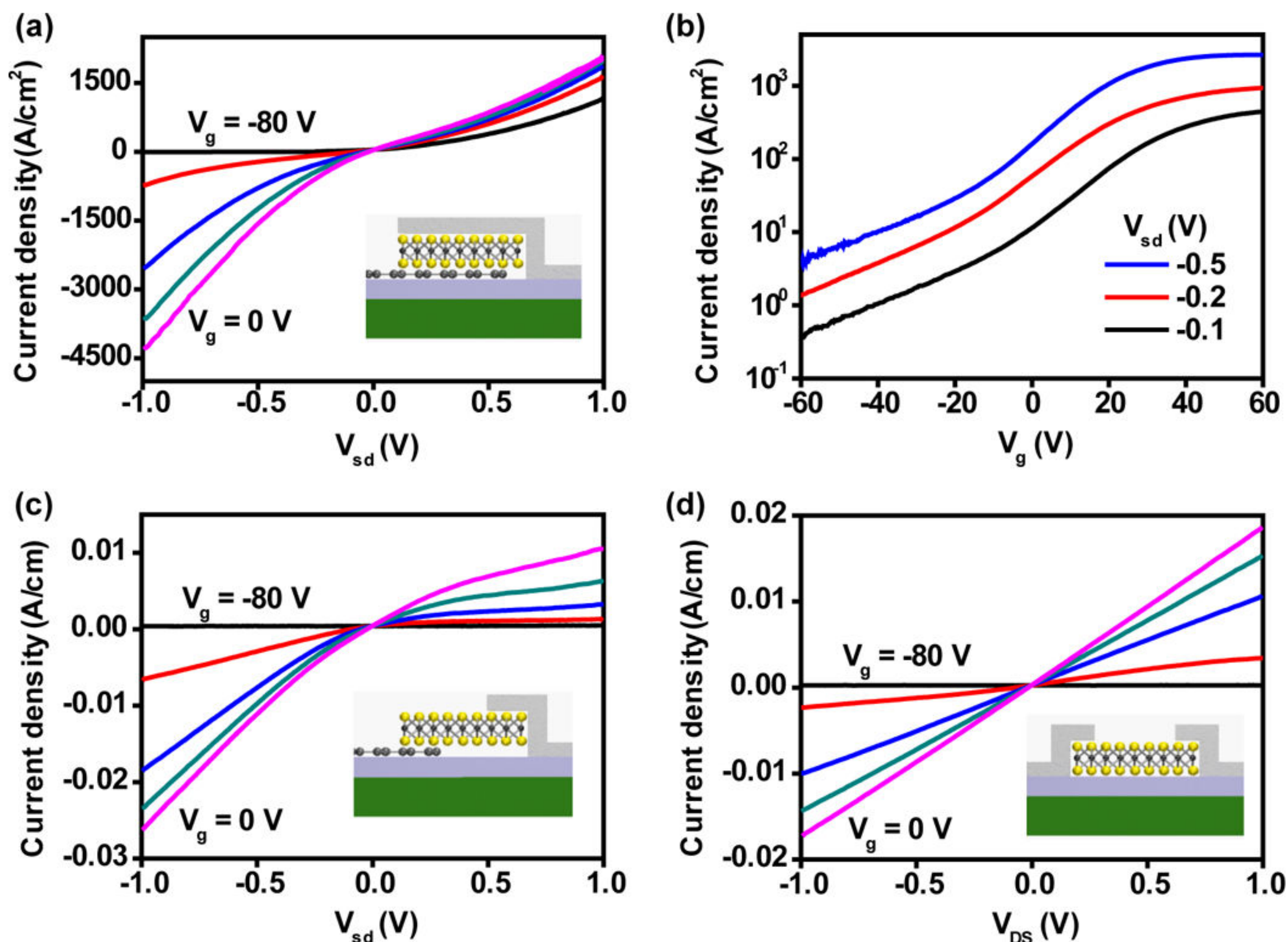


**Figure 3. Room temperature electrical properties of the vertical and planar transistors**

**a,** $I_{sd}$-$V_{sd}$ output characteristics of a vertical transistor. The current is normalized by the area. **b,** $I_{sd}$-$V_{gs}$ transfer characteristics of the device shown in **a** at $V_{sd} = -0.1$, $-0.2$, and $-0.5$ V. **c,** $I_{sd}$-$V_{sd}$ output characteristics of a planar transistor with $MoS_2$ channel between a graphene electrode and metal electrode. **d,** $I_{ds}$-$V_{sd}$ output characteristics of a planar transistor with two top metal electrodes on planar $MoS_2$ channel. The current is normalized by the width of the electrode in **c** and **d**. The back-gate voltage is varied from −80 V to 0 V in the step of 20 V in **a, c** and **d**. Insets in **a, c** and **d** shows the schematics of the transistor structure for each output characteristics.

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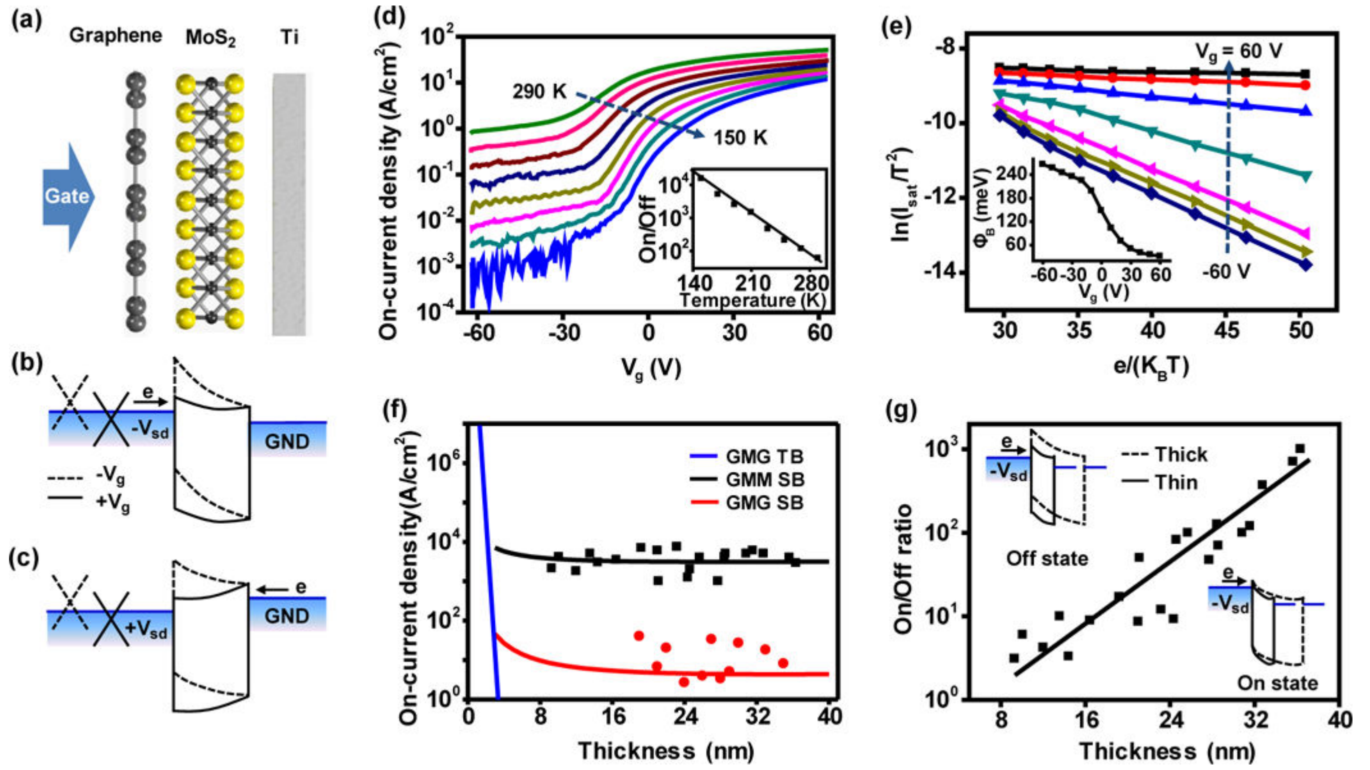


**Figure 4. Schematic illustration of the band diagrams of the vertical transistors and the electrical characteristics**

**a,** The schematic illustration of a vertical transistor. Gate electric field is applied from silicon back gate located bottom of graphene and grounded top electrode. **b, c,** The band structure at negative source bias at graphene (**b,** $V_{sd}<0$) and positive source bias at graphene (**c,** $V_{sd}>0$) under positive (solid) or negative (dashed) $V_g$. **d,** Transfer characteristics of a VFET at different temperature from 290 K to 150 K. The inset shows the corresponding on-off ratio variation. **e,** Temperature dependent diode characteristics. Each curve from bottom to top is obtained at different $V_g$ from −60 V to 60 V with 20 V step variation. The inset shows corresponding Schottky barrier height variation obtained from the slope of the fitted line. **f,** The simulated on-current density of graphene-$MoS_2$-graphene tunneling barrier (GMG TB, blue line), graphene-$MoS_2$-Metal(Ti) Schottky barrier (GMM SB, black line), and graphene-$MoS_2$-graphene Schottky barrier (GMG SB, red line) at bias of −0.1 V. Experimental on-current density are plotted by black square (■) for GMM SB and red circle (●) for GMG SB at $V_{sd}$ = −0.5 V. **g,** The on-off current ratio of the vertical transistors with various channel length (thickness of $MoS_2$). The on- and off-state band diagrams for thin (solid) and thick (dashed) $MoS_2$ layers are represented in the insets.

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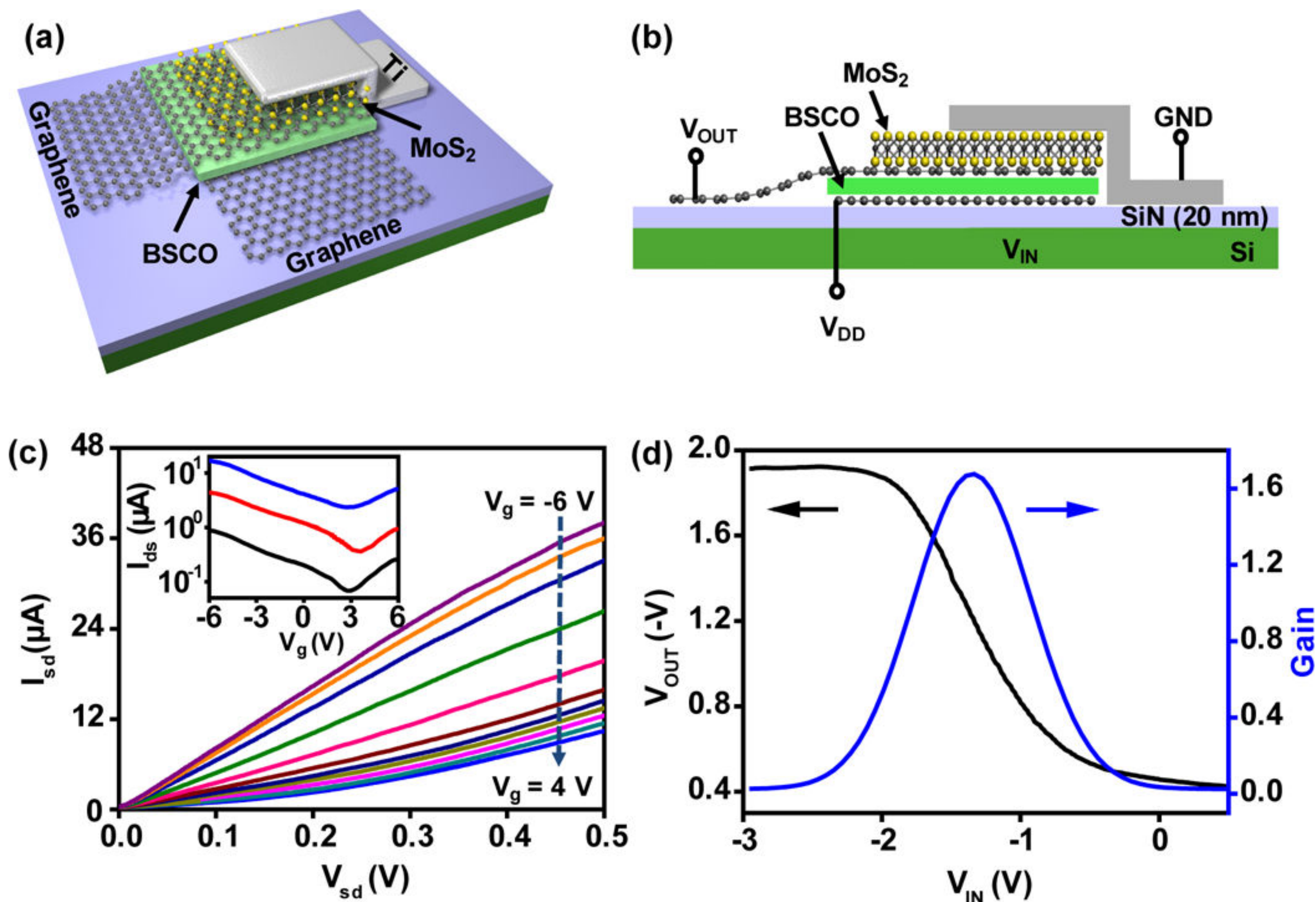


**Figure 5. Vertically stacked multi-heterostructures of layered materials for complementary inverters**

**a,** Three dimensional schematic illustration of a complementary inverter by vertically stacking the layered materials of graphene, $Bi_2Sr_2Co_2O_8$ (BSCO) (p-channel), graphene, MoS2 (n-channel), and metal thin film on Si/$SiN_x$ (20 nm) substrate. **b,** Cross-sectional view of the vertically stacked inverter. **c,** Output characteristics of a p-channel $Bi_2Sr_2Co_2O_8$ VFET with top and bottom graphene electrodes on Si/$SiN_x$ (20 nm) substrate. The back-gate voltage is varied from −6 V (top) to 4 V (bottom) in the step of 1 V. The inset shows the transfer characteristics of $Bi_2Sr_2Co_2O_8$ VFET at $V_{sd}$ = −0.2, −0.05, and −0.01 V from top to bottom. **d,** The inverter characteristics from vertically stacked p- and n-type VFETs. A negative supply voltage ($V_{DD}$=−2V) is applied to bottom graphene, and the gain of the inverter is ~1.7.