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Waveform-Sampling Electronics for a Whole-Body Time-of-Flight PET Scanner

W. J. Ashmanskas,

Department of Radiology, Physics & Instrumentation Group, University of Pennsylvania, Philadelphia, PA 19104-4209, USA

B. C. LeGeyt,

Department of Radiology, Physics & Instrumentation Group, University of Pennsylvania, Philadelphia, PA 19104-4209, USA

F. M. Newcomer [Member, IEEE],

Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, PA 19104-6396, USA

J. V. Panetta,

Department of Radiology, Physics & Instrumentation Group, University of Pennsylvania, Philadelphia, PA 19104-4209, USA

W. A. Ryan [Member, IEEE],

Department of Radiology, Physics & Instrumentation Group, University of Pennsylvania, Philadelphia, PA 19104-4209, USA

R. Van Berg [Senior Member, IEEE],

Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, PA 19104-6396, USA

R. I. Wiener, and

Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, PA 19104-6396, USA

J. S. Karp Fellow [Fellow, IEEE]

Department of Radiology, Physics & Instrumentation Group, University of Pennsylvania, Philadelphia, PA 19104-4209, USA. Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, PA 19104-6396, USA

W. J. Ashmanskas: ashmansk@hep.upenn.edu

Abstract

Waveform sampling is an appealing technique for instruments requiring precision time and pulse-height measurements. Sampling each PMT waveform at oscilloscope-like rates of several gigasamples per second enables one to process PMT signals digitally, which in turn makes it straightforward to optimize timing resolution and amplitude (energy and position) resolution in response to calibration effects, pile-up effects, and other systematic sources of waveform

variation. We describe a system design and preliminary implementation that neatly maps waveform-sampling technology onto the LaPET prototype whole-body time-of-flight PET scanner that serves as the platform for testing this new technology.

I. Introduction

Progress in time-of-flight (TOF) PET timing resolution continues to improve the clinical benefit of PET imaging. A PET scanner's electronics and data-acquisition system must retain the intrinsic accuracy of the detector resolution—timing, energy, and spatial—and maximize the use of available information. The dominant architecture for TOF PET electronics in use today employs separate signal-processing paths for timing and energy measurements, with dedicated TDCs to record pulses' arrival times and moderate-speed (~ 100 MSPS) ADCs to integrate the charge collected from each PMT. Refs. [1],[2],[3],[4] describe examples of that architecture. An alternative approach, called waveform sampling (WFS), uses just one signal path, sampled at oscilloscope-like rates (several gigasamples per second (GSPS)), to extract arrival time, integrated charge, baseline offset, and pulse-shape quality for each PMT. While instrumenting a complete scanner for oscilloscope-quality sampling using conventional flash ADCs would be both power-intensive and prohibitively expensive, recent advances in switched-capacitor-array ASICs such as the Domino Ring Sampler (DRS4) [5],[6] have made WFS affordable for large systems, such as a whole-body TOF PET scanner.

LaPET is a whole-body TOF PET scanner using 38880 LaBr₃:5%Ce [7] scintillator crystals of dimension $4 \times 4 \times 30$ mm³, imaged by 432 Photonis XP20D0 PMTs, grouped into 24 identical detector modules (Fig. 1). Our group previously reported coincidence timing resolution 315–330 ps (FWHM) [8] in single-module benchtop measurements and 375 ps in full-system measurements using semi-custom electronics [9],[10]. The semi-custom electronics are adapted from an older commercial readout system, some parts of which are now obsolete, and instrument only 360 of the 432 PMTs. Here we report on a complete WFS-based redesign of the LaPET electronics, trigger, and data-acquisition system.

WFS offers four key advantages for LaPET: capability to obtain the best intrinsic timing and energy performance [11]; flexibility in handling channel-to-channel calibration effects such as gain variation and timing offsets; flexibility in handling pile-up effects and baseline offsets; and ease with which new pulse-processing techniques can be implemented in a whole-body prototype scanner (Fig. 2). An important difference between a benchtop setup and a full system is the handling of large numbers of channel-by-channel timing and gain variations. *In situ* measurements suggest that present LaPET system timing resolution is limited by such effects. In addition, simulation studies suggest that pile-up effects at high count rate can be mitigated by applying a pulse-shape goodness criterion to sampled waveforms. We thus expect the upgraded electronics to provide system-level performance that more closely approximates single-module benchtop results and to preserve that performance at count rates encountered for patient imaging. The flexibility provided by a full readout system using WFS electronics is an asset for a prototype scanner such as LaPET. Whereas the pulse processing for conventional electronics is largely hard-wired into the circuit-board design, with modifications requiring at minimum several weeks to re-

solder analog filter components, the pulse processing for the DRS4-based system is performed in FPGA firmware. Implementing (and reversing) a modified pulse-processing algorithm for full-system study becomes as straightforward as loading updated firmware into the FPGAs that control LaPET's readout.

Our goals in upgrading LaPET's electronics are both to explore the feasibility of WFS for a large scanner and to improve the overall performance of this prototype scanner. The technology and methods we employ have wide applicability—possibly to eventual implementation in commercial scanners.

The outline of this paper is as follows. In Section II we describe the design of the full system of electronics needed to instrument the complete LaPET scanner for waveform sampling. In Section III we describe experimental tests of $\frac{1}{24}$ of these electronics using a small detector array to validate the performance of the design. This is followed in Section IV by results of these benchtop tests and in Section V by a discussion of how these electronics will enhance the performance and functionality of a TOF PET scanner and next steps for implementation on our prototype LaPET scanner.

II. Design

Our design uses 240 DRS4 chips to obtain oscilloscope-quality sampling of each PMT waveform at 2–5 GSPS. The 7 PMTs with which each crystal's scintillation light is collected map cleanly into the 8 analog inputs of a DRS4 chip, facilitating a redundant and nearly deadtime-free trigger design, in spite of the $3 \mu\text{s}$ required for DRS4 readout. An FPGA-based trigger using analog pulse shaping and 100 MSPS sampling provides coarse energy and timing measurements used to detect coincident pairs and to select DRS4 chips for readout.

In our electronics (Fig. 3), each of LaPET's 24 detector modules is read out by one Module Readout Board (MRB), while coincidence detection between the 24 MRBs is performed by a single Master Coincidence Unit (MCU). An MRB contains 10 DRS4 chips, corresponding to the 10 trigger centers labeled A–J in Fig. 4. A DRS4 samples each of the 7 PMTs forming a trigger zone (6 PMTs for edge zones A and J), as Fig. 4 illustrates for zone F. An eighth DRS4 channel samples a 100 MHz reference clock. The trigger zone concept is explained in detail in Ref. [9]. When readout of a trigger zone is desired, the corresponding DRS4 is stopped for digitization at 33 MSPS by an 8-channel AD9222 ADC. We digitize a region of interest (nominally 100 samples, or 50 ns) sufficient to measure a pre-pulse baseline offset, a leading-edge time, an integrated charge, and a pulse-shape goodness criterion. A Xilinx Virtex-5 FPGA handles control and readout of the MRB's ADCs and DRS4 chips, as well as the board's trigger functions.

Because DRS4 readout renders a trigger zone dead for about $3 \mu\text{s}$ ($30 \text{ ns} \times N_{\text{samples}}$), the trigger must be both selective and redundant to eliminate system deadtime. The MRB trigger path (shown at the bottom of Fig. 4) digitizes all 24 PMT waveforms at 100 MSPS to select a trigger zone and to provide coarse energy and time measurements. Analog circuitry shapes PMT pulses into roughly triangular pulses that rise+fall in 15+15 ns, such that three consecutive samples provide a timing centroid sufficient to form the $\sim 6 \text{ ns}$ coincidence gate.

We chose the 100 MSPS AD9287 after a survey of cost and power consumption of available moderate-speed ADCs. Every 10 ns clock cycle, the MRB's FPGA-based trigger logic combines 3 successive samples from the 7 PMTs in each trigger zone, applies an energy window ($\sim 400\text{--}600$ keV), and may identify one available trigger zone as a single-photon candidate. The energy is estimated by summing $E = \sum_i Q_i$ over 3 successive 10 ns samples for all PMTs in the 7-PMT trigger zone. A time offset with respect to the 10 ns clock edge is estimated for the 7-PMT ring as $t = \sum_i t_i Q_i / E$, where t_i is $-1, 0, +1$ for the 3 successive 10 ns samples. This t sum is adjusted for a PMT-by-PMT timing offset. If an MRB finds an acceptable single-photon candidate, it sends a 6-bit time stamp (0.3125 ns binning) to the MCU for confirmation.

If more than one of the MRB's 10 trigger zones fall within the energy window, the zone with the largest in-range energy is chosen. Busy zones are not considered: a zone firing the single-photon trigger is marked busy until the coincidence logic completes; a zone for which a coincidence is found remains busy until DRS4 readout completes. The large overlap between neighboring trigger zones provides important redundancy: if the preferred DRS4 chip to collect the light from a given photon candidate is busy, typically a nearby non-busy DRS4 is wired to collect $\sim 90\%$ of the light seen by the first-choice DRS4.

Each 10 ns cycle, the MCU's FPGA logic checks for photon pairs whose differences in timing and in azimuth are consistent with positron annihilation within the scanner's transaxial field of view; the MCU accepts or rejects each single-photon candidate with fixed latency ~ 200 ns. The MRB/MCU link uses Category 7a shielded twisted-pair cable, on which one pair distributes the global 100 MHz clock from the MCU, two pairs (400 Mbps bit rate per pair) carry single-photon time stamps from MRB to MCU, and the fourth pair (also 400 Mbps) carries coincidence accepts/rejects as well as system-wide synchronization messages.

For an accepted trigger, each corresponding MRB stops the selected DRS4, processes the 7 PMT waveforms in FPGA logic, and transmits ~ 100 bytes of summary data via Ethernet link (UDP protocol) to a Linux PC for further processing and storage. (See Fig. 3 for a system block diagram.) Deadtime is negligible in detailed simulation studies at nominal clinical conditions of ~ 20 MHz single-photon trigger rate and ~ 700 kHz prompt coincidence rate and remains below 1% at ~ 50 MHz simulated single-photon rate. The redundancy provided by overlapping DRS4 trigger zones, described above, is a key factor in eliminating deadtime at high count rate.

Three SAM (shaper/analog mezzanine) cards provide analog shaping for each MRB (Figs. 5,6). Each SAM card accepts 6 PMT inputs, with adjustable attenuation for each input provided via termination jumpers. There are two shaping paths per PMT signal. One path, read out via the DRS4 chips, preserves each pulse's fast leading edge for TOF measurements but reduces the pulse width from 75 ns to 35 ns (measured where leading and trailing edges cross 5% of peak voltage), reducing the severity of pulse-pile-up effects at high count rates and reducing the time interval that must be digitized in order to separate cleanly the pulse of interest from earlier pulses. A second path, read out via the 100 MSPS

trigger ADCs, rises+falls in 15+15 ns so that the shaped pulse's centroid and area, respectively, provide coarse timing and energy measurements for coincidence detection.

Once the waveforms from a given DRS4 chip are digitized, they are processed digitally to extract a voltage baseline offset, the light incident on each PMT (for position and energy), the arrival time, and a measure of waveform quality (Fig. 2). Averaging 10–20 samples before the incident pulse ($t < 0$ in Fig. 2) provides a baseline voltage to be subtracted from each sample, thus removing low-frequency variations in the quiescent voltage level caused e.g. by power-supply noise. To compute each PMT's incident light, baseline-subtracted samples are integrated, starting a few ns before the leading edge. Our initial measurements show that the optimal integration time is in the range of 30 ns to achieve the best trade-off of energy resolution and pile-up rejection. The design allows for the possibility that integration time will vary with count rate.

To compute an arrival time for a given 511 keV photon, the 7 baseline-subtracted PMT waveforms read from the selected DRS4 are digitally summed, with PMT gain and timing offsets applied to each waveform. A programmable moving-average filter combines adjacent samples to reduce random noise; the empirically optimized window length for the filter is comparable to the 2.5 ns PMT risetime. Interpolation then finds the time at which the filtered waveform crosses a fixed fraction of the pulse amplitude; the empirically optimized threshold is typically 5–10%.

As Fig. 2 illustrates, the shape of the sampled waveform contains information that can potentially flag pile-up pulses, by comparing sampled waveforms with a template. Candidate algorithms have been identified in simulation studies but have not yet been tested with waveform data.

While the MRB's FPGA logic is designed to handle moderate variations in channel-to-channel gain and timing, our system design includes one High Voltage Control (HVC) board for each LaPET detector module to minimize these variations. The HVC board [12] is a digitally programmable power supply capable of independently controlling the dynode and photocathode biasing voltages for each of 18 PMTs. The full scanner requires 24 HVC boards.

III. Experimental setup

While the complete system we have designed will use 24 MRBs to read out the LaPET scanner, to date we have recorded PMT signals using one prototype MRB on a test bench. Here we describe the experimental setup used to test the performance of the board and to validate the design before scaling it up to the full scanner.

The geometry used for testing a single MRB, with two attached SAM cards, is shown in Fig. 7 (left). A 5×5 array of LaBr₃:5%Ce crystals is centered on a ring of 7 Photonis XP20D0 PMTs. The reference detector is a $\phi 14\text{mm} \times 18\text{mm}$ LaBr₃:5%Ce cylinder centered on a single Photonis XP20D0 PMT. The reference detector is placed above the array+ring, all enclosed in a light-tight box, with a $5 \mu\text{Ci}$ ²²Na source placed between the array and the cylinder. The center PMT corresponds to the PMT labeled "C" in Fig. 4, so that the zone-C

DRS4 chip records all 7 PMTs from the ring. The reference PMT corresponds to the upper-left PMT in Fig. 4 and is read out via the zone-A DRS4.

In these tests, the FPGA trigger logic for zone A is modified to consider only the reference PMT, while the logic for zone C is unmodified. Whereas in normal operation the two DRS4 chips containing the two coincident 511 keV photons would reside on two separate MRBs, with coincidences identified by the MCU, for single-MRB testing the two relevant DRS4 chips are on the same MRB, with coincidences identified by ad-hoc firmware within the MRB's FPGA. Also, the readout logic currently transmits raw DRS4 waveforms (450 samples per PMT) over Ethernet to the PC. Thus, in tests to date, all waveform processing (to extract time, energy, position, etc.) runs in PC software rather than in FPGA firmware.

Using the geometry shown in Fig. 7 (right), we have performed another set of benchtop measurements of LaBr₃:Ce crystals and Photonis XP20D0 PMTs (2.5 ns risetime), to compare conventional electronics, commercial digitizer modules, and DRS4 evaluation modules. These measurements placed in coincidence a pair of cylindrical $\phi 14\text{mm} \times 18\text{mm}$ LaBr₃:5%Ce Saint Gobain BrillanCe 380 standard detector crystals, each centered on a Photonis XP20D0 PMT. Arrival times of WFS pulses were computed using the digital leading-edge algorithm described in Section II.

IV. Results

Table I shows coincidence time resolution measured using conventional NIM/CAMAC electronics (LeCroy 825z risetime-compensated discriminator, CAEN C414 TDC with 25 ps binning, LeCroy 2249W charge-integrating ADC), using an Agilent DC271 digitizer board (2 GSPS, 8-bit), and using a DRS4 evaluation board (5 GSPS, 11-bit). These results have been reproduced numerous times in our lab, in a variety of experimental setups. For cases studied, WFS performs at least as well as conventional electronics,¹ and DRS4 evaluation modules perform equivalently to commercial digitizer modules, at an order of magnitude lower cost per channel. Thus, a DRS4-based design can affordably (about \$30 per channel of DRS4+ADC) equip the full LaPET scanner to provide WFS PMT-by-PMT.

We have built and tested 12 SAM cards, out of a total of 72 needed to instrument the complete scanner. SAM card bench tests (Fig. 8) demonstrate that both analog shaping paths function as designed. Our preliminary measurements with the SAM card and a small crystal array show that a 30 ns integration window is sufficient to preserve energy resolution at low count rates, and that the energy resolution does not degrade significantly as the count rate is raised to a level that corresponds to the rate of a human study (e.g. singles trigger rate of 20 Mcps for LaPET). Note that the 30 ns window is considerably shorter than the unshaped pulse width (Fig. 8) as we have currently in the LaPET scanner. At the highest count rates we may encounter, e.g. using a shorter-lived isotope than ¹⁸F, we may find that a shorter integration time is optimal. All MRB results reported below use SAM cards to shape the PMT pulses and an integration time of 28 ns.

¹As argued via simulation study in Ref. [11], WFS is expected to perform slightly better than a constant-fraction discriminator, even in the absence of pile-up effects and baseline offsets.

We have fabricated three prototype MRBs, two of which are fully assembled. One fully assembled MRB has been configured for the experimental setup described in Section III.

To verify the signal path providing the MRB's single-photon triggers, we recorded 10^5 events' trigger-ADC data for each of the 8 PMTs used in the single-MRB bench tests, processing the trigger data in software. Summing 4 successive samples from each PMT (which yields better results than the planned 3-sample design), we obtain 4.3% FWHM energy resolution (at 511 keV) for the reference PMT, indicating that the trigger's energy measurement is capable of cleanly separating the 511 keV peak from the Compton continuum. For the 5×5 array, the trigger's energy resolution (FWHM) is 13% (7.8%) before (after) crystal-by-crystal energy correction. Fig. 9 shows the trigger energy measurement as well as a 5×5 flood image using the trigger ADCs only. While we have no plan to identify crystals at the trigger level, the image shows that the trigger-level data are more than adequate for selecting the relevant DRS4 for readout and can potentially be used to reject, at the single-photon trigger level, patterns of light sharing inconsistent with emanating from a single crystal, e.g. for pile-up rejection. Forming time centroids of 4 successive trigger-ADC samples to measure the time difference between the reference PMT and the ring of 7 PMTs, we find 0.6 ns rms coincidence time resolution for the trigger path, which is sufficient to define the scanner's ≈ 6 ns coincidence gate. If desired, trigger timing can be further improved by fine-tuning resistor values in the analog shaping circuit: such tuning improved our testbench results (in this case re-sampling oscilloscope traces read from a SAM card to mimic the 100 MSPS ADCs) from 0.52 to 0.39 ns rms, using 3-sample timing centroids, while the simulated resolution at the design stage was 0.35 ns rms.

The DRS4 readout path on the MRB records oscilloscope-quality PMT waveforms, as intended. For the 5×5 crystal array, individual crystals are clearly distinguished (Fig. 10), and we measure an overall energy resolution of 5.3% FWHM for the array (after crystal-by-crystal energy correction), consistent with our group's results for this array using conventional electronics. The crystal-to-crystal variation in energy response of the array's 25 crystals has FWHM $\sim 5.5\%$. Therefore, we apply a crystal-dependent correction to account for the systematic variation in light output of each crystal in order to achieve the average energy resolution of 5.3%. At 3.5 GSPS, we measure 264 ps FWHM coincidence timing resolution overall for the array (with crystal-by-crystal timing offset) in coincidence with the cylindrical button, and 256 ps for the best crystal, which is approximately centered on the center PMT (Fig. 11). Taking 200 ps FWHM (previously measured using a DRS4 evaluation board at 5 GSPS) to be the timing resolution for two reference detectors in coincidence, the timing quoted above would correspond to 315 ps FWHM for two 5×5 arrays and 302 ps FWHM for the best crystal in coincidence with an identical crystal. At our minimum sampling rate of 2 GSPS, we measure 281 ps for the best crystal, and 286 ps overall, which would correspond (unfolding the same $\frac{200}{\sqrt{2}}$ ps for the reference detector) to coincidence timing resolutions of 343 ps and 352 ps respectively for the best crystal and for the 5×5 array.

To investigate further the dependence of timing resolution on sampling rate, we measured the "electronics-only" coincidence-timing resolution at 2, 3.5, 4, and 5 GSPS. Every DRS4 chip in our system uses one of its 8 channels to sample the 100 MHz global clock, so that

leading edges of the global clock provide a system-wide time reference. The time reported for a PMT waveform is leading-edge time with respect to a given edge of the 100 MHz global clock. So our coincidence-time measurement takes the form

$$\Delta t = (t_{\text{detector1}} - t_{\text{clk1}}) - (t_{\text{detector2}} - t_{\text{clk2}}).$$

As a measure of intrinsic electronics resolution, we measure the clock period $T_{\text{drsa}} \approx 10$ ns between two adjacent rising edges observed by DRS4 chip “a” and subtract the measurement by another DRS4 chip “b” of the interval T_{drsb} between the same two clock edges. We take the difference $\delta T \equiv T_{\text{drsa}} - T_{\text{drsb}}$ to be the MRB’s intrinsic timing resolution. Fig. 12 graphs $2.35 \times \text{rms}(\delta T)$ vs. DRS4 sample rate. Taking the purely instrumental contribution to the timing resolution to be 133 ps FWHM at 2 GSPS and 83.5 ps at 3.5 GSPS, we expect sampling at 2 GSPS instead of 3.5 GSPS to add a $\sqrt{133^2 - 83.5^2} = 104$ ps FWHM contribution to the coincidence-timing resolution, which we would expect to degrade our measured (at 3.5 GSPS) 264 ps to 284 ps (at 2 GSPS); this agrees well with the measured 5×5 resolution of 286 ps FWHM at 2 GSPS.

V. Discussion

Count-rate effects that lead to both deadtime and degradation of performance can be minimized with either passive pulse-shaping [13], [14] or active pulse-pile-up techniques [15], [16]. Our electronics design combines conventional analog pulse shaping with 2–5 GSPS WFS, which allows for a variety of pile-up rejection or correction techniques. Analog shaping cancels the exponential tail of each scintillation pulse, allowing nearby pulses to be more cleanly separated. WFS facilitates both subtraction of baseline offsets caused by earlier pulses and detection of overlap pulses whose shape does not match a single-pulse template. Fig. 2 shows an example of a pile-up pulse that is easily identifiable by comparing sampled waveforms with a template. While the DRS4 chip is capable of 5 GSPS sampling, we investigate the range 2–5 GSPS: sampling at 2 GSPS reduces readout time proportionally and extends the 1024-sample DRS4 memory (and consequently the allowable trigger latency) from 200 ns to 500 ns. To set the scale for relevant sampling rates, note that the risetime of the LaBr₃:5%Ce scintillator is 1 ns, while that of the Photonis XP20D0 PMT is 2.5 ns.

A typical single-photon trigger rate for human clinical studies with LaPET is 20 Mcps [10], while our target capability is up to 50 Mcps for tracers other than FDG. While 16- and 32-channel DRS4-based digitizer modules are now available commercially, reading out the scanner at these rates without significant deadtime requires a custom trigger scheme, analog pulse shaping, and a PMT-signal fanout scheme tailored to LaPET’s geometry. The custom trigger is needed at high count rates to avoid invoking the 3 μ s DRS4 readout process too often; pulse shaping is needed both to narrow the DRS4 readout window and to minimize pile-up effects; and the analog fanout scheme is needed both to map readout regions onto LaPET’s Anger-logic light-sharing scheme and to provide redundant DRS4 coverage to avoid deadtime during DRS4 readout. Since these functions require a custom circuit-board design, we chose to integrate DRS4-based sampling directly into our own circuit boards.

While an instrumental contribution of 133 ps may be acceptable in quadrature with a ≈ 315 ps detector resolution (degrading the timing resolution to 342 ps), we can reduce the instrumental effect with faster sampling, at a cost of reduced latency available for logic to trigger the DRS4 readout. Inter-chip DRS4 timing jitter can be improved somewhat by optimizing the component values used on the MRB for the DRS4's phase-locked loop [17]: an initial modification improved the 2 GSPS resolution from 133 ps to 124 ps. In addition, a new DRS4 aperture-jitter calibration algorithm has been reported [18], which dramatically improves the differential nonlinearity of DRS4's sample timing, and hence timing resolution. We coded into a simple Monte Carlo simulation the DRS4 artifact reported (and corrected via calibration) in Ref. [18] and found that our simulation reproduced the key features of Fig. 12, supporting the hypothesis that this artifact is a significant factor in our timing resolution at 2 GSPS. We anticipate that our implementing the improved DRS4 timing-calibration algorithm, once its details have been published [19], will eliminate the need to operate the MRB's DRS4 chips above 2 GSPS.

The MCU algorithm has been simulated in C and Verilog code and work is underway to prototype the MCU function for $\frac{2}{24}$ of the scanner using existing MRB hardware. (The partially assembled MRB has been configured to identify coincidences between the two fully assembled MRBs.) Once the concept has been validated, MCU circuit-board design will commence. To date, we have sent a 100 MHz clock and a 400 Mbps serial data stream over a 3-meter CAT7a cable between two MRBs, without error.

The Ethernet/UDP readout scheme was initially prototyped at high data rate (4×70 Mbps sustained rate) using 4 commercial FPGA evaluation boards, a 24/2-port 100/1000 Mbps commercial Ethernet switch, and a Linux PC, and has been used routinely for several months to read out a prototype MRB.

The data-acquisition software will write list-mode events compatible with existing reconstruction software and will re-use existing calibration algorithms that measure detector quantities. Further software development will be needed for event collection and for electronics calibration.

Reducing the readout window from 450 samples to 100 and moving the waveform-processing algorithms from computer software to FPGA firmware will reduce the readout event size from $\mathcal{O}(10$ kB) to $\mathcal{O}(0.1$ kB), allowing us to run at full speed. The goal is for the firmware to reduce each of the event's 14 PMT waveforms to $\mathcal{O}(10)$ bytes of summary data (amplitude, time, shape-quality flag). A lower bound is the 8-byte list-mode event size for the existing electronics, while an upper bound of $\mathcal{O}(100)$ bytes per PMT can be achieved by simply compressing the waveforms. For the complete scanner at its 50 Mcps maximum single-photon trigger rate, simulation studies estimate the average event readout rate per MRB to be 600 Hz. With even modest compression to 100 bytes per PMT, the Ethernet throughput per MRB would be a manageable 400 kB/s.

Once we have moved the processing (or at least preprocessing) of DRS4 waveforms from software into FPGA firmware and adapted our present benchtop tests to find coincidences between two separate MRBs (with a third MRB serving to prototype the MCU function), our

next milestone will be to use these three boards to read out two modules of the LaPET scanner. Finally, a dedicated MCU board and a production run of MRB circuit boards will be fabricated to instrument a larger fraction of the scanner.

VI. Summary

We have demonstrated that WFS retains the intrinsic precision of timing information of the scintillation signal, and have achieved 315 ps (FWHM coincidence timing resolution) for a test array of LaBr₃ crystals with a new design of electronics. These electronics can be scaled to our prototype LaPET scanner, and should enable us to achieve similar timing performance. We currently experience some losses in timing performance with LaPET, which uses more conventional electronics, so that in practice we achieve a system timing resolution between 375–420 ps, depending on the count rate of the study. Some care will be needed to optimize both the sampling rate and the number of samples read out, e.g. for baseline correction, for energy measurement, and for pile-up detection. One challenge in scaling from a small detector on a benchtop to a whole-body TOF PET scanner is the control of channel-to-channel gain and timing offsets. A key challenge in operating a whole-body TOF PET scanner at high count rate (20 ~ 50 Mcps single-photon trigger rate) is to preserve excellent timing, energy, and position resolution in the presence of pile-up interactions. Our electronics design addresses these challenges. By processing individual PMT signals digitally, we maximize available handles for controlling calibration effects. Using high-speed waveform sampling facilitates our handling baseline offsets and pile-up pulses at count rates pertinent for patient imaging. We are currently testing prototypes of the circuit boards with which we will re-instrument the LaPET whole-body prototype scanner. While the modules we have designed are tailored to LaPET's geometry, the concept can be readily adapted to other detector configurations.

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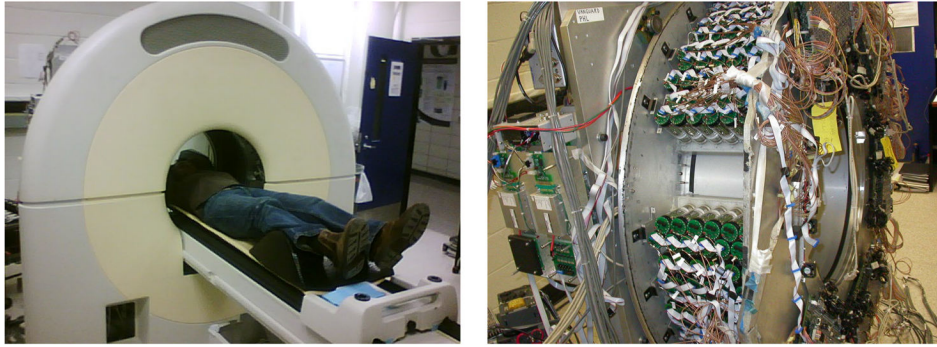


Fig. 1. LaPET's 38880 crystals are separated azimuthally into 24 detector modules and imaged by 432 PMTs (51 mm ϕ). The new electronics obey the same 24-fold symmetry, sharing edge PMT data between neighboring sectors.

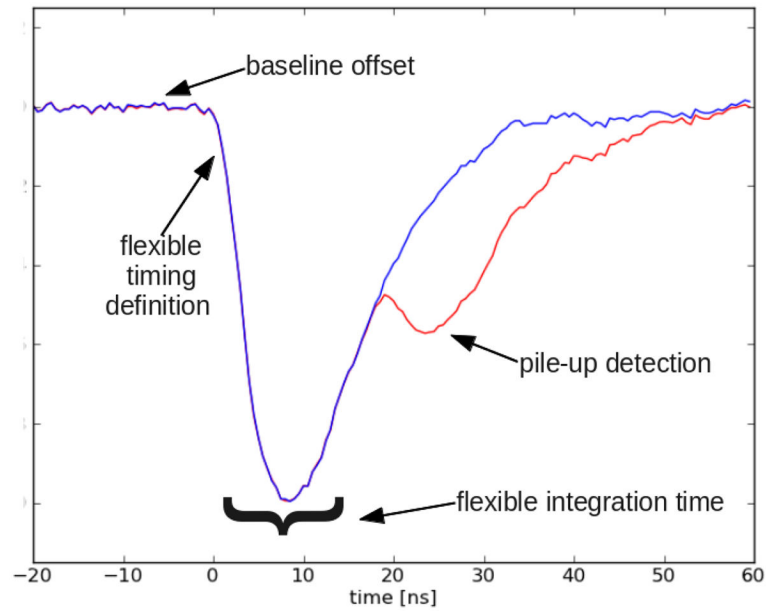


Fig. 2.

This annotated pulse illustrates the flexibility of 2 GSPS WFS for TOF PET readout. WFS enables programmable definition of leading-edge timing and of integrated light collected by PMT, from a single data stream. Digital baseline restoration and shape-based pile-up detection help to preserve performance at high count rates. Integration time is programmable and may be adapted as a function of count rate. Waveform processing and system design are described in Section II.

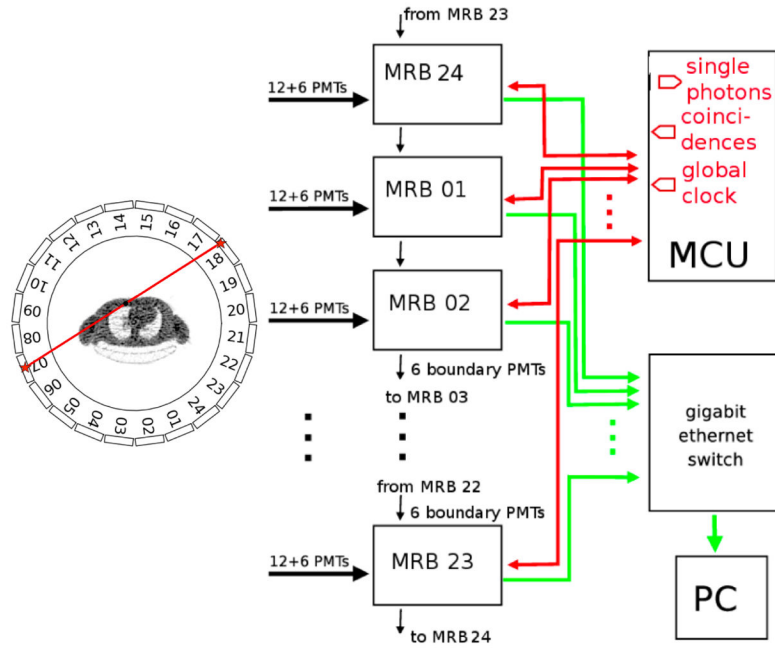


Fig. 3. Waveform-sampling electronics consist of 24 Module Readout Boards (MRB). MRB/PC link uses 100/1000 Mbps Ethernet for data fan-in of accepted pairs. Coincidence logic is purely digital, using Category 7a twisted-pair cable for synchronous data link between each MRB and Master Coincidence Unit. Each MRB hosts three SAM cards, as shown in Fig. 5.

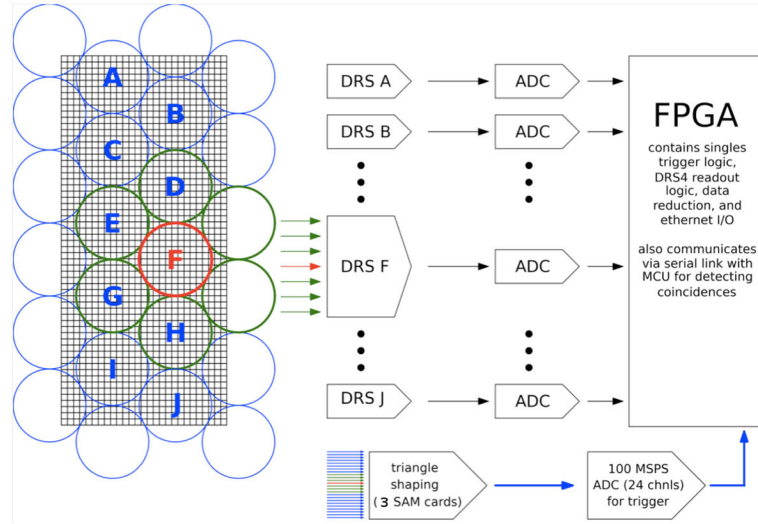


Fig. 4.

Block diagram of Module Readout Board (MRB). Letters **A** through **J** indicate PMTs on which trigger zones are centered. Scintillation light from the 7 PMTs (only 6 PMTs for zones **A** and **J**) in each zone is collected by 7 analog inputs of the corresponding DRS4 chip. (An eighth analog input for each DRS4 chip records a reference clock for timing alignment.) A separate data path digitizes all 24 PMT signals at 100 MSPS for FPGA-based triggering. The left- and right-hand columns of PMTs are shared with adjacent MRBs. SAM-shaped signals from the right-hand column of PMTs are copied by the MRB to the adjacent (downstream) MRB. Signals from the left-hand column of PMTs are received from the adjacent (upstream) MRB, after having been shaped by the upstream MRB's SAM cards.

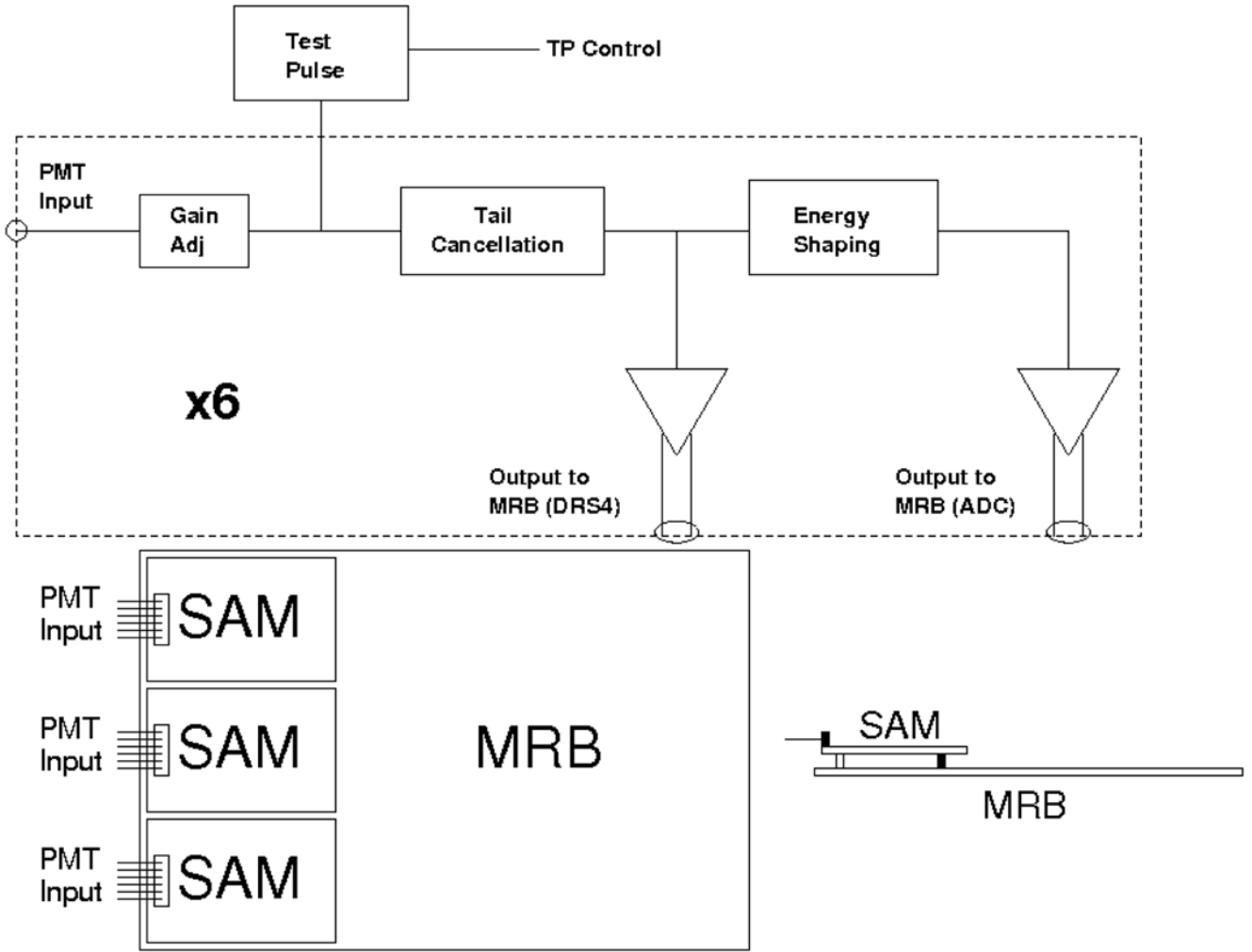


Fig. 5. The upper figure shows a block diagram of $\frac{1}{6}$ of a shaper/analog mezzanine (SAM) card. Each SAM card receives and shapes six PMT signals. Each MRB requires three SAM cards (18 PMT inputs); the MRB sends copies of six of these 18 inputs to the adjacent MRB, so that each MRB processes all 24 PMT signals with which a given detector module's scintillation light is collected. The lower-left figure shows three SAM cards attached to one MRB. The lower-right figure is an elevation view indicating the SAM cards' mounting onto an MRB.

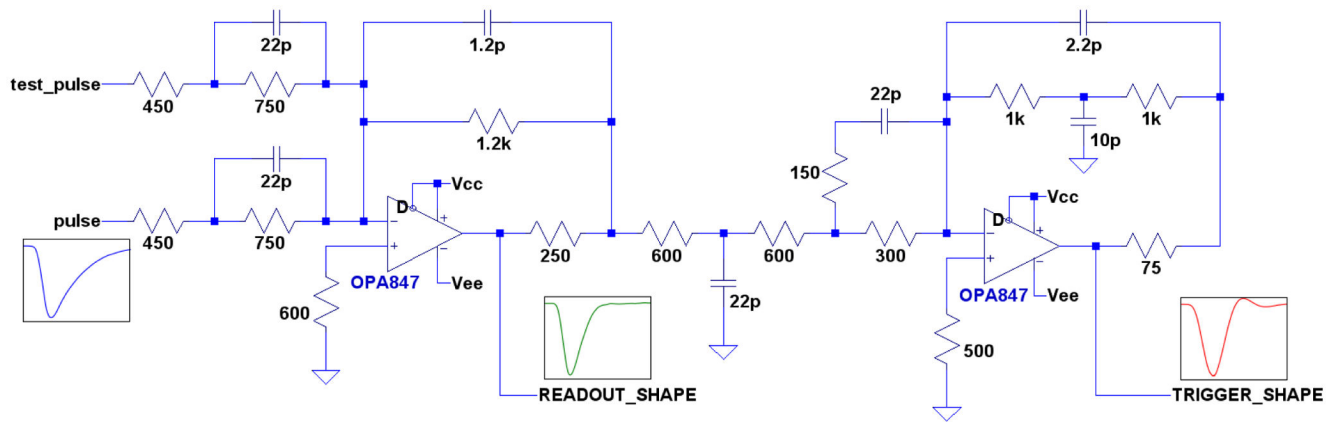


Fig. 6.
Schematic diagram for one PMT channel's shaping, as implemented on SAM card.

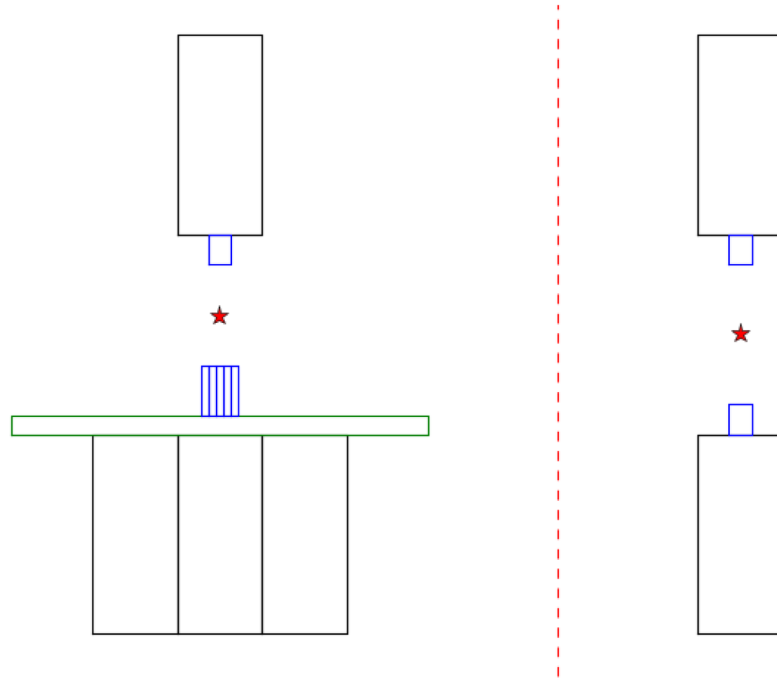


Fig. 7.

The left figure shows a side view of the experimental setup used for testing a single MRB. A 5×5 array of $4 \times 4 \times 30 \text{ mm}^3$ $\text{LaBr}_3:5\% \text{Ce}$ crystals is centered on a hexagonal arrangement of seven 51-mm Photonis XP20D0 PMTs, coupled through a light guide of thickness 11.3 mm. The center PMT corresponds to the PMT labeled “C” in Fig. 4. The reference detector is a $\phi 14 \text{ mm} \times 18 \text{ mm}$ $\text{LaBr}_3:5\% \text{Ce}$ cylinder centered on a single Photonis XP20D0 PMT. The reference PMT faces the ring from above, with the ^{22}Na positron source placed between the array and the cylinder. The right figure shows the experimental setup used to produce Table I: two reference detectors are placed in coincidence.

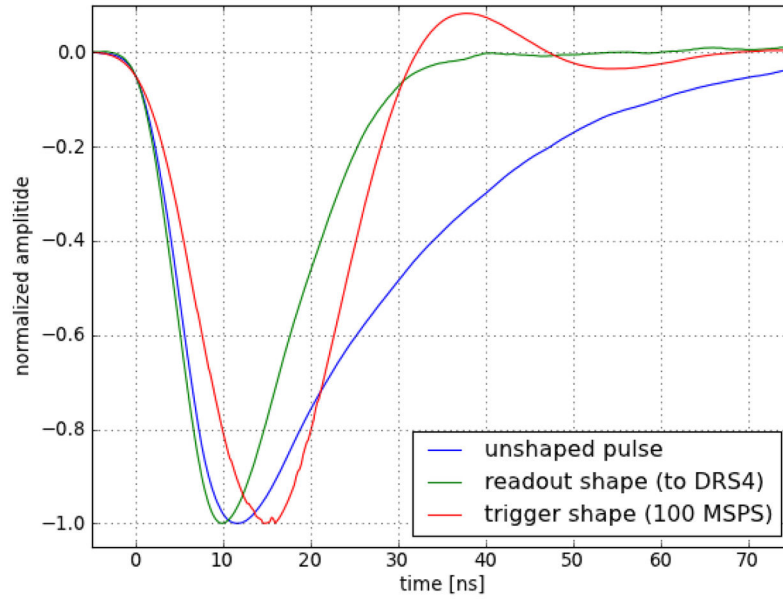


Fig. 8. SAM card input and filtered outputs. PMT pulse (blue curve) recorded by oscilloscope, before shaping by SAM card. Green curve shows tail cancellation that reduces pile-up effects. Red curve shows pulse shaped for 100 MSPS trigger processing. The “readout shape” (green), sent to DRS4 for 2 GSPS sampling, preserves fast leading-edge timing while canceling slow tail of PMT pulse. The “trigger shape” (red) makes rise and fall times roughly equal, so that trigger ADC and FPGA logic can determine coarse energy and timing (via centroid algorithm) for coincidence detection, to select DRS4 chips for readout.

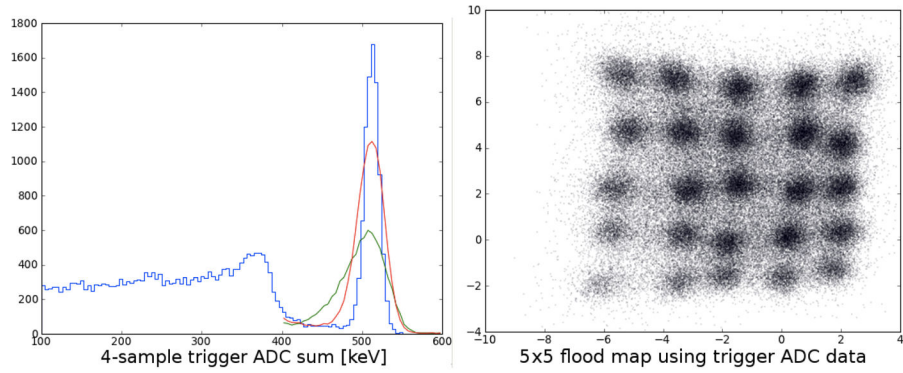


Fig. 9.

Using 100 MSPS trigger ADCs only. The left graph shows energy spectrum from cylindrical reference button (blue histogram), from 5×5 array (green curve), and from 5×5 array with crystal-by-crystal energy correction (red curve). The right graph shows a flood image from the 5×5 crystal array. Energy resolution of trigger data path is sufficient to separate photopeak from scattered photons. While much cleaner results than these are obtained from the full DRS4-based readout path, we show the coarser trigger-path results here to illustrate the information available to the FPGA-based digital trigger.

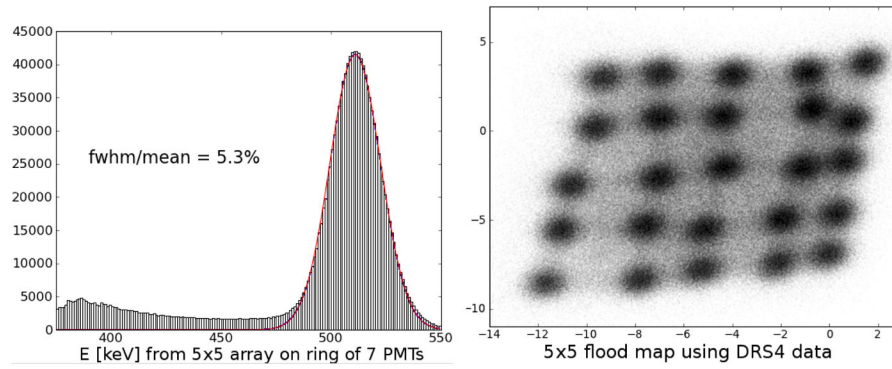


Fig. 10.

Using DRS4 readout path: 511 keV energy response for 5×5 crystal array (left), and flood image (right) showing that individual crystals are clearly identified by Anger-encoded position. After applying a crystal-by-crystal energy offset, the average energy resolution for the 5×5 array is 5.3% FWHM at 511 keV.

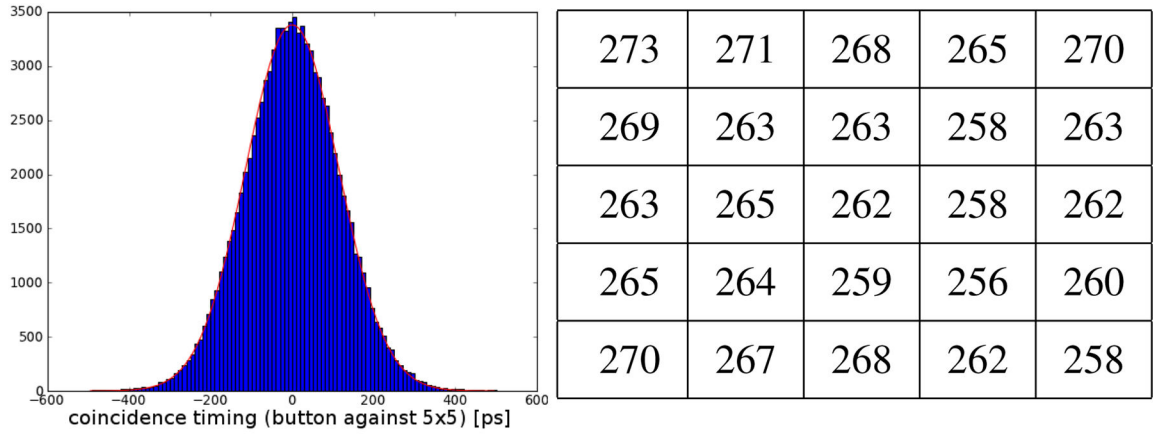


Fig. 11.

(Left) Coincidence timing distribution for 5×5 crystal array in coincidence with cylindrical button, sampled by MRB at 3.5 GSPS sampling rate. (Right) Crystal-by-crystal timing resolution (ps FWHM), with cylindrical button mounted on single PMT as a reference detector. Coincidence timing resolution is 264 ps FWHM overall (after applying crystal-by-crystal timing offset) and 256 ps for the best crystal, which is approximately centered on the center PMT.

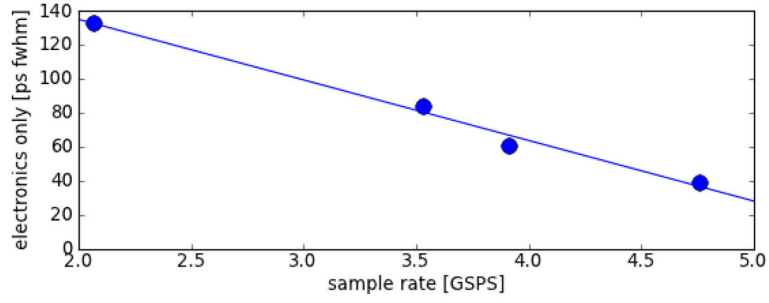


Fig. 12.

Measurement of the intrinsic electronics resolution for coincidence timing measured by the MRB at present. Two DRS4 chips observe copies of the same 100 MHz clock. Using each DRS4 chip, we measure the period of the clock, by applying time-pickoff algorithm to two adjacent leading edges. We then subtract the periods measured by the two DRS4 chips. The graph shows 2.35 times the rms of that distribution, for four different DRS4 sampling rates. The measured values (FWHM) are 133 ps at 2 GSPS, 83.5 ps at 3.5 GSPS, and 39 ps at 5 GSPS.

TABLE I

Coincidence time resolution (FWHM) measured using conventional electronics, using Agilent DC271 digitizer board (2 GSPS), and using DRS4 evaluation board (5 GSPS).

NIM/CAMAC	digitizer board	DRS4 eval board
225 ± 5 ps	210 ± 5 ps	199 ± 5 ps