A Field-Programmable Analog Array Development Platform for Vestibular Prosthesis Signal Processing

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Abstract

We report on a vestibular prosthesis signal processor realized using an experimental field programmable analog array (FPAA). Completing signal processing functions in the analog domain, the processor is designed to help replace a malfunctioning inner ear sensory organ, a semicircular canal. Relying on angular head motion detected by an inertial sensor, the signal processor maps angular velocity into meaningful control signals to drive a current stimulator. To demonstrate biphasic pulse control a 1 kΩ resistive load was placed across an H-bridge circuit. When connected to a 2.4 V supply, a biphasic current of 100 μA was maintained at stimulation frequencies from 50–350 Hz, pulsewidths from 25–400 μsec, and interphase gaps ranging from 25–250 sec.

Keywords

Analog signal processing; biphasic stimulation; field programmable analog array (FPAA); vestibular prosthesis

I. Introduction

The vestibular system is responsible for establishing our sense of body orientation, maintaining balance, and stabilizing gaze [1]. Our natural peripheral vestibular system consists of three angular and two linear motion sensors located within the inner ear: the semi-circular canals (SCCs) and the otolith organs, respectively. The central nervous system (CNS) processes motion information sent by the peripheral sensors through the vestibular nerves. Defects in the sensors, vestibular nerves, or the CNS due to disease or injury cause problematic vestibular sensation [2]. Individuals suffering from loss of peripheral vestibular sensation could benefit greatly from a vestibular prosthesis. This device replaces the malfunctioning vestibular sensors with microfabricated sensors and stimulates the vestibular nerves with current pulses through interface circuitry and an implanted electrode array [3]. Similar to natural SCC neural coding for angular head rotation, the interface circuitry should encode the angular head velocity into a pulse rate [Fig. 1(a)]. A series of vestibular prostheses subsystems and prototypes have demonstrated promising results in overcoming

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peripheral vestibular loss in animal models [4]–[7]. Complementing these efforts is progress in low-power custom integrated interface circuitry [8]–[10], as well as integrating interface circuitry with the sensor [11].

While promising, in-vivo studies indicate a pressing need for optimizing current stimulation paradigms as well as reducing spurious stimulation [12]. Thus, refining and optimizing encoding of angular velocity, and processing of angular velocity signals, is an essential step to achieving the clinical efficacy of a vestibular prosthesis. To investigate a potential platform for angular velocity encoding, this paper explores an experimental field programmable analog array (FPAA) development platform [13]. Accomplished completely in the analog domain, the signal processing circuitry generates a non-linear signal that codes angular velocity into a pulse rate for a single SCC [Fig. 1(b)]. Producing two out-of-phase clocks, the circuit can control all of the timing features of a biphasic pulse and ultimately drive a current stimulator for targeted activation of vestibular nerve fibers.

The rest of this paper is organized as follows. In Section II, we begin with a brief description of the FPAA and the procedure for realizing circuitry on the FPAA. In Section III, we provide the design specifications of the vestibular signal processor followed by a detailed description of the circuit blocks comprising the signal processor. Measurement and test results are discussed in Section IV. Finally, in Section V, we conclude by considering additional aspects of utilizing the FPAA platform such as scaling to a multichannel prosthesis and implementing alternative signal processing algorithms.

II. FPAA Architecture

The FPAA used is an experimental chip; the reconfigurable analog signal processor (RASP) 2.8 designed by the Integrated Computational Electronics Laboratory, Georgia Institute of Technology [13]. Although a commercial FPAA could also serve as a development platform [14], we chose the RASP 2.8 since its floating gate architecture provides greater functionality through the ability to program the switches with variable impedance. In addition, by operating the circuitry in weak inversion, considerable power saving can potentially be realized.

Fabricated with the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm 2P3M CMOS process and operating with a 2.4 V power supply, the RASP 2.8 is comprised of computational analog blocks (CABs) and an interconnect network (Fig. 2). A total of 32 CABs (CAB1 or CAB2) consist of circuit elements and blocks at different levels of complexity. Circuit elements/blocks such as transconductance amplifiers (OTAs), multi-input floating gates, nFET/pFET transistors, floating capacitors, Gilbert Multipliers, and floating-gate current mirrors are distributed among CAB1 and CAB2 [Fig. 2(b)]. The role of the interconnect network, which consists of switches (floating-gate pFETs) and interconnect lines, is to sensitize connections between CAB elements/blocks. In addition, global interconnect lines are also connected to input/output pins for voltage/current measurements.

To implement a particular circuit on the FPAA, connections are made by programming the necessary switches in the interconnect network. An automated placement and routing tool, the generic reconfigurable array specification and programming environment (GRASPER),

determines which switches to activate. GRASPER converts a user-generated SPICE netlist describing the circuit into a netlist of switches [13]. To program a floating-gate pFET, negative charge is injected onto the floating-gate of the transistor. The amount of the charge trapped at the floating-gate affects the effective gate potential of the transistor and thus directly controls the conductance of the device. Briefly, the charge injection mechanism is accomplished by applying a high potential difference (~15 V) between the drain and the source terminals. As a result, a programming current, I_{prog}, passes across the two terminals. I_{prog} can be varied between 1 nA-32 μA, with higher causing more negative charge to be trapped at the floating-gate. The communication between the PC and the FPAA is achieved through a microprocessor-based board.

III. Signal Processor

For each SCC, the encoding of angular velocity into a pulse rate is based on a relationship validated in animal models [4]. This non-linear relationship between the angular velocity and the firing rate is represented as

$$f_{stim} = 200 + 150 \quad tanh\left(\frac{\omega}{500/3}\right) \quad (1)$$

where ω is the angular velocity in °/sec, and is the pulse rate in pulses per second (pps). The offset value in the equation conveys a baseline pulse rate corresponding to zero angular velocity (Fig. 3).

A biphasic current scheme [Fig. 3 (inset)] is generated to prevent any charge accumulation at the tissue site that can cause long-term adverse effects [15]. The amplitude and pulse duration (PD) of the cathodic pulse determines how much charge is delivered to the neural tissue. Similarly, the PD and the amplitude of the anodic pulse determine how much charge is returned from the tissue. The interphase gap (IPG) separates the two pulse periods to ensure the firing of the neuron. This control is essential for optimizing stimulus waveforms to reduce threshold, improve spatial selectivity and reduce spurious stimulation.

The signal processor provides the user with the freedom to control all timing features of a biphasic current pulse. The signal processor senses an analog voltage output from an inertial sensor, $V_{gyro,out}$, and converts this voltage into two out-of-phase clocks (Clock 1 and Clock 2) each with a frequency of f_{stim}. In turn, Clock 1 and Clock 2 serve as control signals for a stimulator. The respective pulse duration of the two clocks determine the cathodic and the anodic PD of the biphasic current waveform. The phase difference between Clock 1 and Clock 2, less the PD, determines an IPG. The three blocks constituting the signal processor are the voltage-to-current converter block, the current-to-frequency converter block, and the clock generation block (Fig. 4). We describe each block in detail below.

1) Voltage-to-Current Converter Block [Fig. 4(a), (d)]

The first block of the signal processor transfers the analog voltage output from an inertial sensor, gyroscope, into a current signal [Fig. 4(a)]. As indicated in (1), the stimulation frequency is related to angular velocity through a hyperbolic tangent function. In the spirit of

biomorphic circuit design, we followed an integrate-and-fire neuron scheme utilizing a floating-gate OTA (FGOTA) [16]. In the sub-threshold region, the output current, I_{out}, of the FGOTA is related to its differential input voltage, $V_p - V_n$, through a *tanh* function

$$I_{out} = I_{bias} \cdot tanh\left(\frac{\kappa\alpha\left(V_p - V_n\right)}{2U_T}\right) \quad (2)$$

where κ is a constant relating the surface potential of a transistor to its gate voltage, α is the attenuation factor due to the capacitive divider at the input differential pair, I_{bias} is the bias current which determines the region of operation of the transistors, and U_T is the thermal voltage. Thus, an FGOTA is at the core of the voltage-to-current converter block.

In our implementation, $V_{gyro,out}$, the output of the gyroscope, is connected to V_n input of the FGOTA. V_p is tied to $V_{gyro,out}$, the reference voltage for the gyroscope. To ensure that I_{out} is positive, M1, drawing I_1 from the output node of the FGOTA, adds a DC offset. The current I_1 is controlled by $V_{control}$ and I_2 is the DC shifted version of $-I_{out}$. To ensure that I_2 maintains f_{stim} within the 50–350 Hz interval, I_2 is scaled and mirrored using a mismatched current mirror circuit. The mirror circuit is formed by two floating-gate pFETs, M2 and M3, thereby creating I_3. Since device sizes are fixed in the FPAA, the mismatch between M2 and M3 is controlled by programming varying amounts of charges (Q2 and Q3) onto their respective floating gates. For the I_{prog} values of M2 and M3 shown in Fig. 4, the I_2/I_3 ratio is measured to be ~80. The minimum level of I_3 is controlled by $V_{control}$. By adjusting $V_{gyro,ref}$ an offset can be added to $V_{gyro,out}$. This serves to translate the I_3 along the x-axis of the I_3 versus $V_{gyro,out}$ curve.

2) Current-to-Frequency Converter and Clock Generator Block [Fig. 4(b), (c)]

Since these two blocks function in an integrated fashion to provide control signals for a current stimulator, we begin by describing the main signals of interest followed by a detailed description of each block. The main output of the current-to-frequency converter block is V_{PT}, a frequency modulated pulse train with an adjustable pulse-width. Fig. 5 depicts the duration that V_{PT} is high and low, t_{high} and t_{low} respectively. The rising edge V_{PT} triggers Clock 1 in the subsequent clock generation block. Similarly, the rising edge of $\overline{V_{PT}}$ triggers Clock 2. As a result, the frequency of V_{PT} determines the pulse rate, f_{stim}. The PD of the target biphasic pulse is controlled in the clock generation block. The IPG is determined by the delay between Clock 1 and Clock 2, t_{high}, less the PD.

a) Current-to-Frequency Converter Block [Fig. 4(b)]

The circuit is a modified version of a self-resetting neuron circuit [17] where the main signal of interest is V_{PT}. The bias voltage V_{bias2} controls the discharge current I_8 through M8 and M9 when M9 is on. As a result V_{bias2} controls t_{high}. Alternatively, t_{low} is affected by I_3 since it controls how fast *C1* (4 pF) and *C2* (2 pF) are charged up. Another parameter affecting t_{high} is V_{bias1}, as it determines how fast V_{PT} makes the low to high transition. The relationship between f_{stim} and I_3 is

$$f_{stim} = \frac{1}{t_{high} + t_{low}} = \left(\frac{I_3}{C_2 V_{DD}}\right)\left(1 - \frac{I_3}{I_8}\right) \quad (3)$$

For $t \gg t_{high}$, it can be shown that

$$f_{stim} \approx \frac{1}{t_{low}} = \frac{I_3}{C_2 V_{DD}}. \quad (4)$$

The linear relationship between f_{stim} and I_3 enables I_3 to have the same dependence on angular velocity as f_{stim} expressed in (1). When examining (3) it appears that at high pulse rates the linear assumption may be inaccurate. Consider an f_{stim} of 450 pps and $t_{low} = 10(t_{high})$. Thus, 200 μs may be dedicated to the PD and IPG of a biphasic pulse. Given that most PDs are 100–200 μ s and that the IPG does not affect response to electrical stimulation of vestibular nerve fibers [12], it is reasonable to assume that the linearity assumption would not be grossly violated. However if necessary, V_{bias2} may be dynamically controlled through a feedback circuit to maintain a small rending the term negligible. As a result the needed linearity can be realized.

b) Clock Generator Block [Fig. 4(c)]—Two fully digital clock generation circuits constitute this block generating Clock 1 and Clock 2, each with a frequency of f_{stim}. The goal of each circuit is to create a pulse at the rising edge of its respective input and set the duration of each pulse [18]. To give the two clocks a phase difference, Clock 1 is generated directly from the pulse train obtained at the previous block, V_{PT}. Clock 2 is generated from the inverse of that pulse train, $\overline{V_{PT}}$. When V_{PT} is low, Clock 1 is also low. During that period, M10 keeps V_X high. When makes a low-to-high transition, because M11 allows current flow, a discharge path is created that decreases V_X. During that phase, Clock 1 is at high. When V_X reaches the low value for the AND gate, Clock 1 also goes down to low. At that instant, M11 turns off, disconnecting the discharge path. The pulse-width of Clock 1 is related to how fast V_X goes down to zero, which is effectively controlled by V_{pulse1}. The circuit for Clock 2 operates similarly and the pulse duration is controlled by V_{pulse2}.

IV. Measurement Results

To observe the pulse rate as a function of angular velocity, the signal processor was driven by a commercial gyroscope. Rotated about its z-axis, the gyroscope exhibited a sensitivity of 2 mV/°/s over a full-scale range of ±500 °/s, with a reference voltage of 1.35 V (InvenSense Inc., Sunnyvale, CA). Using a single-axis rate table (Ideal Aerosmith LLC, Pittsburgh, PA), the gyroscope was subjected to 33 sinusoidal rotations with angular velocity magnitudes that varied between 0°/sec and 500°/sec in 15°/sec increments. Pulse rate data was captured from an oscilloscope and processed using MATLAB software (The Math-Works Inc., Natick, MA) running on a PC. Discrete angular velocities were required since we were limited by the data transfer rate between the oscilloscope and the PC. Approximately 75 data points were obtained for each rotation. To find the pulse rate in the positive direction, the three maximum frequency values were averaged. Similarly, to find the pulse rate in the negative direction, the three minimum frequency values were averaged.

Fig. 6 compares the target and experimental versus angular velocity. To better understand the difference between the two curves we consider the three aspects of the curve relating pulse rate to angular velocity; the steepness, the baseline frequency (the frequency corresponding to zero angular velocity in the plane of measurement), and the frequency range.

The steepness of the output curve is controlled by the transconductance of the FGOTA (voltage-to-current converter). To characterize the linearity and the transconductance of the FGOTA, we varied V_{out} from 0–2.4 V. For a bias current of, $I_{bias} = 3$ nA, the measured linear range for 5% degradation in transconductance of the FGOTA is between 0.31 V and 0.37 V, when V_{out} ranges between 0.27 V and 2.13 V. The data reveals that the transconductance of the FGOTA is only slightly dependent on V_{out} and is ~3 nS. The transconductance of the FGOTA is mainly dependent on the κ_{eff} [$\kappa * a$ term in (2)]. This is verified by a series of curves illustrating f_{stim} versus angular velocity for a range of κ_{eff} from 0.05 to 0.15 (Fig. 6). As expected from (2), the steepness of the curve increases with κ_{eff}. At $\kappa_{eff} = 0.05$ the expected curve closely matches the experimental curve. Yet, the κ_{eff} corresponding to the target curve is around 3 times larger than that (~0.15). There are two reasons why the κ_{eff} is bound to small values. First, the κ of a transistor, in the FGOTA, in the weak inversion region is smaller than when in the strong inversion region. Second, the capacitive divider at the floating gates of the FGOTA reduces a to significantly low values, slightly lower than 1/9 considering the gate capacitances of M2 and M3.

The second aspect is the baseline frequency, $f_{baseline}$. This frequency is effectively controlled by the DC value, I_1, added to I_{out} in Fig. 4(a). By changing (controlled by), the difference between the baseline frequencies of the two curves ($f_{baseline} = 19.5$ pps in Fig. 6) can be adjusted.

The last aspect we consider is the frequency range. This is controlled by three factors: the capacitance $C2$ (3), the bias current of the FGOTA, I_{bias}, and the current ratio of the mismatched current mirror, I_3/I_2. By varying any of these, the experimental curve can be adjusted to maintain within the desired stimulation frequency range.

Fig. 7. summarizes critical outputs from the signal processor blocks. Fig. 7(a) illustrates the non-linear I_3 response to $V_{gyro,out}$ generated by the voltage-to-current converter block. In Fig. 7(b), a linear f_{stim} versus I_3 response is exhibited by the current-to-frequency converter block. And finally, in Fig. 7(c), the triggering of Clock 1 by the rising edge of V_{PT} is shown.

To demonstrate biphasic pulse control a 1 kΩ resistive load was placed across an H-bridge circuit (Fig. 8). Although this is voltage-based stimulation, it served to illustrate the ability of the signal processor to accurately control biphasic pulses ultimately generated by a current stimulator. When connected to a 2.4 V supply, a current level of 100 μA was obtained. Pulse durations of anodic and cathodic phases between 25–400 μs, and an inter-phase gap between 25–250 μs were observed. Hence all timing segments of a biphasic pulse can be controlled well within the necessary ranges.

To appreciate the power demands of the signal processor circuitry, estimates are reported for a 350 Hz pulse rate with a 100 μsec PD. The voltage-to-current converter block consumes

0.48 μW. The combined power required by the current-to-frequency converter block and the clock generator block is mostly due to the dynamic power consumed at the digital gates. Ignoring any short circuit or leakage currents, and assuming a line capacitance of 2 pF for each interconnect line [13], the total power consumption of these is ~44 nW. The necessary switch circuitry consumes an additional 16.8 μW resulting in 18.324 μW. The use of a 14-bit AD5380 DAC (Analog Devices, Inc., Norwood, MA) for setting the six bias voltages consumes 12 mW max. Although the off-chip DAC facilitated circuit prototyping, in practice such bias voltages would be generated on the FPAA. Schlottmann and Hasler illustrate a method for creating voltage references through trapping different amount of charges at the floating gates of a FGOTA [19]. Precisely controllable ($< \pm$ mV) bias voltages from rail-to-rail (0–2.4 V) can be generated and will consume very little power, on the order of W.

V. Discussion

The goal of this work was to implement a vestibular signal processor on a reconfigurable FPAA platform. While we employed a hyperbolic tangent encoding angular velocity to pulse-rate, ongoing studies suggest there are alternative models for mapping between angular velocity to pulse rate [7], [12], [20]. The reconfigurability of the FPAA is an attractive feature for rapid mapping of modifications. Changes may be made to the voltage-to-current converter block alone, while retaining the existing current-to-frequency and clock generation blocks respectively. For example, to efficiently approximate the mean operating characteristics of vestibular nerve afferent fibers, a piece-wise linear (PWL) velocity-to-pulse rate mapping may be employed [12]. To realize this encoding the voltage-to-current converter block could consist of (1) an FGOTA that performs a nearly linear conversion of $V_{gyro,out}$ to I_{out}; (2) an nMOS, to add a DC offset and thereby ensure I_{out} positive for all $V_{gyro,out}$; (3) a current-mode circuit realizing a PWL function [21], [22]; and (4) a current mirror to scale up/down the current output from the PWL circuit.

In addition to the benefit of reconfigurability, the FPAA presents a power advantage. We estimate that when bias voltages are generated on-chip, less than 20 μW will be consumed for a single canal system. As a comparison, Constandinou *et al.* predict a power consumption value of 48.84 μW, based on the simulation results of their semicircular canal processor ASIC [9]. Thus with respect to power the FPAA approach is attractive.

Another important consideration is signal processing for multi-canal system. Using the RASP 2.8 chip, a single-canal signal processor consumes nearly 70% of the chip area but not necessarily 70% of the circuitry. Because CABs include only nFETs or pFETs, it was essential to use circuit elements distally located on the chip. Thus interconnect lines were consumed rendering functional CABs unavailable. Interconnect was also consumed for testing purposes to probe signals by routing them to input/output pins. We estimate that at best a two-canal system could be realized with the RASP 2.8.

To effectively meet the needs for a vestibular signal processor, a future version of the RASP FPAA could be modified in the following ways. First, to better approach steep curves for the velocity-to-pulse rate mapping, additional FGOTAs with different κ_{eff}'s could be provided.

This can be assured by the use of different capacitive divider ratios at the floating gates of the input transistors of the new FGOTAs. Second, when considering a PWL mapping, a wide-range FGOTA could be added to enable a linear $V_{gyro,out}$ to I_{out} conversion. Third, to prevent inefficient interconnect usage, CABs could be altered internally to prevent distant connections. It could be advantageous to consider a more natural interconnection between the CABs such as in a lattice network [23].

VI. Conclusion

In this work we explored an FPAA-based vestibular signal processor. We demonstrated a single-canal system in which a voltage output from a rotated gyroscope was encoded into frequency modulated control signals for a current stimulator. We also discussed some limitations in scaling the RASP 2.8 FPAA to a multi-canal system. More broadly, this implementation demonstrated the utility of processing signals in the analog domain. Parallel to vestibular prostheses, low-power signal processing approaches for cochlear prostheses explore analog signal processing [24], [25]. Furthermore, while a custom ASIC yields a smaller footprint of ~1 mm^2 [9], than the RASP 2.8 FPAA of ~166 cm^2, the option for reconfigurability is advantageous. Serving as a development platform, an FPAA enables rapid revision of encoding schemes during testing in animal models. Given the need to optimize the tradeoff between dynamic range and axis misalignment (unintended stimulation), it may be necessary to adjust mapping and baseline pulse rate on an individual basis. Thus our proposed signal processing development platform may provide a measure of the programmability space needed for a fully implantable device.

In summary, through continued innovative and collaborative efforts along the lines of optimizing encoding, low-power sensing and circuitry, as well as enhanced stimulating electrode design for focused stimulation, an attractive therapeutic option may soon be available for individuals suffering from debilitating bilateral vestibular hypofunction.

Acknowledgment

Biography

Hakan Töreyin (S'11) received the B.S. degree in electrical and electronics engineering from Middle East Technical University, Ankara, Turkey, and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, in 2007 and 2008, respectively.

Currently, he is working toward the Ph.D. degree at the Georgia Institute of Technology. His research interests include interface circuit design for biomedical devices and low-power analog circuits design.

Pamela Bhatti (M'05) received the B.S. degree in engineering science (bioengineering) from the University of California, Berkeley, the M.S. degree in electrical engineering from the University of Washington, Seattle, and the Ph.D. degree in electrical engineering, with an emphasis on micro-electro mechanical systems (MEMS), from the University of Michigan, Ann Arbor, in 1989, 1993, and 2006, respectively.

She is an Assistant Professor in the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta. Before completing her Ph.D. degree, she researched the detection of breast cancer with ultrasound imaging at the University of Michigan's Department of Radiology (1997–1999). Her industry experience includes embedded systems software development at Microware Corporation, Des Moines, IA (1996–1997), local operating network applications development and customer support at Motorola Semiconductor, Austin, TX (1994–1995), and research and fabrication of controlled-release drug delivery systems at Alza Corporation, Palo Alto, CA (1986–1990).

Dr. Bhatti received the NSF Career Award in 2011. Committed to translating technology to the clinical setting, she is a KL2 Scholar with the Atlanta Clinical and Translations Sciences Institute.

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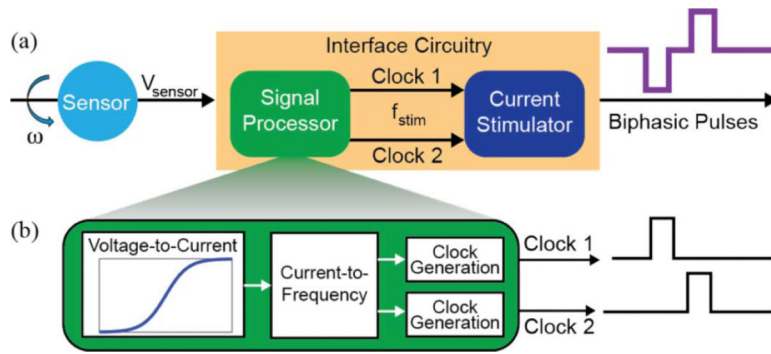
Fig. 1.
Single canal vestibular prosthesis system diagram. (a) The interface circuitry consists of a signal processor and a current stimulator. (b) Circuit blocks constituting the signal processor. Operating in the analog domain, the voltage-to-current block encodes angular velocity as a drive current with a nonlinear transformation. The current-to-frequency block generates voltage pulses at a rate of f_{stim}, the desired pulse rate. Two identical clock generation blocks produce digital control signals for a current stimulator to generate charge-balanced biphasic current pulses.
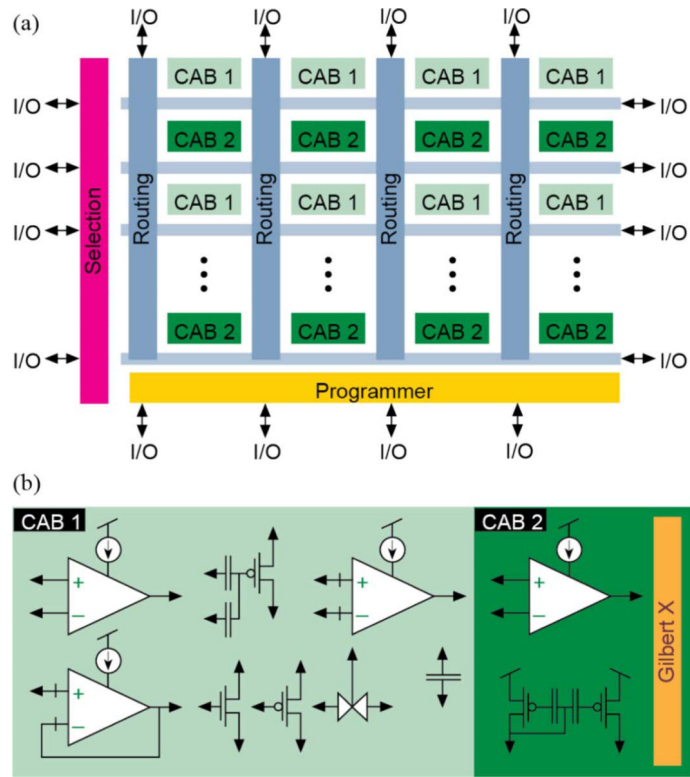
Fig. 2.
Floating-gate FPAA architecture. (a) The FPAA consists of an 8×4 matrix of computational analog blocks (CABs) interconnected through crossbar networks. (b) CAB1 contains three operational transconductance amplifiers (OTAs), three floating capacitors (500 fF), two multi-input floating gates, a voltage buffer, a transmission gate, and nMOS/pMOS transistor arrays. CAB2 has two folded Gilbert multipliers and a floating gate current mirror, and a wide-linear-range OTA. I/O signals are routed to the rows and columns of the switch matrix [13].
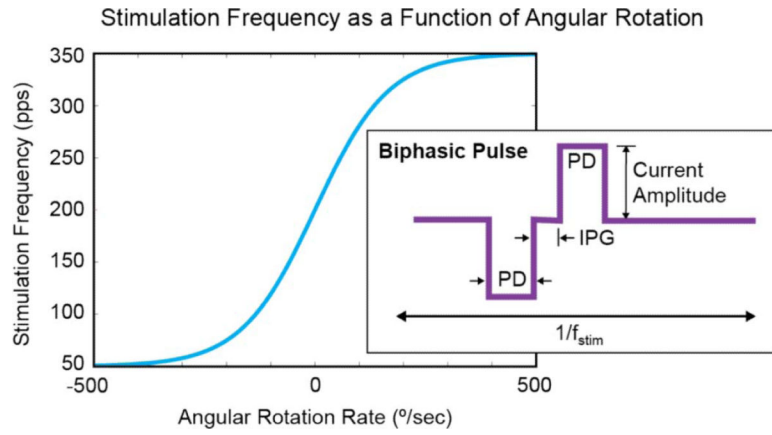
Fig. 3.
Stimulation frequency, f_{stim}, as a function of measured angular velocity [4]. The tanh function varies between 50–350 Hz with a baseline frequency of 200 Hz (zero angular head motion). A representative biphasic pulse is shown inside the graph. The amplitude and pulse duration (PD) of the cathodic pulse determine the charge delivered to the stimulation site. The PD and amplitude of the anodic pulse determine the charge returned from the tissue (balanced with input charge). The interphase gap (IPG) separates the two pulse periods and may be adjusted to optimize the neural response.
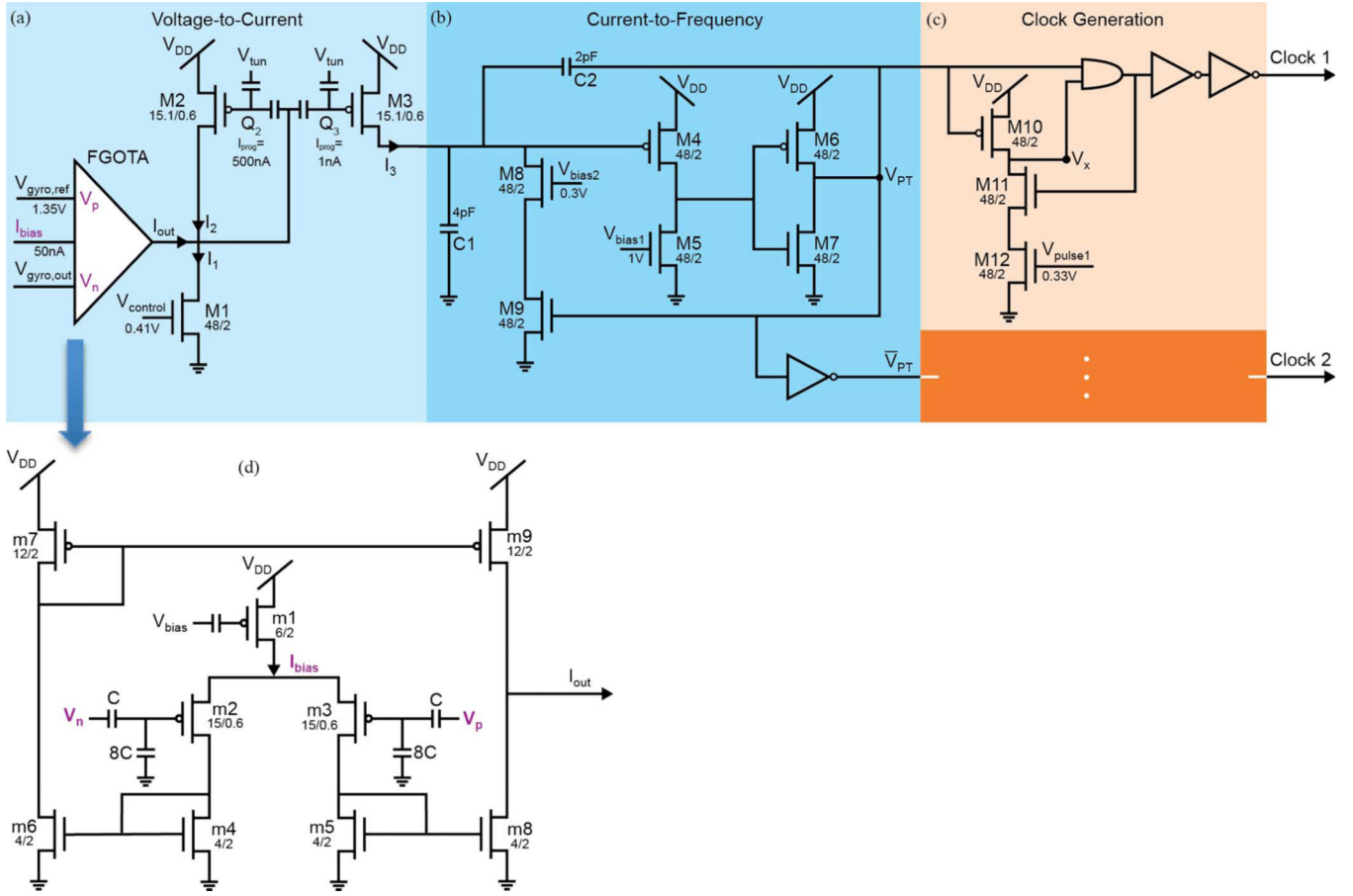
Fig. 4.

Circuit schematic of the signal processor. The bias voltages $V_{gyro,ref}$, $V_{control}$, V_{bias1}, V_{bias2}, V_{pulse1} and V_{pulse2} are generated using an off-chip DAC housed on a development board. (a) The voltage-to-current converter block transfers the voltage signal from the gyroscope, $V_{gyro,out}$, into a current signal, I_3. The current I_3 is related to angular velocity through a tanh function. The minimum level of I_3 is controlled by $V_{control}$. By adjusting $V_{gyro,ref}$ an offset can be added to $V_{gyro,out}$. This serves to translate the I_3 along the x-axis of the I_3 versus $V_{gyro,out}$ curve. (b) The current-to-frequency converter block converts the current signal, I_3, into the pulse train output V_{PT}. Linearly related to I_3, the frequency of V_{PT} determines f_{stim}. (c) Two similar fully digital Clock Generation stages create Clock 1 and Clock 2. The pulse width of Clock 1 is controlled by V_{pulse1} and a similar relationship exists for Clock 2. (d) The FGOTA is the core of the voltage-to-current converter block. In the sub-threshold region, the output current, I_{out}, of the FGOTA is related to its differential input voltage, V_p-V_n, through a tanh function I_{bias}. is the bias current which determines the region of operation and is set up during the programming stage by V_{bias}.
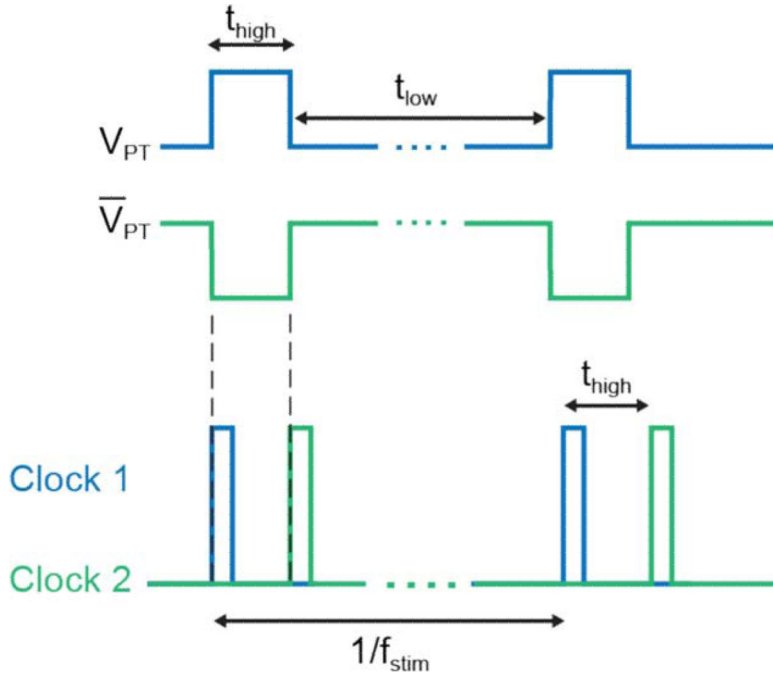
Fig. 5.
Pulse timing control. The signal V_{PT} is output from the current-to-frequency converter block with a pulse rate of f_{stim}. The rising edge of V_{PT} triggers Clock 1 in the clock generation block. The clock generation block also controls the PD, the duration of each clock. The delay between the clocks, t_{high}, less the PD is the IPG.
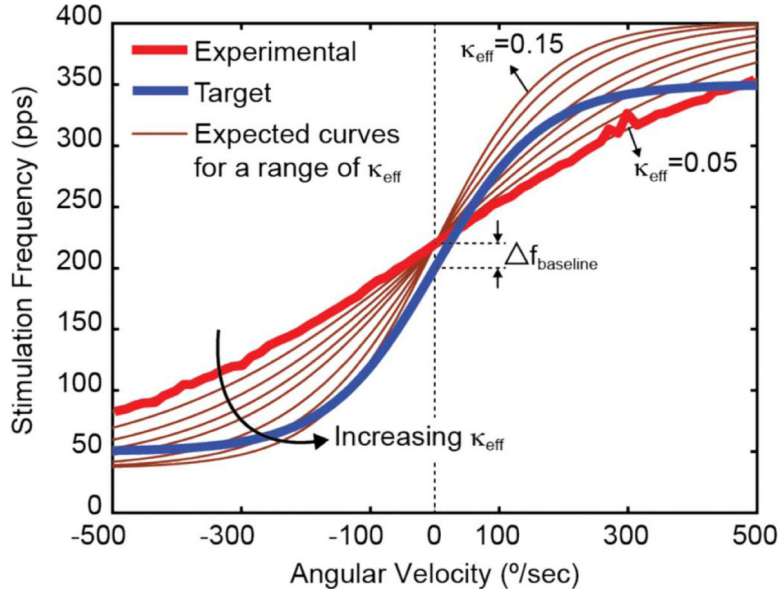
Fig. 6.
Stimulation frequency versus angular velocity. The experimental stimulation frequency (pulse rate) as a function of angular velocity is shown. Superimposed on the plot is a a series of curves illustrating f_{stim} versus angular velocity for κ_{eff} (0.05–0.15). The steepness of the curve is controlled by the κ_{eff} of the FGOTA. The baseline frequency difference between the experimental and the target curves, $f_{baseline}$, can be adjusted by decreasing (controlled by $V_{control}$). To control the stimulation frequency range, the following values can be adjusted: the bias current of the FGOTA, I_{bias}, and the current ratio of the mismatched current mirror, I_3 / I_2(2), and the capacitance C2 (3).
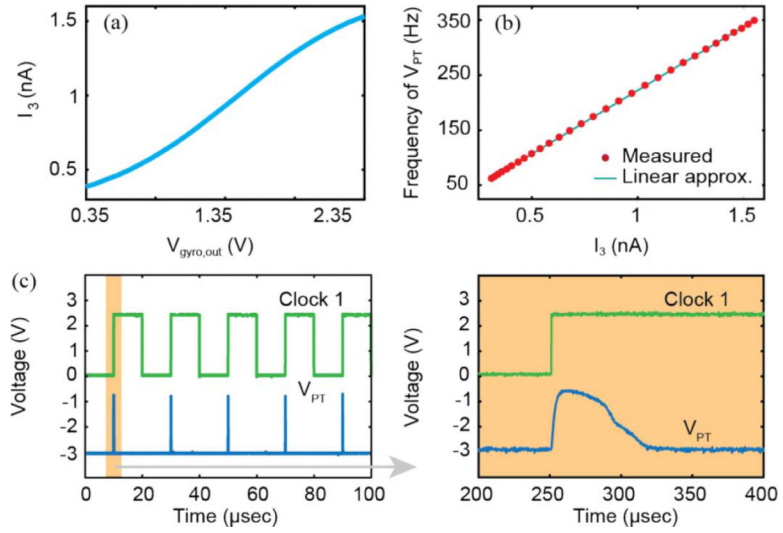
Fig. 7.
Summary of signal processor block level outputs. (a) Non-linear response to $V_{\text{gyro,out}}$ generated by the voltage-to-current conversion block. (b) Linear f_{stim} versus I_3 response is exhibited by the current-to-frequency conversion block with $t_{\text{high}} = 200$ μs. (c) Triggering of Clock 1 by the rising edge of V_{PT}. Note that a long (10 ms) clock pulse was created in the clock generation block to illustrate the relationship between the rising edge V_{PT} of and Clock 1. In practice the pulse duration of Clock 1 would be less than the duration of V_{PT}.
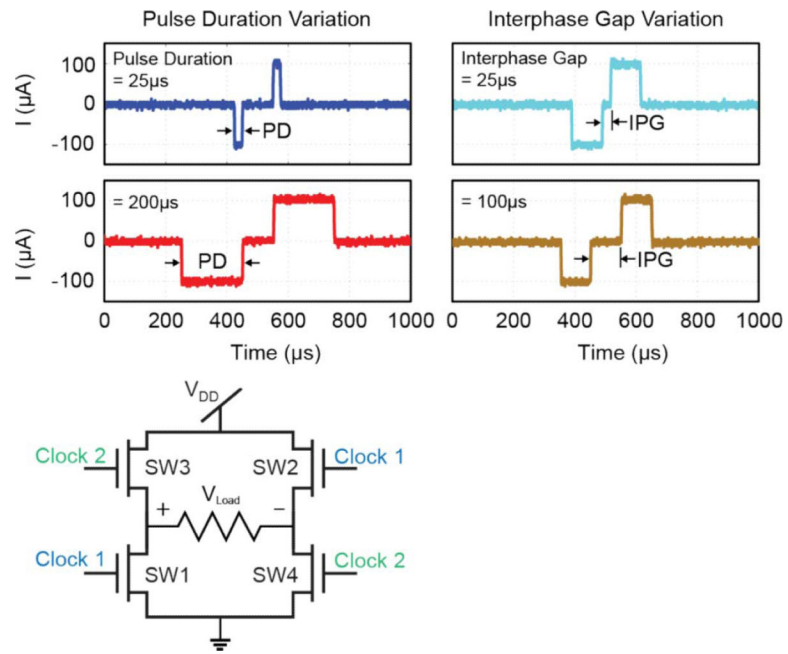
Fig. 8.
Biphasic pulse control. Using a 1 kΩ resistive load placed across an H-bridge circuit, Clock 1 and Clock 2 serve to control a cathodic-first, symmetric, biphasic pulse. Representative values of the PD and IPG are demonstrated.