NANO LETTERS

Letter

pubs.acs.org/NanoLett

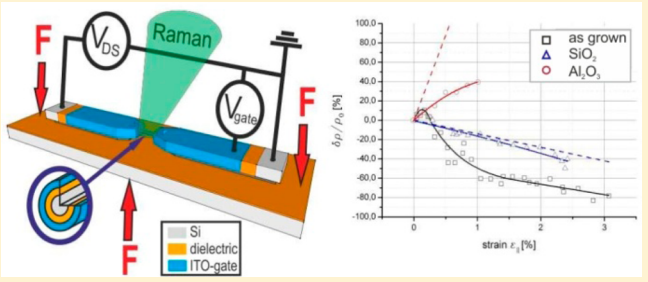
Origin of Anomalous Piezoresistive Effects in VLS Grown Si Nanowires

Karl Winkler, Emmerich Bertagnolli, and Alois Lugstein*

Institute for Solid State Electronics, TU-Wien, Floragasse 7, A-1040 Vienna, Austria

Supporting Information

ABSTRACT: Although the various effects of strain on silicon are subject of intensive research since the 1950s the physical background of anomalous piezoresistive effects in Si nanowires (NWs) is still under debate. Recent investigations concur in that due to the high surface-to-volume ratio extrinsic surface related effects superimpose the intrinsic piezoresistive properties of nanostructures. To clarify this interplay of piezoresistive effects and stress related surface potential modifications, we explored a particular tensile straining device (TSD) with a monolithic embedded vapor−liquid−solid (VLS) grown Si NW. Integrating the suspended NW in a gate all around (GAA) field effect transistor (FET) configuration with a transparent gate stack enables optical and field modulated electrical characterization under high uniaxial tensile strain applied along the ⟨111⟩ Si NW growth direction. A model based on stress-induced carrier mobility change and surface charge modulation is proposed to interpret the actual piezoresistive behavior of Si NWs. By controlling the nature and density of surface states via passivation the "true" piezoresistance of the NWs is found to be comparable with that of bulk Si. This demonstrates the indispensability of application-specific NW surface conditioning and the modulation capability of Si NWs properties for sensor applications.



KEYWORDS: *Silicon, nanowire, VLS growth, piezoresistance, surface doping*

Strain engineering has been widely explored to alter the band structure[1−5] in semiconductors and thereby elementary physical properties like the effective mass,[3,4] carrier mobility,[2] band alignment,[6,7] or electrical conductivity.[5] The benefit of mobility improvement has accomplished the step from basic research to industrial production of strained Si to enhance performance of CMOS devices.[8] The main limitation of strain engineering is founded in the maximum fraction strength of the respective material. For bulk Si the maximum yield stress that can be applied without causing damage to the crystal lattice is 3 GPa.[9] An increase of fracture strength for nanostructures has been proven for VLS grown single crystalline silicon NWs. The reason therefore is 2-fold, namely, a decrease of defect concentration as well as modifications of the fracture initiation mechanism.[10] By using a VLS growth process, such quasi-one-dimensional rods with a nearly defect free lattice structure can be synthesized with excellent control of chemical composition, geometry, and growth orientation. Such grown Si NWs with diameters below 200 nm have shown an increase of the fracture strain limit up to 12 ± 3 GPa[10] at near the same Young's module.[11]

Anomalous piezoresistance observed in such Si NWs represents a further remarkable example of the effect of size on the physical properties of one of the most well studied semiconductors. The change in resistance due to an applied mechanical stress, being orders of magnitude larger than that of bulk Si is seen as a potential breakthrough of detecting motion in nanoelectromechanical systems.[12] However, because of the large surface-to-volume ratio of nanostructures, the electrical and optical properties of NWs are affected or even determined by dangling bonds, defects, or adsorbates.[13−17] As a result, the performance of nanodevices are expected to be strongly determined by surface states, ruling mainly the functionality of, e.g., highly sensitive sensors.[18−22] Thus, with respect to strain related investigations this requires an impeccable design of experiment, to distinguish whether an effect is mainly attributed to the intrinsic strain related effects or to surface state alterations.[14,23,24]

To clarify this interplay of surface related effects and strain engineering in nanostructures, we explored a particular TSD with a suspended VLS grown Si NW integrated in a FET configuration, enabling combined electric field and strain modulation in individual NWs. Figure 1a shows the schematic of the 3-point straining module and Figure 1b the respective SEM image of an individual Si NW bridging the Si pads of a silicon-on-insulator device structure.

By combining well-known top down semiconductor processing techniques and epitaxial Si NW growth with control of the NW location and orientation we circumvent the problem of handling and positioning nanometer-sized objects that arise

Received: November 21, 2014
Revised: January 19, 2015
Published: February 4, 2015

DOI: 10.1021/nl5044743
Nano Lett. 2015, 15, 1780−1785

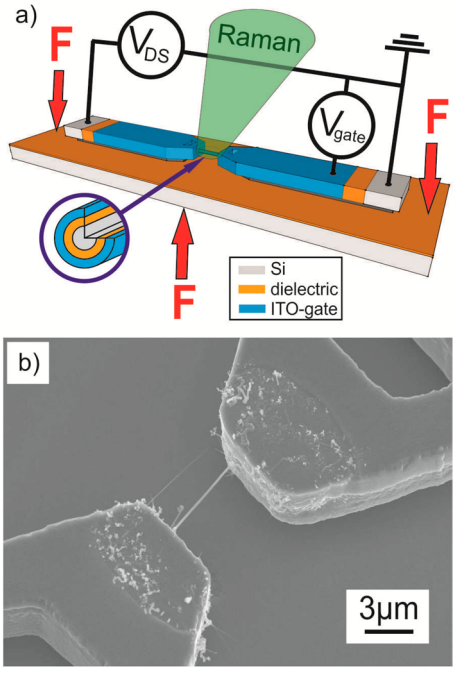


Figure 1. (a) Schematic of the 3-point bending TSD with a monolithically integrated VLS grown Si NW suspended between insulated Si pads. Combined with a dielectric coating and a wrapped around gate, this resembles a gate all around FET. The transparent gate stack enables electrical and optical characterization of the electric field modulated NW under high uniaxial strain. Because of the optically transparent gate stack, μ-Raman spectroscopy can be used for in situ strain measurement. (b) SEM image of the suspended Si NW aligned along the ⟨111⟩ direction, within a trench with vertical {111} facets on a ⟨110⟩-oriented SOI substrate.

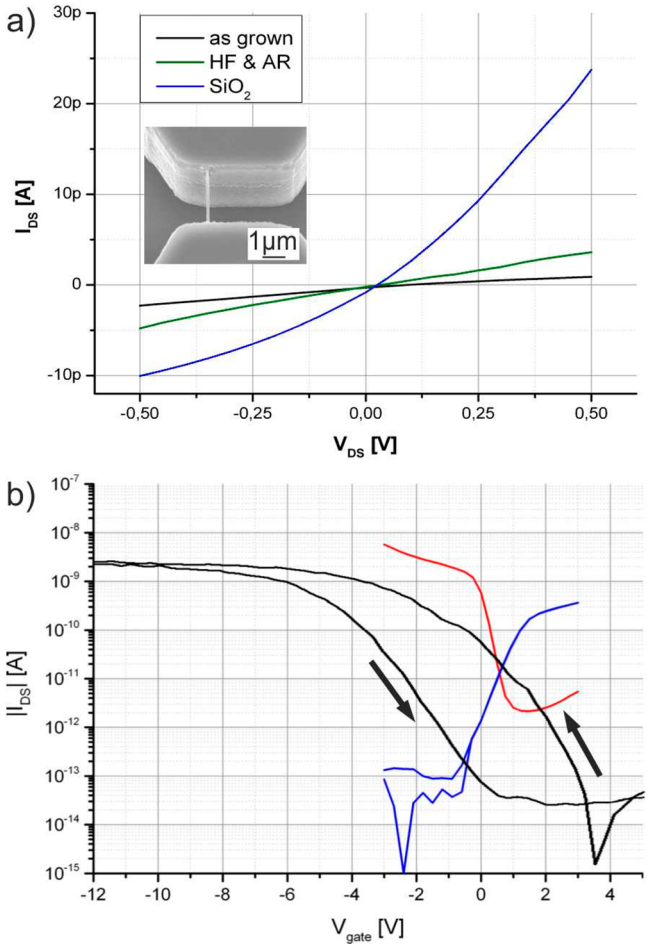


Figure 2. (a) Electrical characterization of a suspended Si NW in the TSD. The I/V curves were measured for the as-grown Si NW as well as after removal of residual gold particles from the NW surface and successive thermal oxidation. (b) Transfer characteristics of NW FET. The black line shows the transfer characteristic of an as-grown Si NW in back gate geometry (see Supporting Information), while the blue and red line represent the transfer characteristics of the Si NW in the TSD with thermal SiO_2 and Al_2O_3 layers as gate dielectrics. The transfer characteristics were measured for unstrained NWs at V_{DS} = 0.5 V.

in the conventional pick-and-place approach.[25] The NW is monolithically integrated into the TSD through a self-aligned VLS growth process, which guarantees electrically reliable and mechanical robust contacts.[26,27] The SEM image in Figure 1b shows a detailed view of the ⟨111⟩-oriented Si NW bridging two insulated Si pads. To accomplish the GAA FET and further enable optical measurements in situ, a transparent gate stack was assembled with SiO_2 or Al_2O_3 as dielectric and indium−tin−oxide (ITO) as the NW wrapped around gate. The TSD chip is aligned and glued firmly onto a steel plate, and electrical contacts are formed by aluminum wire bonding according to the schematic in Figure 1a. Thus, when the steel plate is subjected to 3-point bending, mainly uniaxial tensile stress is created along the suspended NW. Details of TSD design and processing, NW integration, and GAA formation are given in the Supporting Information.

As a feedback for process optimization, I/V characteristics were measured (i) for the as-grown NW, (ii) after removal of Au residuals from the NW surface with aqua regia and buffered hydrofluoric acid (BHF), and finally, (iii) after the deposition of the dielectrics. The I/V curves in Figure 2a show the effect of the chemical treatment as well as subsequent thermal oxidation on the electrical transport properties of the VLS grown Si NW in the TSD.

A characteristic I/V curve for an as-grown Si NW is shown in Figure 2a (black curve). By fitting the linear part near zero bias of nine NWs, a resistivity of 67 ± 8 kΩ cm is determined. Through linearization of the measured I/V curve this value represents an average of the resistivity over the bulk region and the space-charge region at the surface of the NW. For the TSD, electrical measurements are confined to 2-terminal measurements suffering from parasitic effects of the contact resistance. However, because of the low resistivity of the heavily p-doped contact regions the contact resistance was found to be negligible. Several NWs were measured in parallel to the processing steps to characterize the influence of each individual step. The measurement of the as-grown NWs was performed several days after NW synthesis and storage in ambient air; thus, we can expect that each NW is covered with a saturated native oxide of a thickness of about 2 nm.[14] After etching gold particles, decorating a Si NW after VLS growth,[28] with aqua regia and BHF, the TSD was immediately transferred to the electrical probe station. Because of BHF treatment, the native oxide is removed and the NW exhibits an H-terminated surface.[29,30] Compared to the as-grown Si NWs after the chemical treatment the NWs showed an improved conductivity. Finally the formation of the SiO_2 dielectrics via thermal oxidation leads to a further pronounced increase of the current by more than an order of magnitude. Covering a NW with

DOI: 10.1021/nl5044743
Nano Lett. 2015, 15, 1780−1785

Al_2O_3 immediately after the gold removal leads in contrary to a slight decrease of the current. Thus, the I/V characteristic of the Al_2O_3 coated NWs and the as-grown NWs appeared to be very similar.

According to the large surface-to-volume ratio, dangling bonds, surface defects, and adsorbates play a dominant role in the electrical characteristics of NWs. Previous reports suggested that adsorbates (mainly water and oxygen) can seriously influence the electrical properties of nanostructures by trapping carriers.[31−33] However, transferring our device into vacuum does not change the electrical characterization distinctly. According to our experimental results we thus propose that conductivity of VLS grown Si NWs is dominated by surface defects and dangling bonds. After the BHF dip the native oxide is removed and the NW has an H-terminated surface. The increase in conductance by more than an order of magnitude after thermal oxidation can thus be explained through the replacement of the native oxide with quite poor interface properties by a high quality thermal oxide. The SiO_2 layer formation by thermal oxidation isolates the device from the ambient and has been proven to be effective in passivating nanostructure surface defects.[34]

As stated above the suspended NWs with the dielectric (SiO_2 or Al_2O_3) and terminal ITO coating resembles a FET with a transparent wrapped around gate. This setup enables to measure the transfer characteristics of the field-modulated NW at various strain levels. Figure 2b shows the comparison of thus measured transfer characteristics for an unstrained NW with SiO_2 and Al_2O_3 dielectrics as well as for an as-grown NW in four-probe backgate configuration (see Supporting Information). For the as-grown Si NW (black line) the current through the NW increases appreciably with increasing negative gate voltage, characteristic for a p-channel enhancement mode transistor. Even though the VLS synthesized Si NWs are not doped on purpose during growth, unintentional p-type doping usually occurs due to surface states and bulk impurities.[18,35] Surprisingly the Si NWs in the TSD with SiO_2 as dielectric exhibit the typical characteristics of an n-channel FET, i.e., the device is OFF for negative gate voltage. This inversion of the conduction type demonstrates that controlling surface charges can similarly achieve doping effects in NWs. Becuase of Schmidt et al.,[14] the effective carrier concentration in NWs is strongly linked to the density of interface traps as well as to the fixed oxide charges (Q_F). For NWs with low doping concentration the polarity of fixed oxide charge of the surrounding dielectric material in combination with modification of surface states can even cause an inversion of the major carrier type in the NW.[15,24] Thus, using SiO_2 as dielectric, positive fixed oxide charges[36] in the range of $Q_F = +10^{10}$ cm^{-2} changes the transfer characteristic into an n-type. Consequently for Al_2O_3 as dielectric, which exhibits negative fixed oxide charges[36] in the range of $Q_F = -10^{11}$ cm^{-2}, the Si NWs in the TSD device show p-type behavior (Figure 2b). Further for the as-grown NW in back gated configuration sweeping the gate voltage from negative to positive values and vice versa, we observe a pronounced hysteresis (see Figure 2b). This behavior is indicative of charge-trapping states originating from the large number of surface defects and dangling bonds.[37,38] Again, when the native oxide is replaced by the high quality thermal oxide, the transfer characteristic of the suspended NW shows much less hysteresis (see Figure 2b) indicating reduction of charge traps.[18,39]

A prerequisite to investigate the interplay of such surface related effects and mechanical stress on the electronic properties of NWs requires the opportunity to modulate the transverse electric field and an accurate strain measurement. The particular TSD module with the transparent gate stack enables such electrical characterization of the wrapped around gate FET and to determine the actual strain of the Si NW using confocal μ-Raman spectroscopy (see Figure 1a). Application of stress to the NW causes a shift of the first order optical phonon peak of Si at 520.2 cm^{-1} linearly dependent on the strain.[40] These typical shifts to lower wave numbers of a strained NW integrated in the TSD and, for comparison, bulk Si are shown in Figure 3a. The inset shows the relationship between the Raman signal peak shift and thereof calculated strain values of the NW. The maximum peak shift of about 8 cm^{-1} shown for the highest strain level in the main plot of Figure 3a corresponds to a tensile strain of 2.4%. Details of strain

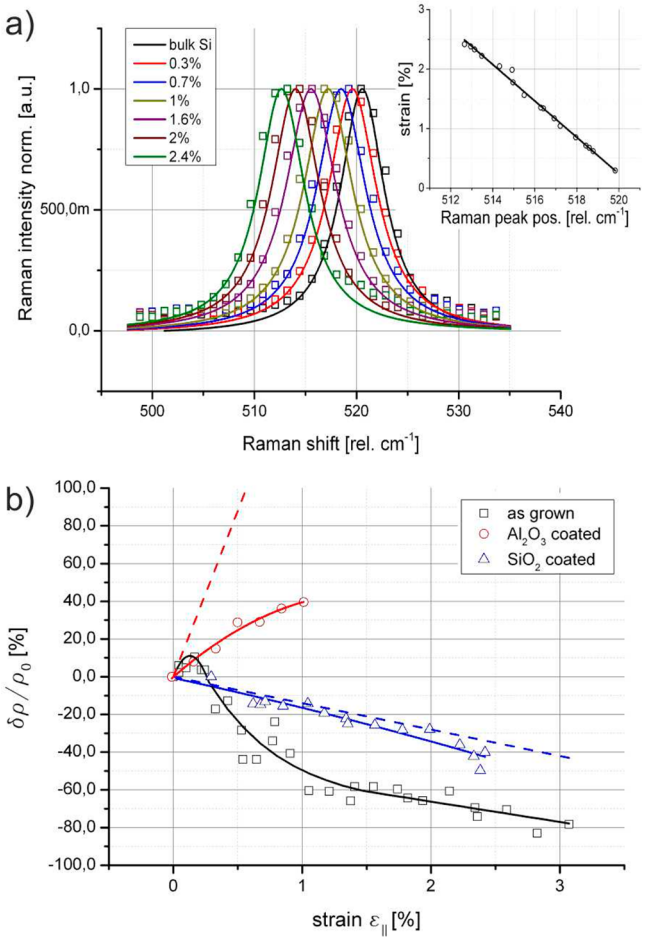


Figure 3. (a) Normalized Raman signal peak position shift corresponding to the strain level of an individual Si NW in the TSD. The Raman signal is shifted to lower wave numbers at increasing tensile strain with respect to the signal of an unstrained Si wafer. The inset shows the correlation between Raman peak position and tensile strain applied to the NW. (b) Relative change in resistivity as a function of applied strain of an as-grown Si NW as well as after passivation with SiO_2 and Al_2O_3. The values are calculated at a bias voltage of $V_{DS} = 0.5$ V and gate voltage $V_G = 0$ V. The data of the as-grown NW are integrated from previous work.[41] The dashed lines show the calculated curves for lightly p- and n-doped silicon.[42]

DOI: 10.1021/nl5044743
Nano Lett. 2015, 15, 1780−1785

determination and the calibration routine are given in the Supporting Information.

The accurate strain measurement and subsequent I/V characterization enable us to measure changes in the resistivity due to strain and thus to determine the piezoresistive coefficients. The equation for the relative change of resistivity $\Delta\rho/\rho$ for a cylindrical piezoresistive NW is given by

$$\frac{\Delta\rho}{\rho} = \frac{\Delta R}{R} - (1 + 2\upsilon)\varepsilon_{\parallel} \cong \frac{\Delta R}{R}$$

with υ the Poisson's ratio and $\varepsilon_{\parallel}$ the strain along the ⟨111⟩ growth direction of the Si NW. Dimensional changes of the NW caused by strain were neglected due to their small contribution. Figure 3b shows the strain induced relative change in resistivity for an as-grown Si NW as well as the Si NW in GAA FET configuration with Al_2O_3 or SiO_2 as dielectric layer. For the as-grown NW covered with native oxide, we determined an anomalous behavior with an increase of the resistivity up to strain levels of about 0.3% followed by a strong decrease down to $\Delta\rho/\rho \approx -80\%$ for about 3% strain.[41] For the Al_2O_3 coated Si NW the resistivity increases monotonically up to a maximum of $\Delta\rho/\rho \approx +30\%$ at a strain level of $\varepsilon_{\parallel} = 1\%$. Although Al_2O_3 coated Si NW withstands higher loads before a sudden failure occurs, electrical characterization was limited due to the appearance of leakage currents in the gate dielectric for strain values >1%. With SiO_2 as dielectric the device appeared to be less prone to strain induced leakage. Contrary to the Al_2O_3 for the SiO_2 coated NW we determined a decrease of the resistivity to $\Delta\rho/\rho \approx -30\%$ at a strain of $\varepsilon_{\parallel} = 2.4\%$ limited by the mechanical robustness of the NWs. Assuming uniaxial strain the piezoresistive coefficients can be calculated according to

$$\frac{\Delta\rho}{\rho} = \pi_l\sigma$$

with $\Delta\rho/\rho$ the relative change of resistivity, π_l the longitudinal piezoresistive coefficient and σ the applied stress. This coefficient is dependent on crystal orientation as well as on doping concentration of the semiconductor.[42]

Simulation results of ⟨111⟩ oriented Si show a piezoresistive coefficient for p-doped bulk Si in the range of $\pi_l = +94 \times 10^{-11}$ Pa^{-1}, while for n-type Si the piezoresistive coefficient has negative sign and is in the range of $\pi_l = -7.5 \times 10^{-11}$ Pa^{-1}.[42] Fitting the measurement data in the linear regime in Figure 3b leads to a longitudinal piezoresistive coefficient of $\pi_l = +26.7 \times 10^{-11}$ Pa^{-1} and $\pi_l = -8.8 \times 10^{-11}$ Pa^{-1} for a Si NW coated with Al_2O_3 and SiO_2, respectively. The dashed lines in Figure 3b show the calculated trend of p-doped (red dashed line) and n-doped (blue dashed line) bulk silicon. While the piezoresistive coefficient of the SiO_2 covered NW shows good agreement with the n-doped bulk value, for the Al_2O_3 passivated Si NW the stress induced increase of the resistivity is less pronounced and tends to saturate at higher strain values. Nonetheless, qualitatively and in accordance with the transfer characteristic measurements the piezoresistive behavior of the Al_2O_3 and SiO_2 covered Si NWs behave like n-type and p-type doped Si, respectively. Thus, for the passivated Si NWs no anomalous piezoresistance was observed, but taking into account surface related doping effects in nanostructures,[15] the true stress-dependent conductance change is consistent with bulk Si piezoresistance.

Measuring the transconductance g_m characteristics for the same NWs one can estimate the field mobility μ of the carriers as a function of strain according to $g_m = dI_D/dV_G = \mu CV_D/L^2$, with L representing the active channel length and C the capacitance between the cylindrical NW and the gate contact.[43] Figure 4a shows the comparison of the change in relative

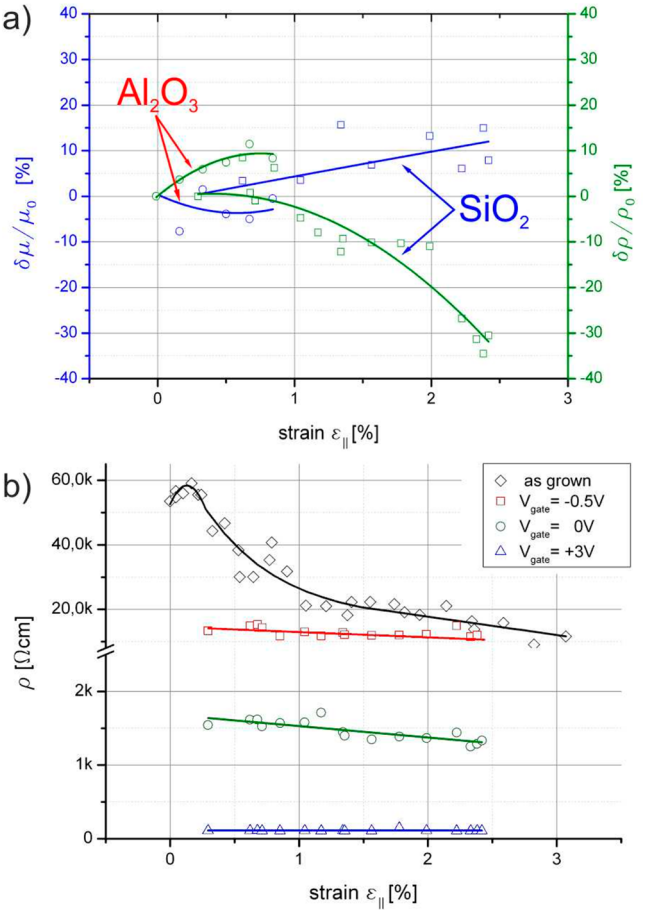


Figure 4. (a) Comparison of the relative change of resistivity and mobility of SiO_2 or Al_2O_3 passivated suspended NWs under tensile strain. The values are extracted at a bias voltage of $V_{DS} = 0.5$ V and a gate voltage of $V_{gate} = 1.5$ V. (b) Absolute value of the resistivity of an as-grown Si NW and a SiO_2 coated NW in the TSD.

resistivity and the corresponding relative change in field-effect mobility as a function of applied strain. For both, the SiO_2 as well as the Al_2O_3 covered NW, the resistivity changes appear to be directly proportional to mobility modifications due to strain. Figure 4b shows the strain related change of the NW resistivity in absolute values for the as-grown and the Si NW FET with SiO_2 as dielectric for different gate voltages. The resistivity of the as-grown NW appears to be more than 35 times larger compared to the SiO_2 coated NW at gate bias of $V_{gate} = 0$ V. The lower resistivity proves again the effectiveness of SiO_2 in surface state passivation. In accordance with Schmidt et al., we observed an increase of mobility as well as the effective carrier concentration of the wire and therefore a significant decrease of resistance.[24] However, more remarkably for the SiO_2 coated NW, even when the gate field modulates the density of charge carriers and thus the conductance in the channel over several decades, the influence of strain appears to be widely unaffected by the gate bias. Thus, again, the piezoresistivity of SiO_2 coated Si NWs, i.e., the increase in conductivity is mainly attributed to

DOI: 10.1021/nl5044743
Nano Lett. 2015, 15, 1780−1785

the strain induced mobility increase independent of the gate modulated charge carrier density.

The issue still to be resolved concerns the origin of the anomalous piezoresistance of the VLS grown Si NWs. For the bare NW integrated in the TSD a positive piezoresistive coefficient of $+36.3 \times 10^{-11}$ Pa^{-1} was calculated for strain values up to 0.3%, whereas for strain values up to 1% negative piezoresistivity was observed with $\pi_l = -50.3 \times 10^{-11}$ Pa^{-1} (Figure 3), more than 6 times higher than for n-doped bulk Si. For even higher strain up to 3% the piezoresistivity converges to values of bulk n-type doped Si. The quite low alteration of the piezoresistance of the passivated NWs indicates the origin of the anomalous piezoresistive effect of as-grown Si NWs to changes in surface charges during strain modulation. In accordance with Rowe, we thus determined stress induced modulation of the surface potential of the semiconductor as the origin of the anomalous piezoresistive behavior, which critically depend on the density and nature of the surface states.[44] Negative charges on the surface would cause surface band bending resulting in hole accumulation and thus induce the observed p-type behavior in as-grown Si NWs. The thus induced depletion region near the surface of the NW reduces also the conduction cross-sectional area.[15,16,45] As the Si NWs are thin, the depletion region occupies a great fraction of the cross-sectional area. Variations in the thickness of the depleted region occur via a stress-induced modulation of the surface potential barrier,[44] which leads to filling or depopulation of the trap states. Different surface states with their particular energy levels and density of states would result in different surface potentials due to Fermi level pinning at the surface states and thus modulate the depletion width.[46,47] Such variation of the depletion zone width would be most pronounced for intrinsic NWs. He and Yang observed large stress effects in NWs with high resistivity and small diameters, where the depletion width is approaching the NW diameter.[48]

For the as-grown nominally intrinsic NWs at low strain levels this depleting effect is more pronounced due to the higher concentration of defect states compared to the passivated NWs overcompensating a possible mobility improvement due to strain. For highly stressed NWs one also has to take into account strain induced bandgap narrowing resulting in an increase of the charge carrier density. In good agreement, several groups reported on experimental and theoretical works that bandgap changes for Si NWs under uniaxial tensile strain can be as large as 60 and 100 meV per 1% axial strain.[4,7,49,50]

Concluding, we have demonstrated that anomalous piezoresistance effects in VLS grown Si NWs are mainly determined by the filling or depopulation of surface states due to the stress induced modulation of the surface potential. By controlling the nature and density of these surface states via passivation, the intrinsic piezoresistance of the NWs is found to be a result of stress-induced carrier mobility change and comparable with that of bulk Si. This demonstrates the indispensability of application orientated surface conditioning to make use of nanostructure related strain effects and highlights the modulation capability of Si NWs for sensor applications, e.g., strain gauges.

■ ASSOCIATED CONTENT

Supporting Information

Device fabrication and NW synthesis, gate stack formation, strain determination, and calibration. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: alois.lugstein@tuwien.ac.at.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

The authors acknowledge financial support from the Austrian Science Fond (FWF) project I 708 N16 and would like to thank Center for Micro- and Nanostructures (ZMNS) for providing the cleanroom facilities.

■ REFERENCES

(1) Greil, J.; Lugstein, A.; Zeiner, C.; Strasser, G.; Bertagnolli, E. *Nano Lett.* **2012**, *12*, 6230−6234.
(2) Niquet, Y.-M.; Delerue, C.; Krzeminski, C. *Nano Lett.* **2012**, *12*, 3545−3550.
(3) Kleimann, P.; Semmache, B.; Le Berre, M.; Barbier, D. *Phys. Rev. B* **1998**, *57*, 8966 .
(4) Shiri, D.; Kong, Y.; Buin, A.; Anantram, M. P. *Appl. Phys. Lett.* **2008**, *93*, 073114.
(5) Cao, J. X.; Gong, X. G.; Wu, R. Q. *Phys. Rev. B* **2007**, *75*, 233302.
(6) Wei, J.-Y.; Maikap, S.; Lee, M. H.; Lee, C. C.; Liu, C. W. *Solid-State Electron.* **2006**, *50*, 109−113.
(7) Hong, K.-H.; Kim, J.; Lee, S.-H.; Shin, J. K. *Nano Lett.* **2008**, *8*, 1335−1340.
(8) Flachowsky, S.; Wei, A.; Illgen, R.; Herrmann, T.; Höntschel, J.; Horstmann, M.; Klix, W.; Stenzel, R. *IEEE Trans. Electron Devices* **2010**, *57*, 1343−1354.
(9) Hu, S. M. *J. Appl. Phys.* **1982**, *53*, 3576.
(10) Hoffmann, S.; Utke, I.; Moser, B.; Michler, J.; Christiansen, S. H.; Schmidt, V.; Senz, S.; Werner, P.; Gösele, U.; Ballif, C. *Nano Lett.* **2006**, *6*, 622−625.
(11) Zhu, Y.; Xu, F.; Qin, Q.; Fung, W. Y.; Lu, W. *Nano Lett.* **2009**, *9*, 3934−3939.
(12) He, R.; Feng, X. L.; Roukes, M. L.; Yang, P. *Nano Lett.* **2008**, *8*, 1756−1761.
(13) Dayeh, S. A. *Semicond. Sci. Technol.* **2010**, *25*, 024004.
(14) Seo, K.; Sharma, S.; Yasseri, A. A.; Stewart, D. R.; Kamins, T. I. *Electrochem. Solid-State Lett.* **2006**, *9*, G69.
(15) Jie, J.; Zhang, W.; Peng, K.; Yuan, G.; Lee, C. S.; Lee, S.-T. *Adv. Funct. Mater.* **2008**, *18*, 3251−3257.
(16) Björk, M. T.; Schmid, H.; Knoch, J.; Riel, H.; Riess, W. *Nat. Nanotechnol.* **2009**, *4*, 103−107.
(17) Jang, H.; Kim, J.; Kim, M.-S.; Cho, J. H.; Choi, H.; Ahn, J.-H. *Nano Lett.* **2014**, 141111093449001.
(18) Fahem, Z.; Csaba, G.; Erlen, C. M.; Lugli, P.; Weber, W. M.; Geelhaar, L.; Riechert, H. *Phys. Status Solidi C* **2008**, *5*, 27−30.
(19) Cao, A.; Sudhölter, E.; de Smet, L. *Sensors* **2013**, *14*, 245−271.
(20) Chen, X.; Wong, C. K. Y.; Yuan, C. A.; Zhang, G. *Sens. Actuators, B* **2013**, *177*, 178−195.
(21) Cvelbar, U.; Ostrikov, K. (Ken); Drenik, A.; Mozetic, M. *Appl. Phys. Lett.* **2008**, *92*, 133505.
(22) Mohseni Kiasari, N.; Soltanian, S.; Gholamkhass, B.; Servati, P. *Sens. Actuators Phys.* **2012**, *182*, 101−105.
(23) Milne, J.; Rowe, A.; Arscott, S.; Renner, C. *Phys. Rev. Lett.* **2010**, 105.
(24) Schmidt, V.; Senz, S.; Gösele, U. *Appl. Phys. A: Mater. Sci. Process.* **2006**, *86*, 187−191.
(25) Whang, D.; Jin, S.; Wu, Y.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 1255−1259.
(26) Saif Islam, M.; Sharma, S.; Kamins, T. I.; Stanley Williams, R. *Appl. Phys. A: Mater. Sci. Process.* **2005**, *80*, 1133−1140.
(27) He, R.; Gao, D.; Fan, R.; Hochbaum, A. I.; Carraro, C.; Maboudian, R.; Yang, P. *Adv. Mater.* **2005**, *17*, 2098−2102.
(28) Dupré, L.; Buttard, D.; Leclere, C.; Renevier, H.; Gentile, P. *Chem. Mater.* **2012**, *24*, 4511−4516.

DOI: 10.1021/nl5044743
Nano Lett. 2015, 15, 1780−1785

(29) Chazalviel, J.-N.; Ozanam, F. *J. Appl. Phys.* **1997**, *81*, 7684.
(30) Ma, D. D. D. *Science* **2003**, *299*, 1874−1877.
(31) Jie, J. S.; Zhang, W. J.; Jiang, Y.; Meng, X. M.; Li, Y. Q.; Lee, S. T. *Nano Lett.* **2006**, *6*, 1887−1892.
(32) Jie, J. S.; Zhang, W. J.; Jiang, Y.; Lee, S. T. *Appl. Phys. Lett.* **2006**, *89*, 223117.
(33) Wang, D.; Chang, Y.-L.; Wang, Q.; Cao, J.; Farmer, D. B.; Gordon, R. G.; Dai, H. *J. Am. Chem. Soc.* **2004**, *126*, 11602−11611.
(34) Kim, H.-J.; Lee, C.-H.; Kim, D.-W.; Yi, G.-C. *Nanotechnology* **2006**, *17*, S327−S331.
(35) Lin, Y.-C.; Lu, K.-C.; Wu, W.-W.; Bai, J.; Chen, L. J.; Tu, K. N.; Huang, Y. *Nano Lett.* **2008**, *8*, 913−918.
(36) Kotipalli, R.; Delamare, R.; Poncelet, O.; Tang, X.; Francis, L. A.; Flandre, D. *EPJ Photovolt.* **2013**, *4*, 45107.
(37) Fujii, H.; Kanemaru, S.; Matsukawa, T.; Itoh, J. *Appl. Phys. Lett.* **1999**, *75*, 3986.
(38) Matsukawa, T.; Kanemaru, S.; Masahara, M.; Nagao, M.; Tanoue, H.; Itoh, J. *J. Vac. Sci. Technol., B* **2003**, *21*, 664.
(39) Goldberger, J.; Hochbaum, A. I.; Fan, R.; Yang, P. *Nano Lett.* **2006**, *6*, 973−977.
(40) Ureña, F.; Olsen, S. H.; Raskin, J.-P. *J. Appl. Phys.* **2013**, *114*, 144507.
(41) Wagesreither, S.; Bertagnolli, E.; Kawase, S.; Isono, Y.; Lugstein, A. *Nanotechnology* **2014**, *25*, 455705.
(42) Kanda, Y. *IEEE Trans. Electron Devices* **1982**, *29*, 64−70.
(43) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*; John Wiley & Sons: New York, 2006.
(44) Rowe, A. C. *Nat. Nanotechnol.* **2008**, *3*, 311−312.
(45) Kimukin, I.; Islam, M. S.; Williams, R. S. *Nanotechnology* **2006**, *17*, S240−S245.
(46) Derrien, J.; Ringeisen, F. *Solid State Commun.* **1984**, *50*, 627−628.
(47) Watanabe, D.; En, A.; Nakamura, S.; Suhara, M.; Okumura, T. *Appl. Surf. Sci.* **2003**, *216*, 24−29.
(48) He, R.; Yang, P. *Nat. Nanotechnol.* **2006**, *1*, 42−46.
(49) Nakamura, H. *IEEE-NANO 2009 9th IEEE Conf. Nanotechnol.* **2009**, 555−558.
(50) Munguía, J.; Bremond, G.; Bluet, J. M.; Hartmann, J. M.; Mermoux, M. *Appl. Phys. Lett.* **2008**, *93*, 102101.

DOI: 10.1021/nl5044743
Nano Lett. 2015, 15, 1780−1785