SCIENTIFIC REPORTS

OPEN

Received: 10 February 2016
Accepted: 22 June 2016
Published: 12 July 2016

Thickness Considerations of Two-Dimensional Layered Semiconductors for Transistor Applications

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Layered two-dimensional semiconductors have attracted tremendous attention owing to their demonstrated excellent transistor switching characteristics with a large ratio of on-state to off-state current, I_{on}/I_{off}. However, the depletion-mode nature of the transistors sets a limit on the thickness of the layered semiconductor films primarily determined by a given I_{on}/I_{off} as an acceptable specification. Identifying the optimum thickness range is of significance for material synthesis and device fabrication. Here, we systematically investigate the thickness-dependent switching behavior of transistors with a wide thickness range of multilayer-MoS_2 films. A difference in I_{on}/I_{off} by several orders of magnitude is observed when the film thickness, t, approaches a critical depletion width. The decrease in I_{on}/I_{off} is exponential for t between 20 nm and 100 nm, by a factor of 10 for each additional 10 nm. For t larger than 100 nm, I_{on}/I_{off} approaches unity. Simulation using technical computer-aided tools established for silicon technology faithfully reproduces the experimentally determined scaling behavior of I_{on}/I_{off} with t. This excellent agreement confirms that multilayer-MoS_2 films can be approximated as a homogeneous semiconductor with high surface conductivity that tends to deteriorate I_{on}/I_{off}. Our findings are helpful in guiding material synthesis and designing advanced field-effect transistors based on the layered semiconductors.

The first successful demonstration of field-effect transistors (FETs) based on monolayer molybdenum disulfide (MoS_2) with appealing performance[1,2] has stimulated intensive research on two-dimensional (2D) transition metal dichalcogenides (TMDs). The planar nature of these 2D semiconductor materials could potentially lead complementary metal-oxide-semiconductor (CMOS) technology to the ultimate size scaling envisioned by Moore's law and beyond[3–5]. MoS_2, a representative layered TMD, has a satisfactory bandgap in the range of 1.3 to 1.8 eV[6,7], which is advantageous over the well-studied gapless graphene with respect to the standby leakage current of its FETs[8]. The bandgap of MoS_2 is thickness-dependent and it is 1.8 eV for monolayers. As a result, transistors of both single- and multilayer-MoS_2 films have an exhibited high ratio of on-state to off-state current ($I_{on}/I_{off} > 10^6$) with reasonable electron mobility[1,9–11]. All this makes the layered TMDs promising in fields of low-power switches/circuits[11,12], nonvolatile memory devices[13,14], ultrasensitive photodetectors[15,16], *etc.*

In FET applications, multilayer MoS_2 with a smaller bandgap is of greater potential than the monolayer counterpart[17]. First, multilayer MoS_2 has a 3-fold higher density of states and conducts current along multiple channels, which can be translated to a considerably high drive current[11,18]. Second, the interlayer screening effect leads to a higher carrier mobility[19,20] and better noise immunity[21] in multilayer MoS_2. Compared to the direct-bandgap monolayer MoS_2 requiring a strict thickness control, the electronic properties of multilayer MoS_2 manifested by an indirect bandgap are relatively insensitive to layer thickness. Hence, multilayer MoS_2 is better suited for large-area and/or high-density electronics[22–24]. However, multilayer MoS_2 and other TMD semiconductors have so far gained limited attention for their use in electronics, compared to their monolayer counterparts.

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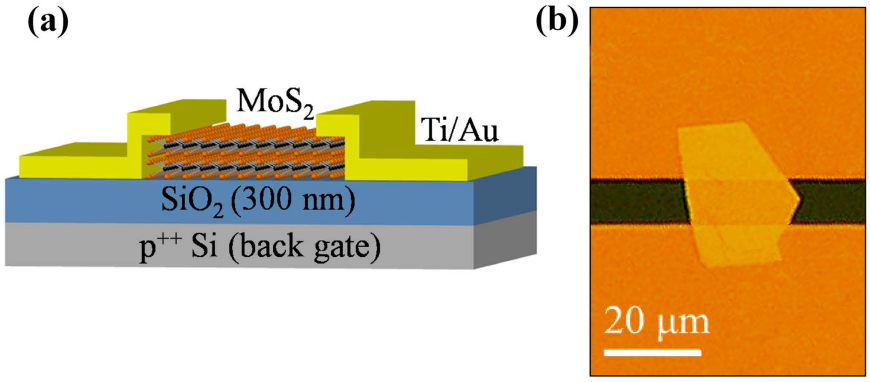

Figure 1. (**a**) Schematic representation and (**b**) Optical image of the field-effect transistor based on multilayer MoS_2.

Usually, MoS_2 is an *n*-type semiconductor that is determined by both intrinsic and extrinsic effects, such as sulfur vacancies, impurities or other structural defects[25–27]. Control of the electron mobility and carrier density in MoS_2 FETs can be achieved by engineering on the gate structure and dielectrics[28–30]. In multilayer MoS_2, the gate control of the electron density in the channel is weakened with increasing MoS_2 thickness. When the MoS_2 thickness is larger than the maximum depletion width, W_{max}, the electrostatic gating loses control over the electrons in the excess part of the MoS_2 film beyond W_{max}. This situation is well known in the partially depleted silicon-on-insulator (SOI) technology. If there is no energy barrier at the source or drain terminals, the electrons in this excess MoS_2 will contribute significantly to the leakage current. The potential advantages of multilayer MoS_2 are, then, offset by a high I_{off}, leading to a significantly reduced I_{on}/I_{off}. Hence, identifying the optimum thickness range is of significance for material synthesis and practical device application of the 2D TMDs. For digital logic applications, I_{on}/I_{off} of at least 10^3 is generally required[31]. In this work, we will use this $I_{on}/I_{off} = 10^3$ ratio as a design criterion, especially when an optimum layer thickness is concerned for achieving high performance with acceptable I_{on}/I_{off}. In view of performance variation associated with probable non-uniformity with unintentional *n*-doping in the starting MoS_2 material as well as from device fabrication, this work builds on a statistical study of the key device parameters in order to gain a comprehensive understanding of the switching properties. Specifically, we investigate the thickness-dependent I_{on}/I_{off} in multilayer MoS_2 by a statistical analysis of more than 80 devices in a wide thickness range. Differences in I_{on}/I_{off} are large amounting to several orders of magnitude with increasing layer thickness. The optimum layer thickness is defined by W_{max}, beyond which I_{on}/I_{off} is reduced below 10^3.

Results

A schematic representation of a back-gate multilayer-MoS_2 transistor used in our work is shown in Fig. 1a, whereas a typical top view photomicrograph of a fabricated device is given in Fig. 1b. Isolated MoS_2 flakes on the SiO_2/Si substrate were exfoliated from a bulk MoS_2 crystal using a conventional mechanical exfoliation technique[32]. The sample preparation and device fabrication are detailed in Methods. The thickness of different flakes, *t*, was measured by means of atomic force microscopy (AFM), as illustrated in Fig. 2. Only one channel length of 10 μm is used for all devices and it is defined by the spacing of a Cu grid shadow mask. However, the channel width that is determined by the width of the flakes varies in the range of 2–60 μm as a result of the stochastic nature of the MoS_2 exfoliation process. The source and drain metal used in our devices is 50 nm Au with a 5 nm thick Ti adhesion layer. The Ti adhesion layer that is in intimate contact with MoS_2 has a work function of ~4.3 eV, which is very close to the conduction band edge of thin-layer MoS_2[9,33]. Furthermore, Ti is a transition metal with its *d*-electron orbitals mixing favorably with the 4*d* states of Mo and resulting in an increase in the density of states at the Fermi level and a strong Fermi level pinning at the contact[9,34,35]. Therefore, this favorable interface geometry is expected to facilitate a good chemical bonding and allow for a maximized electron injection at the source/drain contacts with an increased overlap between the states at the interface.

The transfer characteristics of a multilayer-MoS_2 FET shows a typical *n*-type unipolar carrier transport behavior (Fig. 3a). This confirms a rather small (<0.1 eV), if not negligible, Schottky barrier height (SBH) for electrons at the Au/Ti-MoS_2 contacts (Supplementary Fig. S1). The SBH for holes is, thus, high (>1.2 eV) since the sum of electron SBH and hole SBH should approximately be equal to the energy bandgap (1.3 eV) of MoS_2 (inset in Fig. 3a). Tunneling through the Schottky barrier at the metal/MoS_2 contacts not only limits the charge injection in the device at its on-state but also plays a critical role when evaluating the device off-state in the subthreshold region of the transistor. The small electron SBH facilitates the injection of accumulated electrons at positive gate voltage, V_g, while the large hole SBH suppresses the injection of inverted holes at negative V_g. This results in the *n*-type unipolar behavior with a high I_{on}/I_{off} and is in stark contrast to the ambipolar conduction behavior in graphene FETs with a low I_{on}/I_{off}[32]. The FET with a 30-nm-thick multilayer MoS_2 in Fig. 3a operates as a depletion-mode FET with a large negative threshold voltage, V_t, and a high I_{on}/I_{off} of 10^5. All the FETs fabricated in this work exhibit the same *n*-type characteristics, regardless of the thickness of the MoS_2 film in channel (Supplementary Fig. S2).

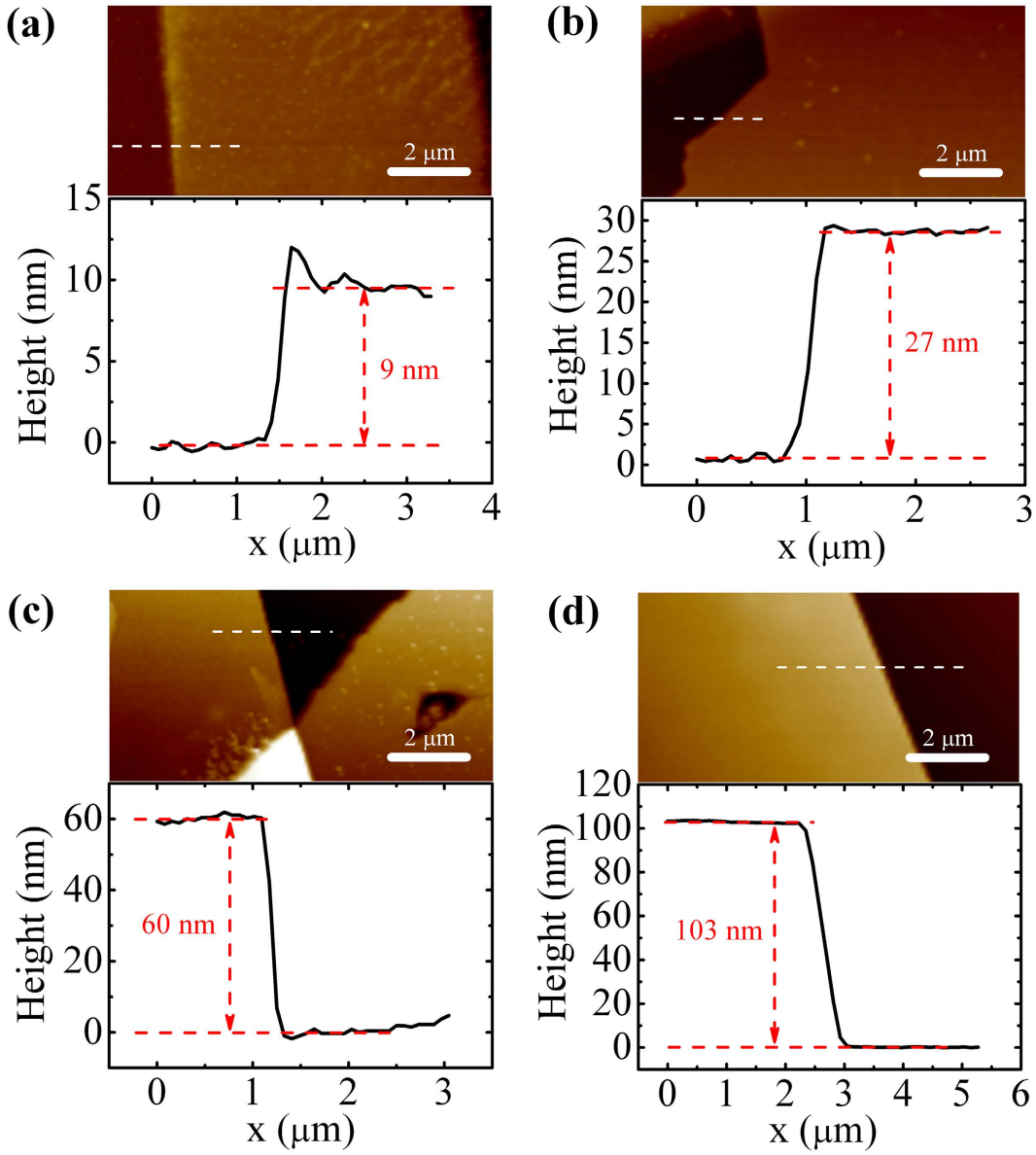

Figure 2. (**a–d**) AFM images of 9, 27, 60 and 103-nm thick MoS_2 films on SiO_2/Si substrate. The height profiles are measured along the dashed lines in the images.

The depletion-mode nature of the transistors will set a limit on the thickness of the multilayer MoS_2 films primarily determined by the preset $I_{on}/I_{off} = 10^3$ as an acceptable specification. Over 80 multilayer-MoS_2 FETs were fabricated and characterized. Their I_{on} and I_{off} versus t ranging from 6 nm to 225 nm are plotted in Fig. 3b. The minimum I_{off} occurring for the smallest t is limited by the noise level in the devices. A clear trend is observed for I_{off}; it increases rapidly with increasing t below 100 nm. Beyond $t = 100$ nm, I_{off} becomes comparable with I_{on} and is almost independent of layer thickness. The stochastic variation of the flake widths makes the variation of I_{on} with t unspecific. However, I_{on}/I_{off} is unaffected by the width variation due to the same width-dependence of I_{on} and I_{off}[36]. In the first 20–30 nm, I_{on}/I_{off} exhibits a gradual decrease with increasing t, see Fig. 3c, likely caused by the I_{off} variation. This is followed by an exponential decrease in I_{on}/I_{off} with t until it approaches unity for $t > 100$ nm. This is better seen in the inset of Fig. 3c where the best linear fit to the logarithmic I_{on}/I_{off} versus t in the range of 20–100 nm gives

$$\log_{10}\left(\frac{I_{on}}{I_{off}}\right) = 8.24 - 0.087t \quad (1)$$

It is well known that in the monolayer 2D materials, the charge carriers are confined in the 2D planes. This confinement can result in some unique characteristics not common in 3D materials, *e.g.* Si. When the layer thickness is increased, the carriers can hop freely between neighboring layers and move in the whole 2D layered

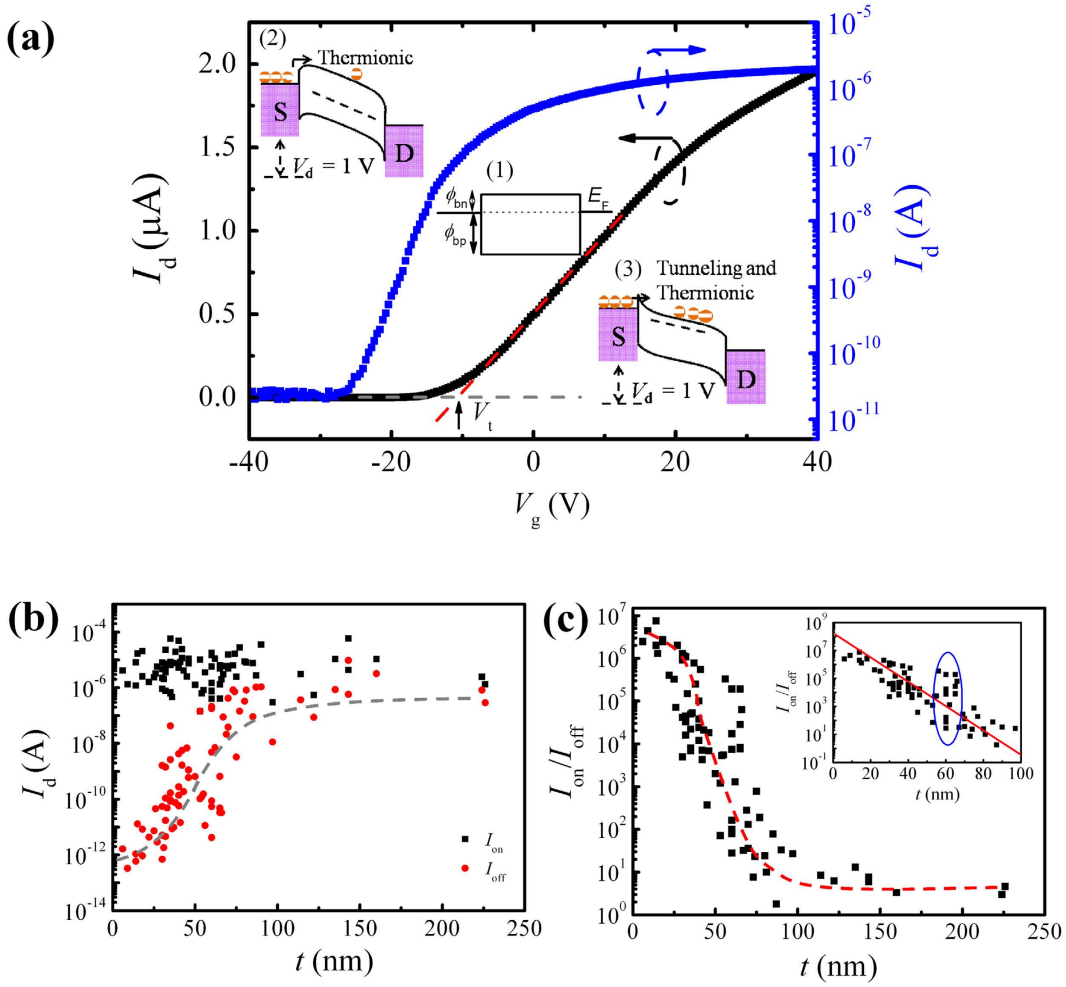

Figure 3. (**a**) Transfer characteristics of a representative transistor with a 30-nm-thick MoS_2 film on a linear scale (left y-axis) and a log scale (right y-axis). The threshold voltage, V_t, is determined by the intercept on the x-axis with the regression fitted line to the linear scale characteristics. The insets represent the energy band diagrams corresponding to the applied V_g in three distinct regions: (1) at flat band, (2) below threshold, and (3) above threshold. ϕ_{bn} and ϕ_{bp} indicate electron and hole SBH, respectively. (**b**) Dependence of I_{on} and I_{off} on MoS_2 flake thickness. The grey dashed line serves as a guide to the eye. (**c**) Thickness-dependence of I_{on}/I_{off}. The red dashed line serves as a guide to the eye. Inset is the zoom in for the first 100 nm. The red solid line in the inset is a linear fit on the semi-log scale.

material[37]. As a result, the carriers distribute fairly uniformly in the 2D material. In this aspect, multilayer-MoS_2 films can be approximated as a homogeneous semiconductor and simulated with traditional device simulators. We have therefore used a commercial simulation tool SILVACO TCAD[38] to numerically solve the coupled Poisson and continuity equations for the multilayer-MoS_2 FETs. Our focus here is on charge and current distributions in MoS_2. For simplicity, the electron SBH is set to 0.1 eV and the unintentional n-doping concentration, N_d, in MoS_2 is assumed to be 3.5×10^{17} cm^{-3}, in order to attain identical V_t between the simulation and experiments. The doping concentration[39] in MoS_2 is found to vary from 10^{16} to 10^{19} cm^{-3}. The other material parameters used in the simulation are shown in Supplementary Table S1[11,39,40]. The simulated transfer characteristics of multilayer-MoS_2 FETs for various channel thicknesses (Fig. 4a) and the variation of I_{on}/I_{off} with t (Fig. 4b) are in good agreement with the experimental results. In particular, the simulated I_{on}/I_{off} shows a steep decrease with t around ~50 nm, matching very well with the data in Fig. 3c. This critical thickness is strongly correlated with W_{max} that is related to N_d by the following formula[36]:

$$W_{max} = \sqrt{\frac{4kT\varepsilon_s\varepsilon_0}{q^2 N_d} \ln \frac{N_d}{n_i}} \quad (2)$$

where, k is the Boltzmann constant, T is absolute temperature, q is elementary charge, ε_s is the relative dielectric constant of multilayer MoS_2 (~11)[39,41], ε_0 is the vacuum permittivity, and $n_i = 1.6 \times 10^8$ cm^{-3} is the intrinsic carrier concentration in MoS_2 due to thermal interband excitation[11]. The calculated W_{max} with the given N_d is ~60 nm. The spatial distribution of charge carriers is inhomogeneous, due to charge screening, along the depth of the

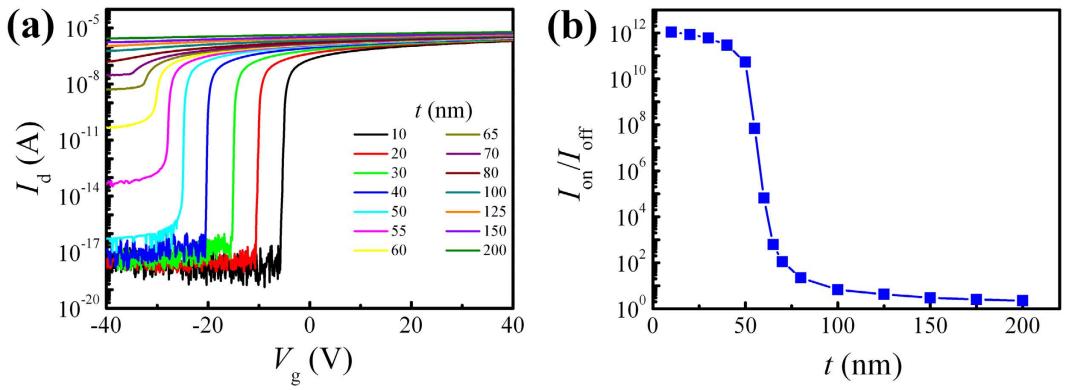

Figure 4. (**a**) Simulated transfer curves of FETs with various MoS_2 thicknesses. (**b**) Simulated thickness-dependence of I_{on}/I_{off}.

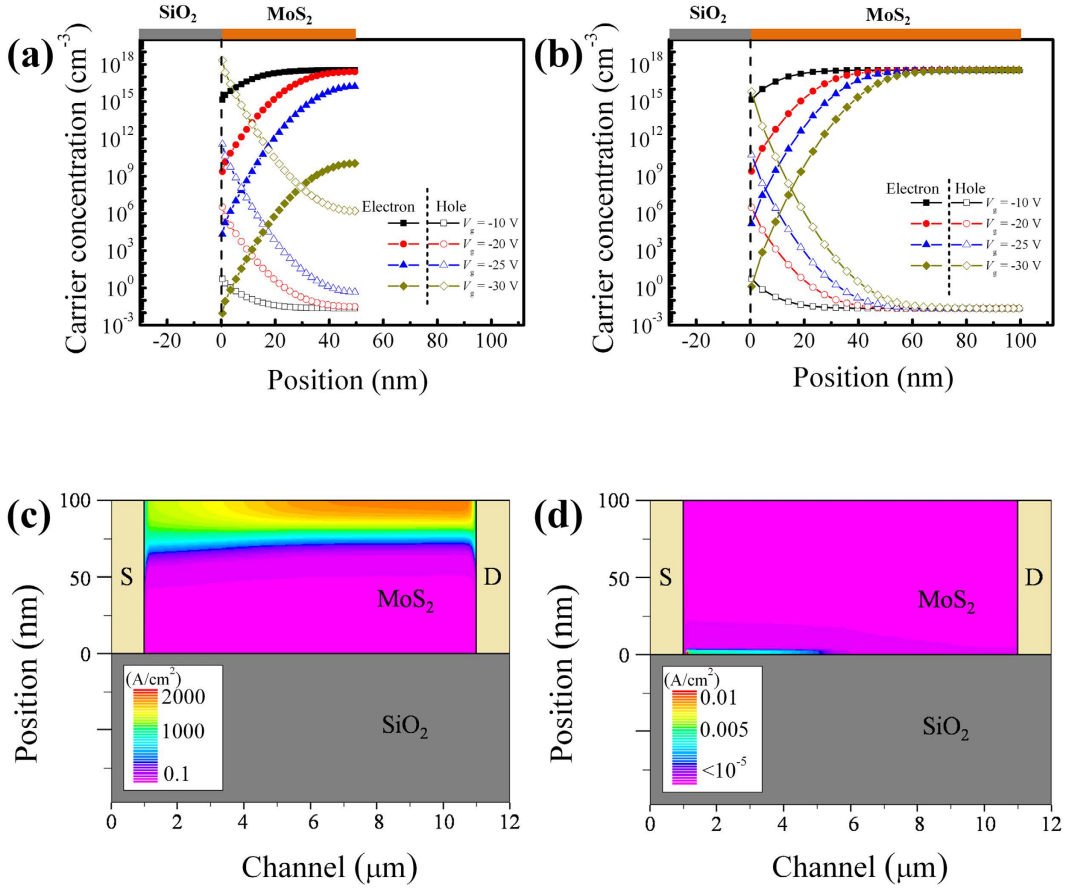

Figure 5. Carrier distribution in 50-nm (**a**) and 100-nm (**b**) MoS_2 at various V_g. (**c,d**) Electron and hole current distributions in a 100-nm-thick MoS_2 at $V_g = -30$ V.

multilayer-MoS_2 film. Specifically, the charge carriers in the MoS_2 layers close to the SiO_2 interface are effectively controlled by V_g. The electrostatic gate control of the carriers are weakened gradually, or even completely lost, in the MoS_2 layers further away from the SiO_2 interface on the account of charge screening.

As the device switching behavior is mainly determined by I_{off}, the carrier distribution at negative V_g is shown, respectively, in Fig. 5a,b for $t < W_{max}$ and $t > W_{max}$. At a negative V_g, electrons are repelled from while holes are attracted to the MoS_2/SiO_2 interface. For $t < W_{max}$, electrons are depleted in the whole MoS_2 film at $V_g < -25$ V. Simultaneously, an inversion layer populated with holes is formed at the MoS_2/SiO_2 interface. However, when $t > W_{max}$, the carrier concentration close to the sample surface (away from the MoS_2/SiO_2 interface) remains constant independent of V_g. This is a result of charge screening effect that results in a poor electrostatic control of the electrons in the excess part of the MoS_2 film. This high and uncontrolled electron concentration in this excess

MoS_2 close to the sample surface, shown in Fig. 5c, contributes to I_{off}. Although a hole inversion layer is formed under large negative V_g, the hole conduction current can be neglected due to a large SBH at the contact interfaces (see Fig. 5d).

It is established now that W_{max} is an important parameter determining the switching behavior of multilayer-MoS_2 FETs. When $t \ll W_{max}$, the electrons can be fully depleted from the entire channel region under negative V_g and an excellent switching behavior with a very low leakage current prevails. Under such circumstances, I_{on}/I_{off} is rather insensitive to t, as manifested by the slowly descending I_{on}/I_{off} with t shown in Figs 3c and 4b. When t around W_{max}, the electrons in the excess part of the MoS_2 film cannot be fully depleted easily. An exponential decrease in I_{on}/I_{off} by about 4 orders of magnitude with t changing from 30 to 65 nm. Moreover, W_{max} depends on doping concentration. The stochastic doping concentration in the MoS_2 flakes can induce a variation in W_{max}, which in its turn results in a large spread in the switching property at ~60 nm (indicated by a circle in the inset of Fig. 3c).

Discussion

In view of its significance in device physics, design and fabrication, quantifying the transistor switching behavior as a function of the layer thickness of the 2D semiconductor materials is of vital importance. A critical parameter W_{max} is discussed when characterizing layered TMD semiconductors such as MoS_2 as the channel material in FETs. Both experimental and theoretical studies show $W_{max} = 50–60$ nm for the multilayer-MoS_2 FETs. At this thickness, the FETs are characterized by an acceptable I_{on}/I_{off} around 10^3. If the multilayer-MoS_2 film is thinner than this W_{max}, an excellent switching behavior with a low leakage current and a much higher I_{on}/I_{off} (than 10^3) will prevail. If the multilayer-MoS_2 film is substantially thicker than this W_{max}, a large leakage current will persist and the switching behavior becomes inferior. An exponential decrease in I_{on}/I_{off} is found in the 20–100 nm thickness range, by a factor of 10 for each additional 10 nm. The findings in this work are useful in guiding material synthesis and designing advanced FETs with layered TMD semiconductors. It appears that the device physics established for traditional semiconductors such as Si is applicable for the layered TMD semiconductors, as it should be.

Methods

Thin MoS_2 flakes were peeled off from bulk MoS_2 (SPI supplies) by mechanical exfoliation. They were subsequently transferred to a heavily doped p-type Si substrate with a 300-nm-thick thermally grown SiO_2. The SiO_2/Si substrate was pre-cleaned by sonication in acetone, isopropyl alcohol, and deionized water. The transferred MoS_2 flakes were identified using an optical microscope (Keyence digital microscope VHX-600). The thickness of the MoS_2 flakes was measured using AFM (Dimension 3100 with Nanoscope IIIa controller, Veeco) operated in tapping mode under ambient conditions. In order to avoid contamination from photolithography or electron-beam lithography, a 10-μm spacing copper grid was placed on top of the thin MoS_2 flakes as a shadow mask for the electrode fabrication. A bilayer stack Ti/Au of 5/50 nm thickness was then deposited by means of electron-beam evaporation as the source and drain electrodes. The heavily doped Si substrate was used as the common back gate for the fabricated MoS_2 FETs. Electrical characterization of the devices was carried out in a shielded probe station with Keithley 4200 semiconductor characterization system in ambient environments.

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Acknowledgements

This work is supported partially by the National Natural Science Foundation of China (Nos 61204090 and 61171010), Fundamental Research Project of young teachers to enhance research capacity, Fudan University (No. 20520133248), State Key Laboratory of ASIC & System, Fudan University (No. 2015MS005), the Swedish Research Council (No. 2014-5591) and the Knut & Alice Wallenberg Foundation (No. 2011.0082).

Author Contributions

Z.-J.Q. conceived the research and analyzed the results. Y.Z., H.W. and H.X. carried out MoS_2 device fabrication. Y.Z. performed AFM analysis and electrical characterization. H.L. performed TCAD simulation. Z.-J.Q., S.-L.Z. and R.L. wrote the manuscript. All authors discussed the results and commented the manuscript.

Additional Information

Supplementary information accompanies this paper at http://www.nature.com/srep

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Zhang, Y. *et al.* Thickness Considerations of Two-Dimensional Layered Semiconductors for Transistor Applications. *Sci. Rep.* **6**, 29615; doi: 10.1038/srep29615 (2016).