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Implantable neurotechnologies: a review of integrated circuit neural amplifiers

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Abstract

Neural signal recording is critical in modern day neuroscience research and emerging neural prosthesis programs. Neural recording requires the use of precise, low-noise amplifier systems to acquire and condition the weak neural signals that are transduced through electrode interfaces. Neural amplifiers and amplifier-based systems are available commercially or can be designed in-house and fabricated using integrated circuit (IC) technologies, resulting in very large-scale integration or application-specific integrated circuit solutions. IC-based neural amplifiers are now used to acquire untethered/portable neural recordings, as they meet the requirements of a miniaturized form factor, light weight and low power consumption. Furthermore, such miniaturized and low-power IC neural amplifiers are now being used in emerging implantable neural prosthesis technologies. This review focuses on neural amplifier-based devices and is presented in two interrelated parts. First, neural signal recording is reviewed, and practical challenges are highlighted. Current amplifier designs with increased functionality and performance and without penalties in chip size and power are featured. Second, applications of IC-based neural amplifiers in basic science experiments (e.g., cortical studies using animal models), neural prostheses (e.g., brain/nerve machine interfaces) and treatment of neuronal diseases (e.g., DBS for treatment of epilepsy) are highlighted. The review concludes with future outlooks of this technology and important challenges with regard to neural signal amplification.

Keywords

Neural recording amplifier; Central nervous system; Peripheral nervous system; VLSI; Integrated circuits

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Compliance with ethical standards

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1 Introduction

Microelectronic recording interfaces are widely used in neuroscience research as well as in diagnostic and therapeutic technologies. The high-quality amplification of weak neural signals remains a challenge in both data acquisition and diagnostic devices. Important examples of neural recordings include electrocorticograms (ECoG) [9, 35, 57, 126, 130] and electroneurograms [134]. In addition, neural recordings are essential for brain–machine interfaces [59] and closed-loop therapeutic devices that interface with the brain [9, 15], nerves [22, 116] or visceral organs [44]. The key requirements in the above applications are to acquire, amplify and process neural signals using low-noise amplifiers and associated signal conditioning circuits [143, 152]. The amplified and processed recordings may then be used in research, clinical diagnostics or, in the case of closed-loop therapeutic devices, functional electrical stimulation.

Neural recordings can be acquired using commercially available amplifier systems [42, 87, 102, 137]. However, custom-designed neural recording ICs offer several prime advantages, including miniaturized form factor, low weight and low power consumption. These properties allow for portable and implantable neurodevices. The first neural amplifier IC was reported by Dorman et al. [32]. Continuous advancements in microelectronic fabrication technology and novel circuit design techniques have benefited IC neural amplifiers with steady and significant improvements, particularly regarding the noise-versus-power tradeoff. The area density of such IC chips has also increased in line with Moore’s law [65], which has thus far correctly predicted the continuing progress in shrinking transistor sizes with simultaneous improvements in IC performance. Despite the progress made in IC-based neural amplifiers, designing such amplifiers is still a non-trivial exercise, requiring expertise in circuit design and in-depth familiarity with the biological aspects of neural recording. This review includes the background design concepts and considerations of neural signal recording and discusses the state-of-the-art design technologies. A survey of applications in neural engineering and prosthetic systems that benefit from these technologies is also given. The review concludes with future outlooks and challenges in the evolution of neural amplifier design and applications.

2 Background on neural recording amplifiers

2.1 Neural signal characteristics

Neural amplifiers are biopotential amplifiers that are specifically designed to amplify and condition bioelectric signals that arise from the nervous system, both central and peripheral. The characteristics of neural signals are presented in Fig. 1 [143]. Neural signals are characterized by their signal bandwidth (frequency content) and amplitude. They are generally smaller in amplitude than electrical signals of the heart and muscle, and they span low- (below 100 Hz) to mid-range (10 s of kHz) frequencies. Thus, neural amplifiers require high-gain and low-noise characteristics. Meeting these design requirements is technologically challenging and requires specialized design strategies.

2.1.1 General neural recording setup and challenges—The foremost challenge in biopotential recording of neural signals is to acquire, with high quality, neural potentials

in the presence of noise inherent to the electronics and electrodes and noise due to external electrical interference. As shown in Fig. 1, neural signals are typically small in amplitude; therefore, the electronic noise of the amplifiers and all electronic components remains a major consideration. Inherent electronic noise includes the thermal and flicker noise sources within the amplifier's transistors and the supporting circuitry within the amplifier. External sources of interference include unwanted biopotential signals, such as myoelectric potentials arising from muscle contractions, non-biological signals, such as AC power (Fig. 1), and radio frequency signals in the environment [143, 152].

Such interfering noise sources are at least an order of magnitude larger than neural signals of interest and can potentially mask or corrupt the acquired neural signal. To suppress such interference as much as possible, neural recording is universally performed using the differential recording setup illustrated in Fig. 2 [143]. In a differential recording setup, a signal electrode is placed close to the neurons of interest, and a reference electrode is placed at a nearby location within the same volume conductor. The subject is also grounded via another electrode to establish a proper bias condition for the inputs of the neural amplifier. With this configuration, an interfering noise source, $V_{\text{intereference}}$, would induce a signal across Z_{GND} that appears as a common-mode signal at the differential inputs of the neural amplifier. For a perfect differential amplifier having an infinite common-mode rejection ratio (CMRR), infinite input impedance and zero electrode impedance, this common-mode signal would be completely suppressed. However, in practice, such circuit parameters are not obtainable. The CMRR of neural amplifiers typically ranges from 70 to 120 dB, which is sufficient for suppressing common-mode interference in most biopotential recordings. A common oversight is ignoring the use of the ground electrode or accidentally creating a high-impedance ground electrode. This results in large common-mode interference that overwhelms the front-end amplifiers, despite a high CMRR [81]. Although electrical shielding would reduce this common-mode interference by reducing the induced current coupled into the amplifier, it is not always practical to shield the lead wires and the amplifiers. Therefore, a high CMRR is an important and desired characteristic.

2.2 General neural amplifier system architecture and design considerations

The basic structure of neural amplifier systems is shown in Fig. 3. The neural signals are transduced by neural probes [10, 90, 144], such as surface or subdural electrodes for recording ECoG signals or microelectrodes for recording neural spikes or action potentials [99]. However, neural signals are first preamplified by a front-end amplifier. This amplifier should have the lowest input-referred noise and higher gain than the subsequent stages, as the RTI noise of all subsequent stages are referred back to the electrodes through the gain of this amplifier [52]. The subsequent amplifier stages composed of one or more cascaded amplifier configurations provide additional gain, limit the signal bandwidth (to filter noise) and drive external loads, such as the input of an oscilloscope or a digitizer. After the neural signals are amplified, they can be processed and observed via analog signal processing methods. This can be as simple as visualizing the waveforms on an oscilloscope or telemetering using an analog radio transmitter [32]. The amplified signals can also be digitized and post-processed using algorithms that are run either on-chip [16] or off-chip on digital post-processors.

Minimizing the total power consumption for such neural recording systems is an important task, especially for such systems that are designed for portable applications or implantation. When a neural amplifier IC is used for portable recording applications, it is usually powered via a compact and reliable power source (e.g., a battery) [11]. Portable recording applications using neural amplifier ICs need to consume minimal power to allow for the use of small batteries while extending operation time. When a recording device containing a neural amplifier IC is implanted for chronic recording, the device should generate less than 40 mW/cm^2 of heat flux to prevent heating the surrounding nerve tissues by more than 2 °C, beyond which tissue/nerve necrosis occurs [146]. Neural amplifier ICs that consume low power certainly helps in achieving this requirement. If the implantable system is powered via electromagnetic induction, the body adsorption loss leads to a poor power transfer efficiency and therefore requires an electromagnetic power source to emit a high level of electromagnetic power through bodily tissues. Ensuring electromagnetic power emissions are maintained below regulatory levels [60] is particularly challenging. Therefore, low-power neural amplifier designs are essential to mitigating this challenge.

In addition to noise and power considerations, the size of IC neural amplifiers is an additional consideration when they are used for portable or implantable applications. Both applications require a highly miniaturized integrated system with a small IC area and overall system footprint. In general, both the chip area and power consumption of any neural amplifier are dependent on the application and design process (the number of active channels, the size of transistors and the wiring). On the one hand, it is desirable to have a small IC die size. On the other hand, it is desirable to maximize on-chip functionality (a large number of channels, post-processing capability, wireless power and communication circuits). A trade-off between the IC die size and functionality is generally required. However, modern circuit designs [77, 92] and IC fabrication technologies [18, 86] have resulted in innovative designs, enabling designers to relax such compromises.

Vulnerability to an electrostatic discharge (ESD) from a charged human operator or during machine-based assembly processes is another critical consideration [33, 115]. This is a particularly serious problem when the amplifier IC is used in dry environments, such as in the operating theater or in dry climates. Although most ICs are designed to meet standard ESD specifications [3, 4], the static electric charges that are typically encountered may result in voltages higher than 25 kV [115], and hence proper ESD design of the ICs and correct device handling procedures are still required. Furthermore, latent and cumulative soft damage occurs when the pins of neural ICs are repeatedly subjected to ESD, as would occur when an unknowingly charged human operator repeatedly handles the IC amplifier terminals. Hence, standard ESD protection handling procedures, such as grounding the subject and surgeon performing the implant must be adhered to when assembling and implanting such sensitive IC amplifiers. Special design considerations also have to be made to mitigate an ESD failure, especially for implanted applications. A typical ESD event would disconnect the input terminals of an IC neural amplifier from the electrodes, disabling the still functional amplifiers' ability to acquire the neural signals. However, a worst-case ESD damage scenario would cause an electrical current to flow from the voltage supply terminal of the powered IC though the input pins to an electrode site. This would lead to uncontrolled

electrical current stimulation of the surrounding biological tissue whenever the device is powered up [61], causing long-term tissue damage.

2.3 Design strategies to minimize power consumption

Decreasing the total power consumption for the system depicted in Fig. 3 can be accomplished at the systems level or at the component level. Here, we describe three system-level techniques commonly used to minimize the power consumed by a neural recording system. The first strategy is resource sharing. The second strategy is power scheduling. The final strategy is power supply voltage reduction.

The first widely used technique consists of multiplexing a high-density electrode array to a much smaller amplifier array. This strategy leverages the fact that not all electrode sites may provide useful information after implantation [97, 101, 145] or that the necessary information can be obtained from a small subset of electrodes, although the useful electrode subset is not known a priori [118]. For example, Al-ashmouny et al. reported a 128-input channel neural recording IC [2] with only 16 inputs selectively routed to the front-end amplifiers, therefore achieving power and area reduction. Another recent work by Lopez et al. [77] adopted the same method and multiplexed 455 electrode inputs to 52 amplifiers.

A closely related technique involves the sharing of power- and area-consuming components within the system. For example, it is common for multiple amplifier channels to share a single ADC or output driver in a time-multiplexed sequence [1, 51, 73, 94]. Chae et al. [16] described a method to minimize the power–area product of a neural recording system though the proper selection of the number of channels that share a single ADC. A recent work by Majidzadeh et al. [78] demonstrated how to share the reference branch of one front-end amplifier among multiple channels. However, this technique cannot be scaled beyond 4 channels due to inter-channel crosstalk.

Power scheduling involves modulating the supply current of individual amplifier channels to reduce the overall power consumption. For example, in [67, 156], when channels were not sampled by the ADC, they were put into a sleep mode where the channel’s power consumption was maintained at a level to minimize the wake-up time. Further, the electrode’s background noise power can vary from site to site due to both the material properties of the electrode and the activities of non-isolated neurons [25]. Therefore, another power-scheduling method is to adapt the current consumption of each amplifier channel according to the background noise present at the respective electrode [17, 122, 141]. For an electrode site that has higher input noise, the power consumption of the corresponding front-end amplifier can be reduced, and vice versa.

Finally, reducing the supply voltage of the entire chip or individual subsystems can be a very effective method to reduce power. For example, the IC neural amplifier reported by Wattanapanitch and Sarpeshkar [141] was partitioned into two separate voltage domains. The front-end amplifiers operated at 1.8 V, while the supply voltage of the ADC and the backend digital blocks were reduced to 1 V to decrease the dynamic switching power. Similarly, Al-ashmouny et al. [2] reported an implementation where the supply voltage of the ADC was made scalable according to the sampling rate, throttling the power

consumption. Finally, the chip reported by Han et al. [48] used 0.9 and 0.45 V supply domains for the amplification stage and ADC, respectively. A dynamic voltage folding circuit then remapped the large output swing of the amplifiers to fit the limited input swing of the ADC.

2.4 Front-end neural amplifier circuit design

The circuit design of the front-end amplifier in Fig. 3 deserves special attention, as the electrical performance of this amplifier directly determines the performance of the overall recording system. Front-end amplifier gains range from 200 to 10,000. The choice of gain is influenced by the required application (CNS or PNS recording) and the system's power supply [107]. The noise introduced by the amplifier is typically designed to be lower than that introduced by the electrodes and, for a majority of neural applications, is maintained below 5 μV_{rms} for amplifiers used to record CNS signals and less than 1 μV_{rms} for PNS-recording amplifiers [76, 105]. The most common front-end amplifier for IC neural recordings was first proposed by Najafi and Wise [89] and then further refined by Harrison [52] to its present circuit shown in Fig. 4.

The input neural signals are AC-coupled through the pair of input capacitors, C_{in}, and feed the shunt–shunt negative feedback network formed by feedback capacitors, C_{fb}, applied around the operational transconductance amplifier (OTA), A_1. The closed-loop gain is therefore accurately defined by the ratio $C_{\text{in}}/C_{\text{fb}}$. The pseudo-resistors formed by PMOS transistors help establish a proper DC negative feedback bias and together with C_{fb} also define the low-side 3-dB cutoff frequency of the neural amplifier. To suppress noise contributions from downstream signal processing stages, a high amplifier gain is desired and achieved by incorporating a high $C_{\text{in}}/C_{\text{fb}}$ ratio (usually by using a large C_{in}), but at the expense of increased silicon area and lowered input impedance. Recent studies have attempted to reduce the silicon area by using smaller unit capacitors or reducing the amplifier gain [77, 78]. However, Ng and Xu proposed relaxing this area–gain trade-off by introducing additional shunt elements onto the negative feedback network [92]. Recent works have also reported that by carefully designing the OTA A1, low current consumption and low input-referred noise are easily achievable [63, 141, 142, 156].

Several metrics have been introduced to quantify front-end amplifier performance. For example, the noise efficiency factor (NEF) characterizes an amplifier's input-referred noise with respect to its current consumption and bandwidth [131]. The NEF is defined as:

$$\text{NEF} = V_{\text{irms}} \sqrt{\frac{2I_{\text{tot}}}{\pi . U_t \cdot 4\kappa T \cdot \text{BW}}} \quad (1)$$

where V_{irms} is the input-referred root-mean-square (RMS) noise voltage, I_{tot} is the total amplifier bias current, U_t is the thermal voltage, κ is the Boltzmann's constant, T is the absolute temperature, and BW is the amplifier's effective noise bandwidth. The NEF is a useful performance metric by which neural amplifiers can be compared, and it represents a

relative measure of how much noise an amplifier produces compared to that of a single bipolar transistor consuming the same bias current.

However, the NEF alone is not a sufficient metric to compare neural amplifiers that are operated at different supply voltages. This inadequacy becomes more pronounced, as recent works have reported operating supply voltages below 1 V [49, 129, 156]. Recently, Muller et al. [86] introduced the power efficiency factor (PEF), which takes into account both the operating current and the supply voltage and therefore provides a better comparison of the amplifier's performance. The PEF is defined as:

$$\mathrm{PEF}=\mathrm{NEF}^2\mathrm{VDD} \quad (2)$$

2.5 Front-end operational transconductance amplifier topologies

As illustrated in Fig. 4, the active amplifying element is generally referred to as an operational transconductance amplifier (OTA). As opposed to an operational amplifier (OpAmp), the OTA does not have a power-consuming output driver circuit, as it does not need to bias any resistive elements other than the high-resistance pseudo-resistor in the feedback network in Fig. 4. Four different CMOS OTA topologies that are often used in neural amplifiers are depicted in Fig. 5. In all cases, the input-referred noise of the OTA arises from the thermal noise and flicker noise of the transistors' conduction channels [43]. The thermal noise of the OTA is inversely related to the amount of bias current supplied to the input differential pair of the OTA (M_1 and M_2), whereas the flicker noise component is inversely proportional to the active gate area of the input different pair. The transistors can be operated in either weak, midor strong inversion, of which the former achieves the highest transconductance (g_m) per unit ampere of bias current. Therefore, to reduce the input-referred noise, the NEF and the PEF, the input transistors are usually operated in the weak inversion region and supplied with a large biasing current. Although the gate areas of the input transistors are usually large to reduce the flicker noise component, the flicker noise reduction is contradicted by the increased capacitance multiplying effect contributed by the parasitic gate area [92]. Hence, the gate areas of the input differential pair must be appropriately sized according to the method described by Ng and Xu [92].

A comprehensive noise-versus-power consumption analysis of the OTAs, as shown in Fig. 5, was performed by Sansen [119], which led to the conclusion that the 2-stage Miller OTA (Fig. 5a) and the symmetrical cascode OTA (Fig. 5b) have higher (worse) obtainable NEFs compared to the alternative topologies. For both types of OTAs, a significant part of the total supply current is only used for maintaining proper biasing and feedback stability at their second stages, leaving less current to bias their input differential stages and therefore leading to a higher NEF. The telescopic cascode OTA (Fig. 5c) achieves the lowest NEF among the listed OTAs, as all of the supply current is devoted to biasing the differential pair, allowing it to obtain a higher input g_m (and hence lower noise and NEF) compared to the prior 2 OTAs. Indeed, previous studies [53, 98, 128], which used either a symmetrical cascode OTA or a 2-stage Miller OTA, reported NEFs ranging from 4 to 17. Recent works [94, 149], which used the telescopic cascode OTA, achieved consistently low NEF values below 2.6.

For recording systems that must operate at supply voltages below 2.5 V and that must be implemented with CMOS processes lacking transistors with low threshold voltages, the telescopic cascode OTA cannot be used, as it requires at least 2.5 V to operate. Instead, the folded cascode OTA (Fig. 5d) is the natural choice for front-end amplifiers operating at supply voltages below 3 V and requiring low NEF and PEF values [103, 141, 142].

Wattanapanitch et al. [142] further proposed an NEF optimization scheme for low-voltage neural amplifiers implemented using the folded cascode OTA, which were adopted in later studies [103, 141].

Resource sharing, which is generally employed at the system level, can be used to increase the power efficiency of the front-end amplifier. The term current reuse is used to describe amplifier topologies that share the biasing current among additional active elements or across channels. Figure 6 (reproduced from [74]) shows an example currentreuse amplifier topology. Here, two complementary input pairs (P1, N1) and (P2, N2) are used within the same amplifier, which allows the NEF to be reduced by a factor of √2. If the g_m of the NMOS and PMOS is assumed the same, the g_m of the amplifier increases by a factor of two for the same amount of biasing current. This leads to a reduction in the thermal noise component of the input-referred noise (and hence the NEF) by a factor of √2. Amplifiers using this topology achieve state-of-the-art noise performance [49, 129, 156]. Although this current-reuse technique is a promising method for reducing the thermal noise component, it doubles the gate capacitance of the input differential pair. Thus, the gate area optimization technique proposed by Ng and Xu [92] must be used to reduce the input-referred noise due to flicker noise and capacitor transformer effect for the complimentary input pairs.

3 Applications of neural amplifiers

3.1 Neural amplifiers for studies of the central nervous system (CNS)

CNS-based IC neural amplifiers have widespread applications ranging from basic science research in animal models to translational research with human subjects. Most CNS-based neural amplifier systems have signal band-widths that are constrained to either acquire action potentials (AP), also called spikes, typically in the range of 200 Hz to 10 kHz, or to local field potential (LFPs) with a typical bandwidth of 0.1–200 Hz. By constraining the amplifiers to record only within the bandwidths of interest, the noise contribution from the amplifier is significantly reduced and therefore improves the recording quality. CNS amplifiers have also been developed that can acquire both types of signals, separately filtering, amplifying and outputting each signal type [46, 86, 100]. The next subsection discusses the state-of-the-art neural amplifier ICs. The subsequent subsections discuss some reported applications where IC neural amplifiers are used in CNS research.

3.2 State-of-the-art CNS neural amplifier IC designs

Neural amplifier ICs were first designed to meet the need for compact electrical recording of brain activities. In 1985, Dorman et al. [32] reported a single chip that contained three front-end amplifiers and a radio transmitter that relayed the recorded signals to an off-chip display. Similarly, Wise and Najafi reported a 10-channel amplifier system (Fig. 7a) that was

integrated with a neural probe [89]. The steady reduction in fine-line CMOS technologies has contributed to increased channel counts [6, 77] and expanded capabilities, such as on-chip analog-to-digital conversion [49, 156] and digital radio transmission [16, 67]. Another emerging trend includes on-chip signal processing, such as spike detection [16, 54] or other forms of data compression [108, 132, 155] to reduce the amount of transmitted data. These design choices are driven by the trend of packing increasingly higher numbers of recording channels on a single IC and the desire of researchers to have more integrated features. These needs require more power-efficient methods to send recorded data off-chip.

Table 1 summarizes several IC neural amplifiers for CNS studies and their specifications and performances. Of note is the reduction in the process dimensions (smallest features), which has been reduced to 180 nm. Another area of continued improvement is the reduction in total power consumption of the ICs. Various solutions in Table 1 achieve hundreds of channels while meeting the criteria of a small die size, low power consumption and low noise.

3.3 Application of neural amplifiers for brain science

IC neural amplifiers are used by neuroscientists to study the CNS of living organisms. Typical neuroscience studies involve inserting electrodes [10, 90, 144] into specific regions of the cortex to acquire neural electrical activity. IC neural amplifiers then amplify and condition the weak cortical signals for post-processing and analysis. The primary goal of such studies is to understand how the activities of groups of neurons are related to sensation, behavior and cognition [14, 117]. Such neurophysiological investigations simultaneously record from dozens of neurons involved in specified behavioral tasks, for example, while an experimental subject performs motor or sensory tasks. Anesthetized and tethered preparations yield invaluable information [27, 34, 56, 72]. Nevertheless, neuroscientists increasingly seek to study animal subjects while naturally behaving. This requires recording systems with a high degree of miniaturization, a small form factor and reduced weight. Often, such systems are powered using miniaturized and light-weight battery packs [36] or wireless power transfer systems [135]. With continuous improvements in IC design and fabrication technology, IC neural recording systems can be now integrated with wireless telemetry for data and, in some cases, wireless power transfer [67, 94]. This has enabled many neuroscientific studies that incorporate freely roaming animal models. The following paragraphs summarize recently reported neural recording IC systems that have been successfully used with common animal models.

The most common animal model for studying brain is the rodent. Due to their small size, rodents can bear limited weight and, hence, portable neural recording systems for rodent studies must have a small form factor and low weight. For example, Szuts et al. [133] reported a 64-channel neural amplifier chip (*Neuroplat64*) that was mounted onto the head of a rat. The analog output is wirelessly transmitted to a base system for digitization followed by archival and post-processing. This device consumed 645 mW and weighted 52 g. Subsequently, both Ruther et al. [113] and Fan et al. [36] reported a system using a commercially available, wireless neurorecording amplifier head-stage [85, 136] that consisted of a 15-channel neurorecording IC packaged with a radio frequency (RF) IC for wireless data transfer (Fig. 8a). The total power consumption of both the amplifier and the

RF IC was only 21 mW. Having integrated all the necessary components onto 2 chips and powered by smaller-sized batteries, this integrated system weighed just 9 g.

The reported system-on-chip solutions require a battery as a power supply. This adds additional weight that the rodent subjects must bear, which often leads to animal fatigue and limits the duration of experiments. Recently, the chip implementation reported by Lee et al. [67] eliminated the need for a battery by integrating an on-chip inductive wireless power harvester in addition to 32 neural recording amplifiers and an RF transceiver. With intelligent neural amplifier power scheduling, the total chip consumed 5.85 mW and could be powered by a near-field wireless harvesting scheme [64].

Non-human primates (NHPs) are also extensively used for neuroscience studies. Due to the large roaming space required by NHPs, the short-range wireless power harvesting methods described for rodents, such as in [67] and [64], are not sufficient to wirelessly power neural recording systems for NHP studies. All current wireless recording systems for primate studies therefore require a light-weight battery pack, which is often head mounted. For example, Roy and Wang reported a battery-powered neural recording setup [110] based on the same system used in [136] to study the auditory cortex of free-ranging Marmosets over a 5-hour period on a single battery charge.

Nurmikko's group has reported two battery-powered, wireless neural recording systems encased in biocompatible titanium casings [12, 151]. In their first version, as shown in Fig. 8b [12], the casing held a 100-channel neural recording IC, digitizers and a 24-Mbps wireless data link module. Both systems contained an inductively powered battery charger to wirelessly charge the implanted battery, and the second system [151] mitigated charging-induced heating. Weighing only 44.5 g and consuming only 90 mW, the system in [12] has successfully acquired neural recordings from free-ranging Rhesus macaques and swine models for up to 7 h on a single charge.

Shenoy's group has developed four generations of the "Hermes" family of portable wireless neural recording systems [20, 40, 84, 120] that were successfully applied in recent NHP studies [23, 37, 38]. Their latest implementation is the HermesE system, which is composed of a 96-channel neural recording chip with on-chip digitizers and an off-chip UWB transmitter. The HermesE chip was fabricated in an advanced CMOS 0.13-μm process, measured 25 mm^2 and consumed only 6.5 mW.

Wireless recording instrumentation designed for small subjects, such as insects, requires very aggressive reductions in size, weight and power consumption. Harrison et al. [55] reported integrating 2 channels of neural amplifiers, 2 channels of EMG amplifiers, a shared digitizer and a 920-MHz radio onto a single chip. As this design required an operating voltage of 3 V, it was powered by two watch batteries, consumed only 3.6 mW and had a total run time of 2 h. The chip package, batteries and the PCB weighed 0.79 g and were used to perform wireless neural recording from an untethered locust (Fig. 9a) and swimming electric fish [39]. Also reported in the same paper, a second version of the chip was implemented in a finer CMOS 0.35-μm process technology, which allowed the chip to operate at only 1.5 V and hence required only a single watch (button) battery. This chip

consumed only 1 mW and had a longer run time of 5 h compared to the first version. The chip was also directly bonded to a thinner flexible PCB, reducing the total weight of the system to 0.17 g, and was used to record action potentials from the target-selective descending neuron in the nerve cord of a free-flying dragonfly (Fig. 9b). A similar chip reported by Fotowat et al. [135] included 10 neural recording channels and an RF wireless power harvesting circuit. Compared to the chips reported in [55], the chip reported in [135] consumed only 1.23 mW due to the use of more power-efficient neural amplifiers. Without the need for any battery, it weighed 38 mg and had no run-time restrictions.

3.3.1 Neural amplifiers for therapeutic neuromodulation—The information gleaned from the acquisition of neural electrical activity can be used to augment therapeutic stimulation of the nervous system [88]. Neural stimulation can be used to treat neurological diseases of the brain, restore the functions of the limbs, interface and restore functions provided by peripheral or visceral nerves, restore bladder function or relieve chronic pain. For example, deep brain stimulation (DBS) is particularly successful in treating movement disorders, such as Parkinson's Disease, dystonia and essential tremor [5, 24, 83]. DBS is also an alternative treatment for pharmacoresistant epilepsy, pain control and psychiatric disorders [5]. However, current DBS therapies are conducted in open-loop configurations and require periodic visits with a clinician to make adjustments for optimal stimulation efficacy. Closed-loop DBS has been proposed to provide synchronous adaptive neuromodulation based on real-time pathological brain states in each patient [15, 83, 121]. In this paradigm, neural activities are amplified and analyzed to detect disease-state biomarkers; this information is then used to either augment ongoing stimulation or initiate new stimulation. This process is dynamically repeated until the desired therapeutic efficacy is achieved. For example, the Neuropace system (California, USA) [91] is a commercially available device that performs closed-loop neurostimulation for the treatment of epilepsy. Recent studies on patients implanted with this device have exhibited significant reductions in seizures over a sustained period of time, and hence, the patients experience an improved quality of life [8].

Neural amplifier systems can be coupled with a microcomputer module and discrete electrical stimulators to form a complete closed-loop neuromodulation device. However, integration of these modules onto a single neuromodulation chip significantly decreases the form factor and simplifies the packaging required for implantation. Shahrokhi et al. reported a prototype 128-channel neurorecording and stimulator chip [125] with off-chip signal processing for a proposed closed-loop neuromodulation system. Recently, Abdelhalim et al. [1] reported a neuromodulation system-on-chip (SoC) that detects and suppresses imminent epileptic seizures based on fluctuations in phase synchrony within the narrow frequency bands of recorded neural signals. This chip was tested on rat models and off-line human trials. Similarly, Flynn et al. first reported a 64-channel neurorecording and stimulator chip [68] that relied on off-chip signal processing. Subsequently, they developed a closed-loop DBS SoC that contained an integrated power harvester, 4 neural amplifiers, a digital signal processor (DSP), 8 neurostimulators and a two-way wireless transceiver [104]. The on-chip DSP analyzed neural signal frequency content and set stimulation parameters. Another recent work by Wu et al. [19] reported a neuromodulation chip comprising 8 neural

recording amplifiers, a bio-signal processor with 92 % seizure detection accuracy and a high-voltage stimulator.

3.3.2 Application of neural amplifiers for CNS Neuroprosthesis—CNS-based neuroprostheses, or brain–machine interfaces (BMIs), are systems whereby neural electrical activities are decoded and used to control robotic limbs [76, 89, 105] or to stimulate muscles for restoring limb function [35]. Hochberg et al. [57] developed a BMI in which a tetraplegic patient used his thoughts to move a computer cursor to perform simple controls with a robotic hand. This technology has steadily matured. For example, Hochberg et al. and Collinger et al. [26, 58] allowed tetraplegic patients to finely control a robotic hand based on cortical signals representing the patient's intended movement or thoughts. This paradigm can be combined with functional electrical stimulation. For example, Miller et al. [35] used a BMI interface to drive stimulation of hand muscles to restore compromised grasping ability in a macaque model.

The above-reported BMI interfaces have all used neural recording amplifiers to acquire, amplify and digitize neural signals for decoding thought. Currently, all reported BMI experiments with human patients [26, 35, 57, 58, 150] require the subjects tethered percutaneously to a bench-top computer for neural signal acquisition and decoding. Although many of the miniature and lightweight wireless recording systems ICs [12, 20, 40, 84, 120, 136, 151] discussed in the earlier sections of this review would simplify the BMI interface, major regulatory approvals (FCC, FDA, IEC) are needed before these devices can be safely applied to human use (especially for implantable applications).

3.4 Neural amplifiers for the peripheral nervous system (PNS)

3.4.1 PNS neural amplifier design and considerations—Neural amplifiers are also used to acquire signals from the peripheral nervous system. Signals acquired by nerve electrodes, either extrafascicularly or intrafascicularly, generally have extremely small amplitudes. For example, intrafascicular electrodes, such as the transverse intrafascicular multichannel electrode (TIME) and the longitudinal intrafascicular electrode (LIFE), transduce signals that have amplitudes less than 100 μV_{pp} [62, 66, 71, 79, 82, 109]. In addition, the signals transduced by extrafascicular electrodes, such as nerve cuff electrodes, have amplitudes less than 20 μV_{pp} [41, 75, 127, 138]. Hence, to maintain a signal-to-noise ratio of more than 1.5, the peripheral neural amplifiers that are coupled with extracellular electrodes are typically designed with a much lower input-referred noise (<12 μV_{pp}) than normal CNS-based neural amplifiers.

Due to the noise constraints placed on recording instrumentation, electrophysiological recordings from the PNS are largely performed using commercial bench-top low-noise amplifier setups [75, 82, 109] that require subjects to be tethered to the equipment. Until now, there have been limited reports of IC-based PNS amplifier implementations, and existing technologies have generally only been applied to acute experiments. In general, the reported PNS neural amplifiers consume higher power per channel to achieve a much lower noise level for maintaining at least a signal-to noise ratio (SNR) of 2. Uranga et al. [139] reported a neural amplifier chip for the PNS based on CMOS chopper-stabilized amplifiers

with a bandwidth of 3 kHz. Donaldson et al. reported successive generations of very low-noise amplifier chips suitable for interfacing with extrafascicular electrodes (e.g., nerve cuff electrodes) [29, 105, 107, 134]. Recent studies have reported neural amplifiers [107, 134] that employ the velocity selection recording (VSR) technique, first proposed in [106], to selectively amplify weak PNS signals with differing conduction velocities. The ability of VSR to discriminate recorded activity based on fiber type has been validated in several acute in vivo studies [123, 124, 153]; demonstrating this technique in a chronically implanted model would represent a major advancement.

3.4.2 Applications of PNS neural recordings—A promising use of PNS neural recording amplifiers is in neuromodulation and neuroprosthesis systems. Recently, a peripheral nerve-based neuromodulation system for bladder control was demonstrated in rats [22, 28, 80]. Such a device, in human patients, could restore bladder control lost due to spinal cord injury. In this system, neural amplifiers were used to record the afferent activity of bladder sensory nerves and to predict the fullness of the bladder. Upon detecting a full bladder, a neurostimulator issued an electrical current to the ventral roots [22] to activate bladder emptying. Additionally, high-frequency, blocking stimulation was used to prevent inadvertent bladder emptying. Similarly, Sahin et al. [116] demonstrated a closed-loop PNS neuromodulation device to treat obstructive sleep apnea. In a canine model, neural activity was recorded from the hypoglossal nerve and was processed to detect blockages to the upper airway. When a blockage was detected, the system triggered stimulation of the same nerve to open the upper airway and mitigate the blockage.

Recently, peripheral nerve-based motor neuropros-thesis systems have also been reported. Dhillon et al. [30, 31] demonstrated the control of a robotic arm by a human amputee using signals recorded from an intrafascicular electrode interface while also incorporating sensory feedback. Similarly, Jia et al. [62] demonstrated the ability of a human amputee to control a finger extension. Most recently, Micera et al. used peripheral nerve stimulation to evoke graded sensory perceptions in a human amputee subject while using the subject’s residual muscle activity to decode movement intention and actuate a robotic arm (Fig. 10) [82, 109].

Neural recording IC technology has not been widely adopted in PNS-based research or neuromodulation systems. Although neural recording ICs targeted for PNS-based neural prostheses have been proposed [30, 31, 82, 94, 109, 114, 149], demonstrating a fully implanted system, analogous to the works of [74, 149] and [132], is lacking. Hence, the opportunity to utilize implantable IC neural amplification systems for PNS interfacing remains largely unexplored.

The use of neural recording amplifiers in the PNS continues to be an active area of development. For example, Rozman et al. [112] demonstrated neural recording from the nerves innervating the pancreas and proposed using such recordings to achieve closed-loop controlled secretion of pancreatic hormones. As discussed in the last section, there are no reported applications of neural recording ICs for any chronically implantable PNS neuroprosthesis.

3.5 Future outlook and challenges

3.5.1 Expanding applications for IC neural recordings—The role of neural recording ICs is likely to expand with the development of closed-loop neuromodulation therapies. As previously discussed, implanted neural recording ICs can acquire useful signals for closed-loop stimulation for DBS [15, 83, 121], the treatment of epilepsy [1] and the restoration of bladder function [47]. Potential neuromodulation therapies are emerging for hypertension [47], inflammatory disease [96] and heart failure [154], and the ultimate success of these therapies may hinge on the ability to decode relevant biomarkers in real time. Hence, research on neural amplifiers is in a continual state of technological enhancement, promising improvements in the IC process as well as further reductions in power consumption and amplifier noise and increased channel densities.

3.5.2 Amplifier and electrode co-design—The advantages of integrating neural amplifiers as close as possible to the electrode site were first demonstrated in [89]. Numerous works [45, 97, 145] have since built upon this achievement, particularly to scale up the number of electrodes and amplifier channels. Recently, Lopez et al. reported the integration of a 455-active electrode amplifier onto a single shank of a silicon probe (Fig. 11a) [77]. Guo et al. also reported the co-integration of extrafascicular (Fig. 11b) [45] with neural amplifiers, while Ng et al. reported integrating intrafascicular (Fig. 11c) [95] peripheral nerve electrodes with neural amplifiers. The trend of building highly integrated systems is ongoing. However, the challenges regarding integrating CMOS processing (for the IC design) with MEMS processing (for the electrodes and sensors) remain, which include biocompatible hermetic sealing of the IC to prevent moisture absorption and seepage along with active electronic components. Of course, amplifier/electrode co-design introduces more stringent area and power constraints on the neural amplifiers, as they must fit the smaller form factor of the electrode while maintaining low amplifier input-referred noise.

3.5.3 Advancing with Moore’s law—For the past 30 years, the semiconductor industry has faithfully followed Moore’s law, which predicted that the number of transistors in an IC doubles every 2 years. Moore’s law also predicted that the size of transistors (and hence the die cost per transistor) would reduce by half every 2 years. This law has led to a consistent “scaling down” of transistor sizes by IC manufacturers and ushered sub-nanometer scale, fine-line CMOS process technologies. However, CMOS scaling has benefited ICs that contain primarily digital functions, such as the microprocessor and DSP. In fact, scaling has imposed increased design challenges to traditional analog circuits. Designing neural amplifiers, or any analog integrated circuit, in such fine-line, CMOS processes hold numerous challenges, including increased gate and channel leakage [111], increased flicker noise [21, 140] and increased intradie variability [13, 50]. There are more process-related design constraints that must be considered compared to the other mature industrial process technologies [69, 70, 147, 148]. Hence, it may seem that neural amplifiers would not benefit from this continuous CMOS process scaling. On the contrary, some notable neural amplifier ICs have significantly improved according to this trend and have been implemented in sub-100-nm CMOS processes. For example, Ng and Xu reported a neural amplifier system implemented in a 65-nm CMOS process that leverages the complementary characteristics of thin-gate and thick-gate transistors to perform on-chip

analog signal processing [93]. A second reported method involves the migration of analog functions into their equivalent digital logic implementations. For example, Muller et al. digitized nearly the full analog-to-digital conversion chain [86] on a single IC. Finally, certain device “imperfections” can be leveraged as part of the circuit design. For example, Berge and Hafliger used the leaky gate of a transistor to form both the feedback capacitor and the DC bias pseudo-resistor of the neural amplifier, therefore completely eliminating the traditional pseudo-resistor element [7]. In order for the advanced CMOS process technologies to be a viable choice for implementing neural amplifiers, economies of scale must be accelerated, and new circuit design techniques must be devised to address or utilize “imperfections” associated with such advanced process technologies.

4 Conclusion

The neural amplifier is an indispensable part of physiological monitoring systems used in neuroscience research and in commercially and clinically applicable therapeutic solutions. This review discusses the background of neural amplifiers and IC-based realizations in terms of design and application. State-of-the-art implementations and applications for CNS and PNS neural recording ICs are discussed. Semiconductor technology continues to advance, bringing improvements in biopotential amplifier design, their circuit performance and scalability. Further, recent works have demonstrated integration of VLSI circuits and ASICs with microelectrodes and other sensors and have demonstrated system-level solutions. Recently, technologies for large-scale (multichannel) cortical recording and integration of systems for demonstrations in animal models have advanced significantly. Nonetheless, there remains further need to advance the state of the art; for example, in the near future, neural amplifier ICs will enable fully implantable PNS interfaces, enabling closed-loop neuromodulation therapies. Neural recording IC design and matching the novel designs to fully integrated solutions for clinical recording and therapeutic devices remain work in progress. The biggest challenge is making these researchgrade circuits and integrated devices available to the broader research community and to translate such technologies into commercially available and clinically approved products.

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Abbreviations

ADC	Analog-to-digital converter
ASK	Amplitude shift keying
CNS	Central nervous system
CMOS	Complementary metal oxide semiconductor
CMRR	Common mode rejection ratio
FET	Field effect transistor

FSK	Frequency shift keying
IC	Integrated circuit (chip)
IEEE	Institute of Electrical and Electronic Engineers
MOS	Metal oxide semiconductor
NEF	Noise efficiency factor
OTA	Operational transconductance amplifier
OpAmp	Operational amplifier
PEF	Power efficiency factor
PNS	Peripheral nervous system
RF	Radio frequency
UWB	Ultra wide band radio
VLSI	Very large scale integration

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Biographies

Kian Ann Ng received his B.E. degree in electrical and electronic engineering and his M.E. degree in IC design from Nanyang Technological University, Singapore, in 2000 and 2005, respectively. From 2000 to 2009, he held senior technical positions with STMicroelectronics, Chartered Semiconductor Manufacturing and Oxford Semiconductors. He has designed EEG/ECG mixed-signal front ends, switched-capacitor circuits, RF identification circuits, image sensors, ESD/IO circuits, USB (1.0–3.0) SERDES and Firewire SERDES. He has co-authored 3 journal papers and 8 conference papers and holds 3 US patents. Currently, he is a Research Associate and Ph.D. candidate at the National University of Singapore. His research focuses on implantable neural recording systems and peripheral nerve prostheses. Kian Ann is a member of the IEEE and an active committee member of the IEEE Solid-State Circuits Society (Singapore Chapter).

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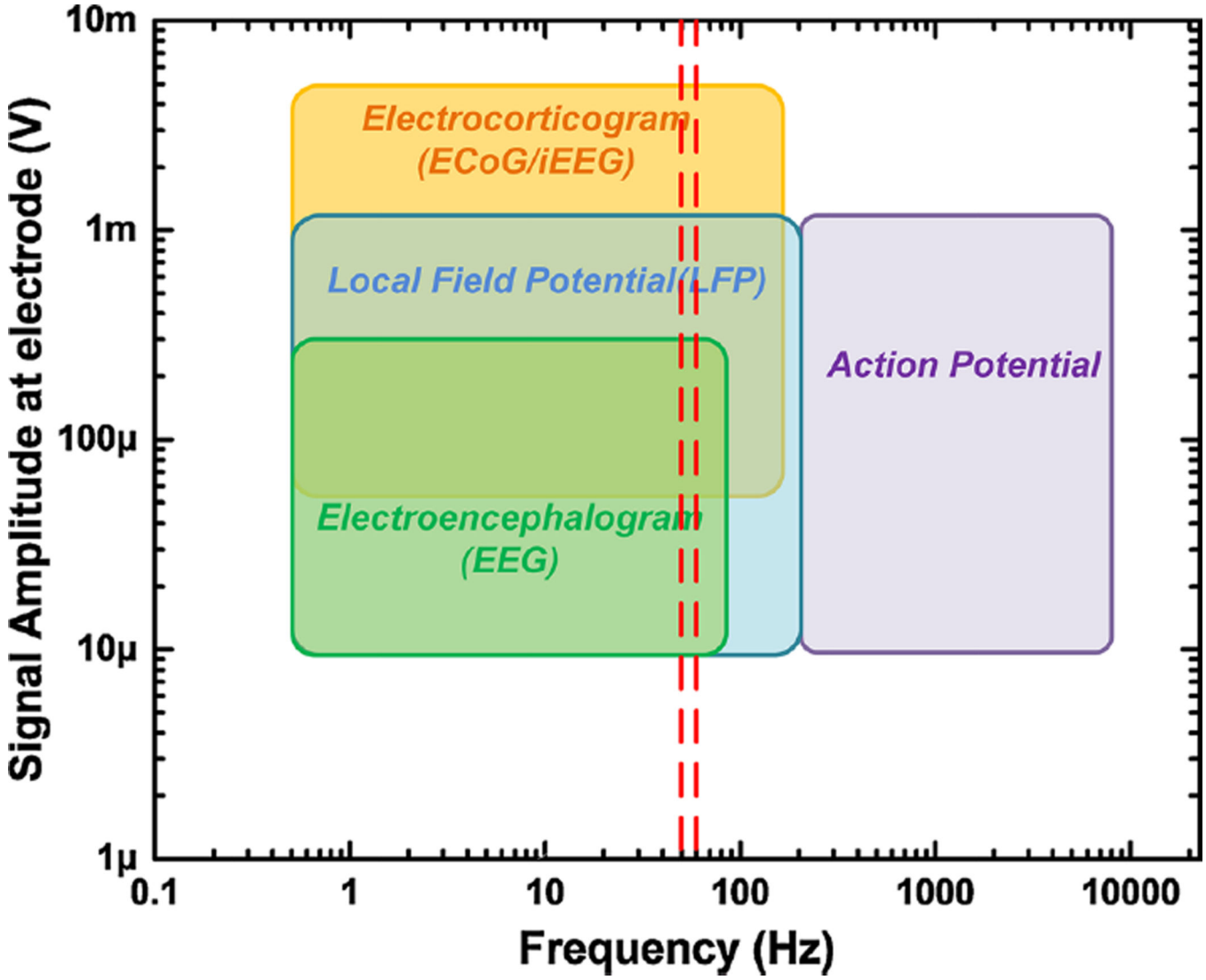

Fig. 1.

Amplitude and frequency ranges of neural signals. EEG signals span relatively low frequencies, whereas neuronal action potentials span high frequencies. The small amplitudes of the neural signals require amplifiers with high-gain and low-noise features. The *two red vertical lines* indicate the most common interference signal frequencies (50 and 60 Hz) encountered during neural signal recording (color figure online)

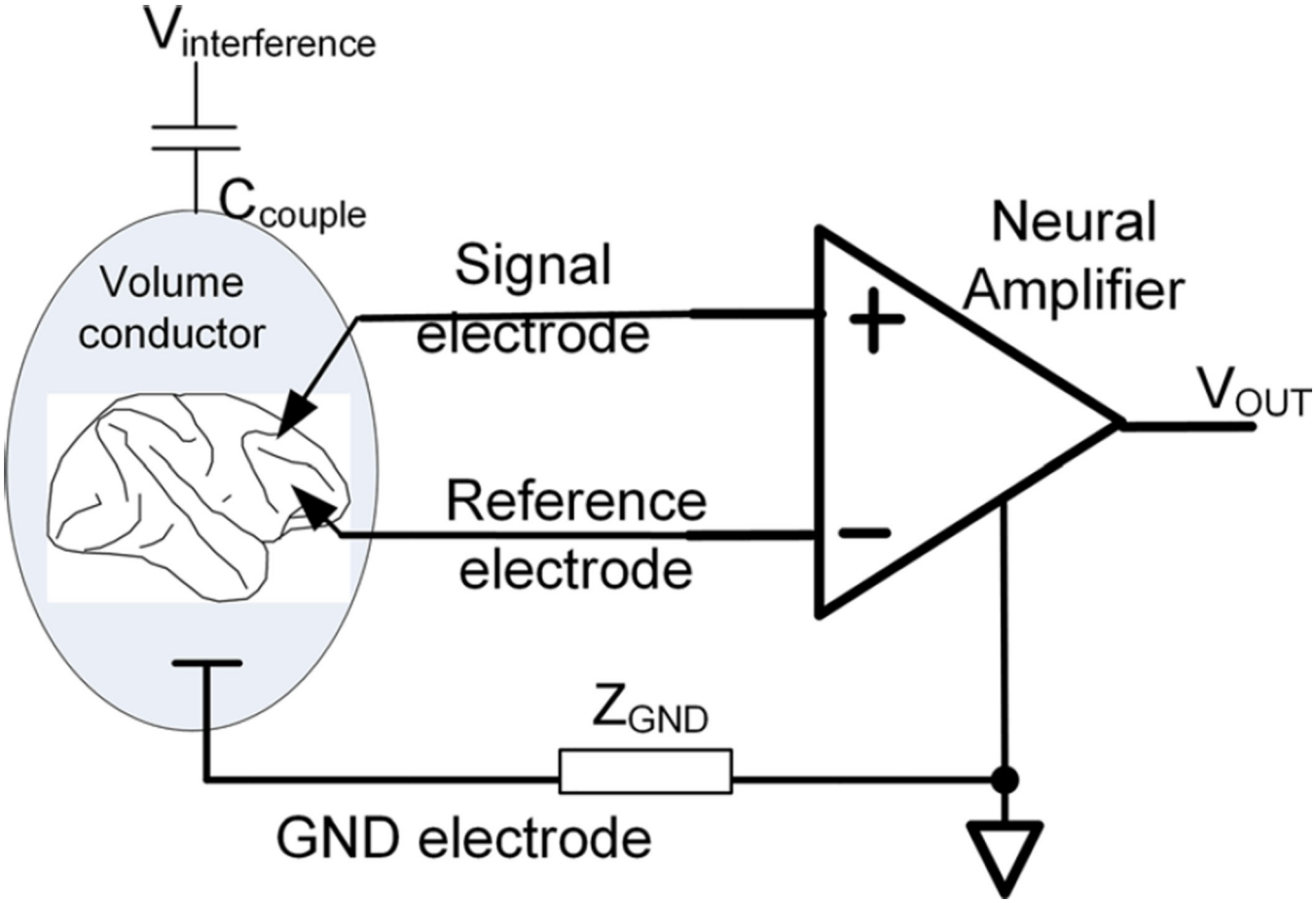

Fig. 2.

Typical differential setup for neural recording. Common-mode electric current is induced into the body through the coupling capacitor, C_{couple}. The desired electrical signals through the signal and the reference electrodes are differentially amplified, while the passage of the induced current through the ground (GND) electrode contributes the common-mode signal

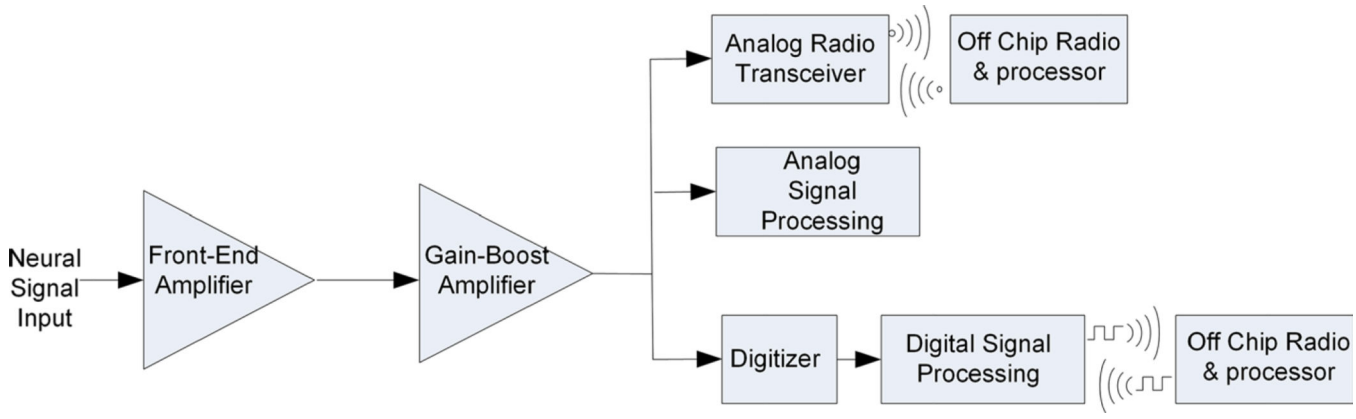

Fig. 3.
General system-on-chip block diagram of neural recording ICs

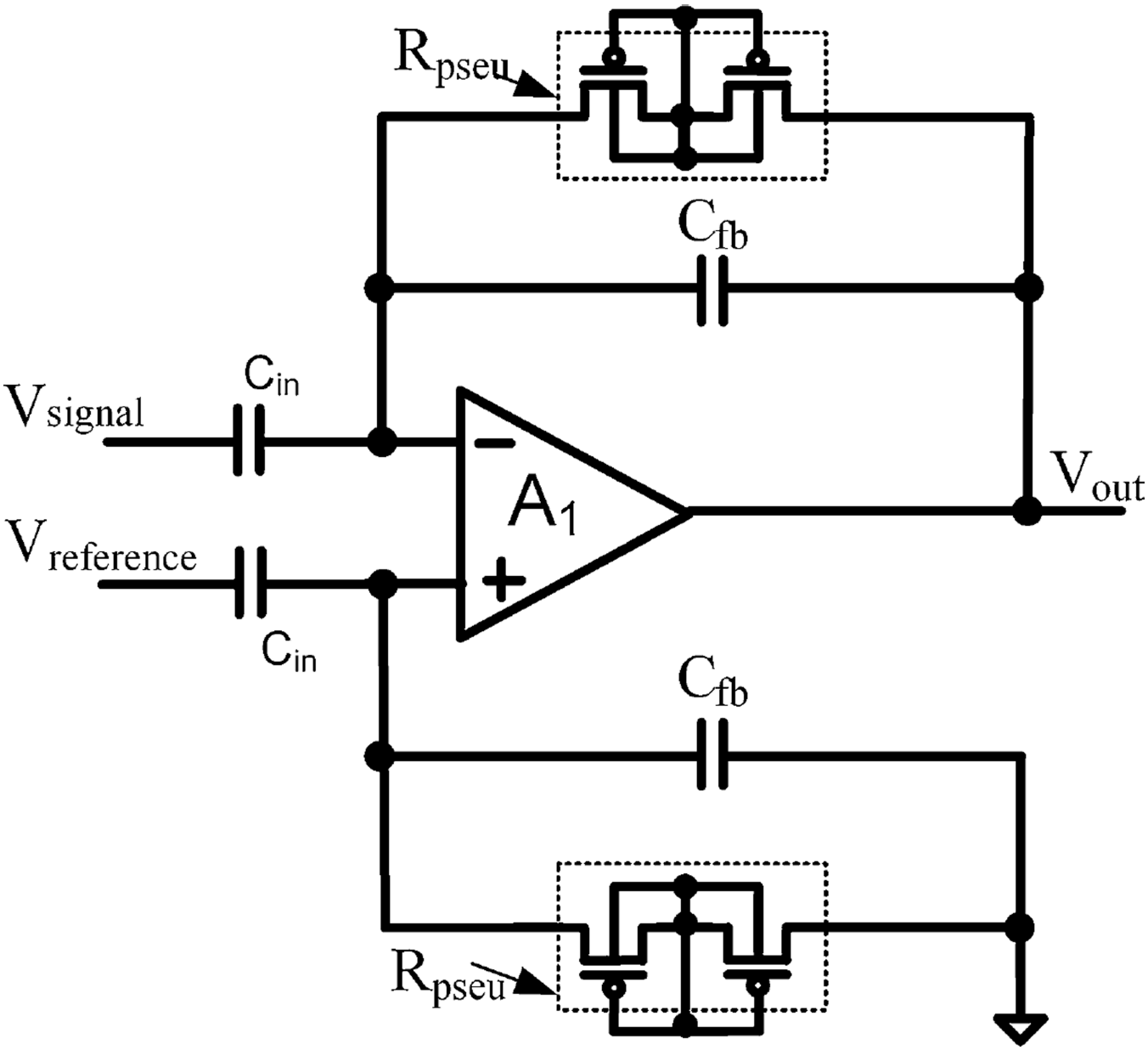

Fig. 4.
Front-end neural recording amplifier as proposed in [52] and explained in the text

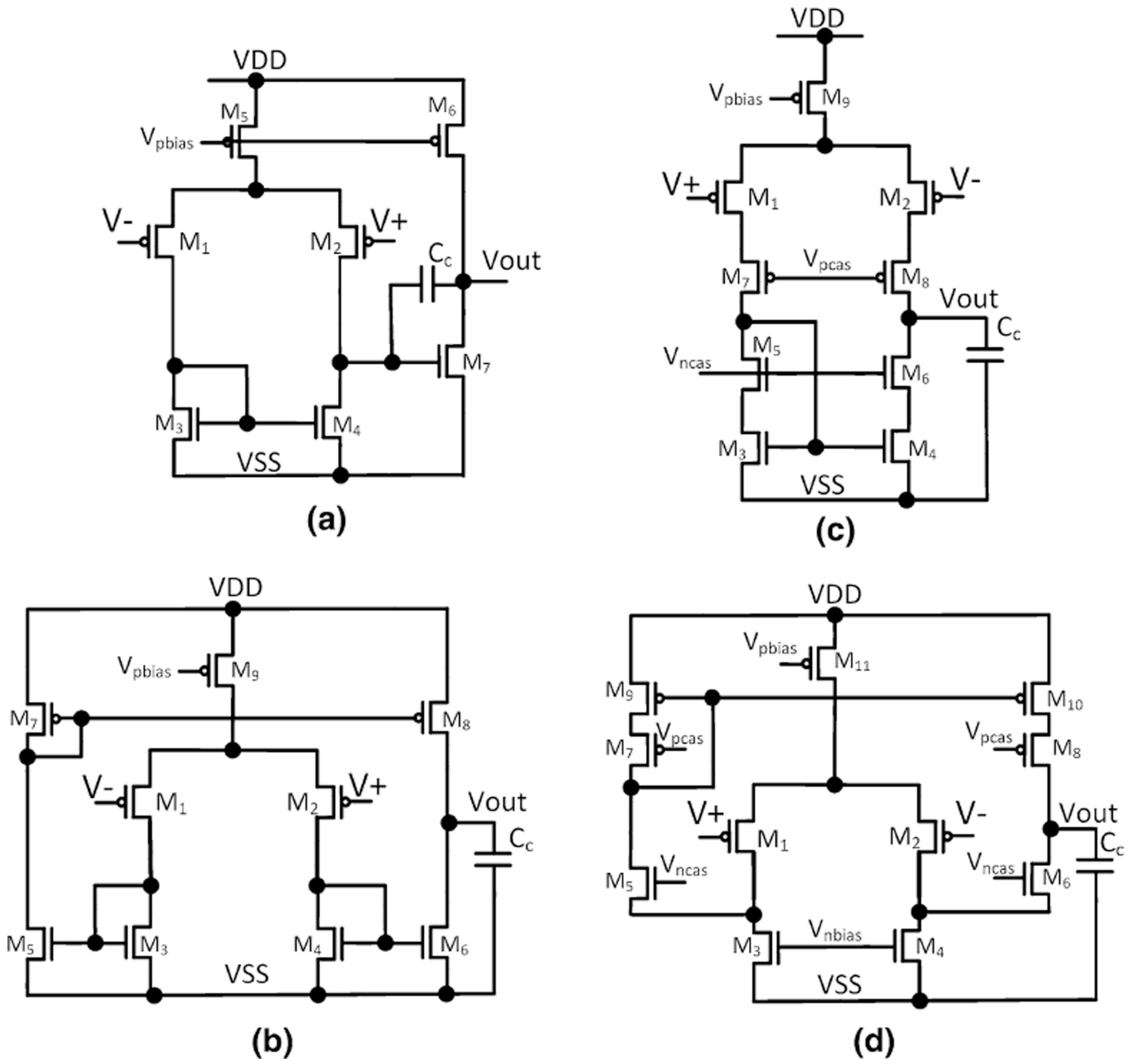

Fig. 5.

Types of operational transconductance amplifiers that are used as the active elements of the capacitive coupled neural amplifier: **a** 2-stage Miller OTA, **b** telescopic cascode OTA, **c** symmetrical cascode OTA and **d** folded cascode OTA

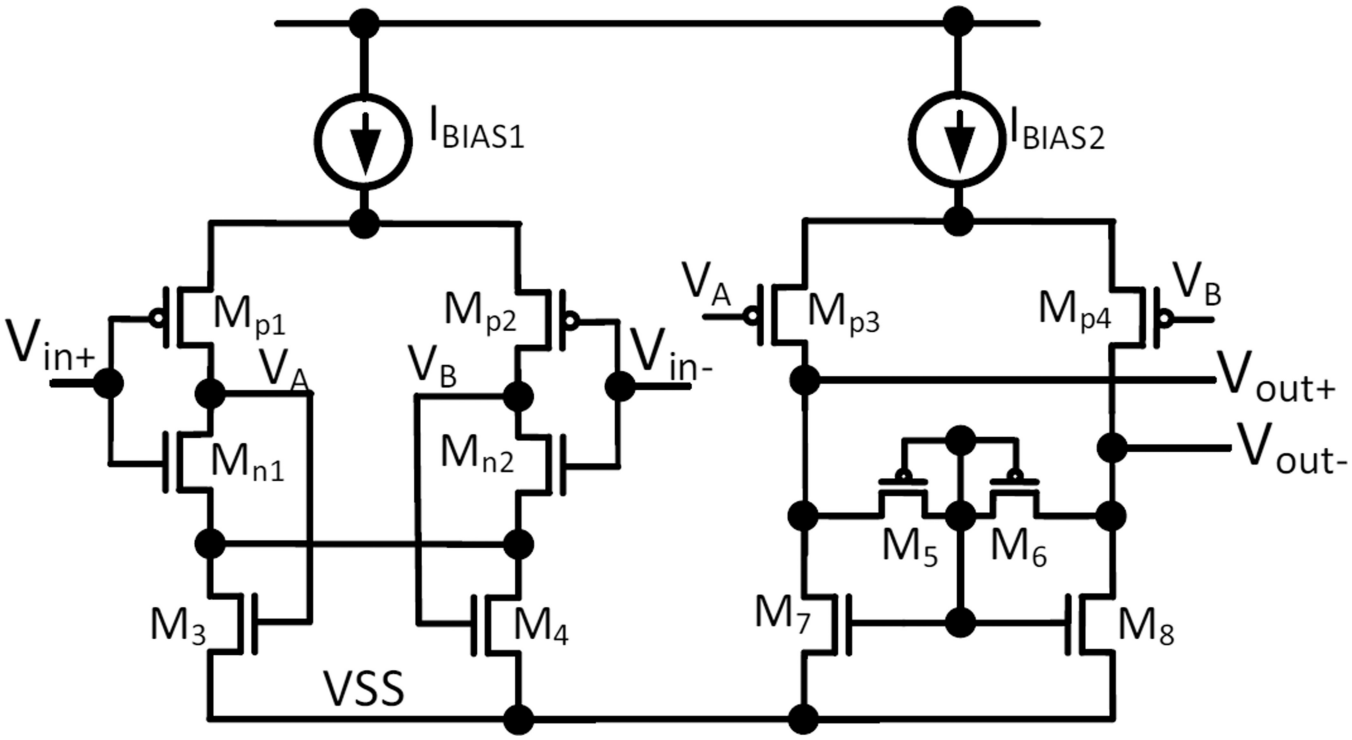

Fig. 6.
An example of the current-reuse OTA proposed by Liu et al. [74]

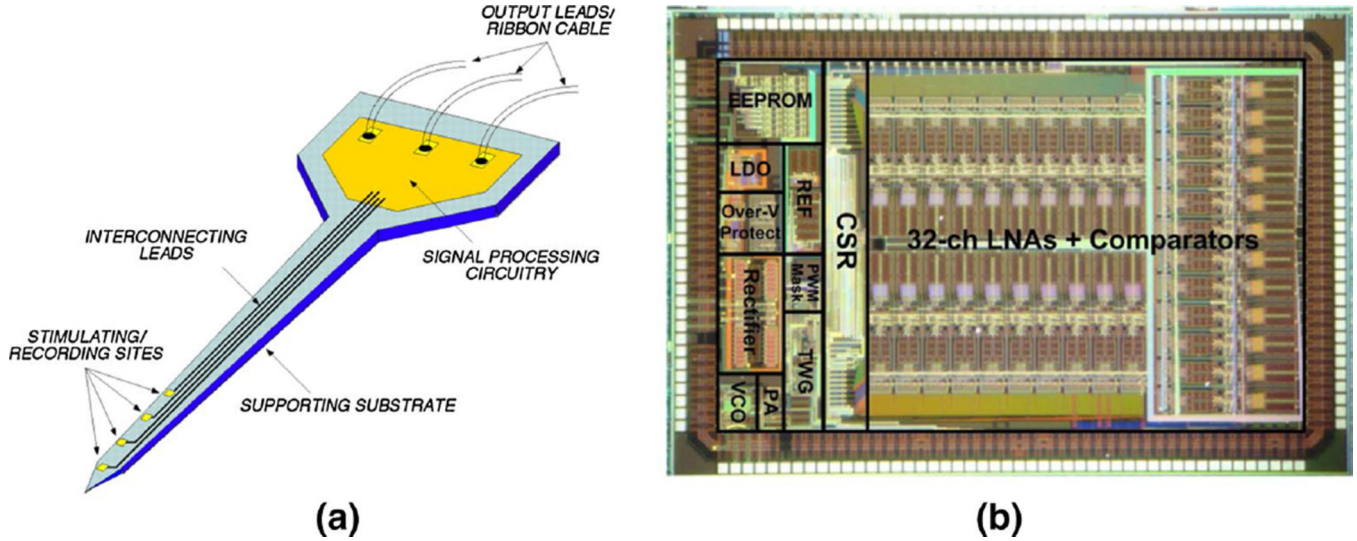

Fig. 7.

a Early manifestation of a complete neural recording amplifier system proposed by Wise and Najafi [89]. **b** A recent state-of-the-art implementation of a neural amplifier system reported by Lee et al. [67]. Measuring 4.9 mm by 3 mm, neural amplifiers, analog-to-digital converters, inductive power harvesting and a digital data transmitter are included on a single chip. Reproduced with permission from IEEE

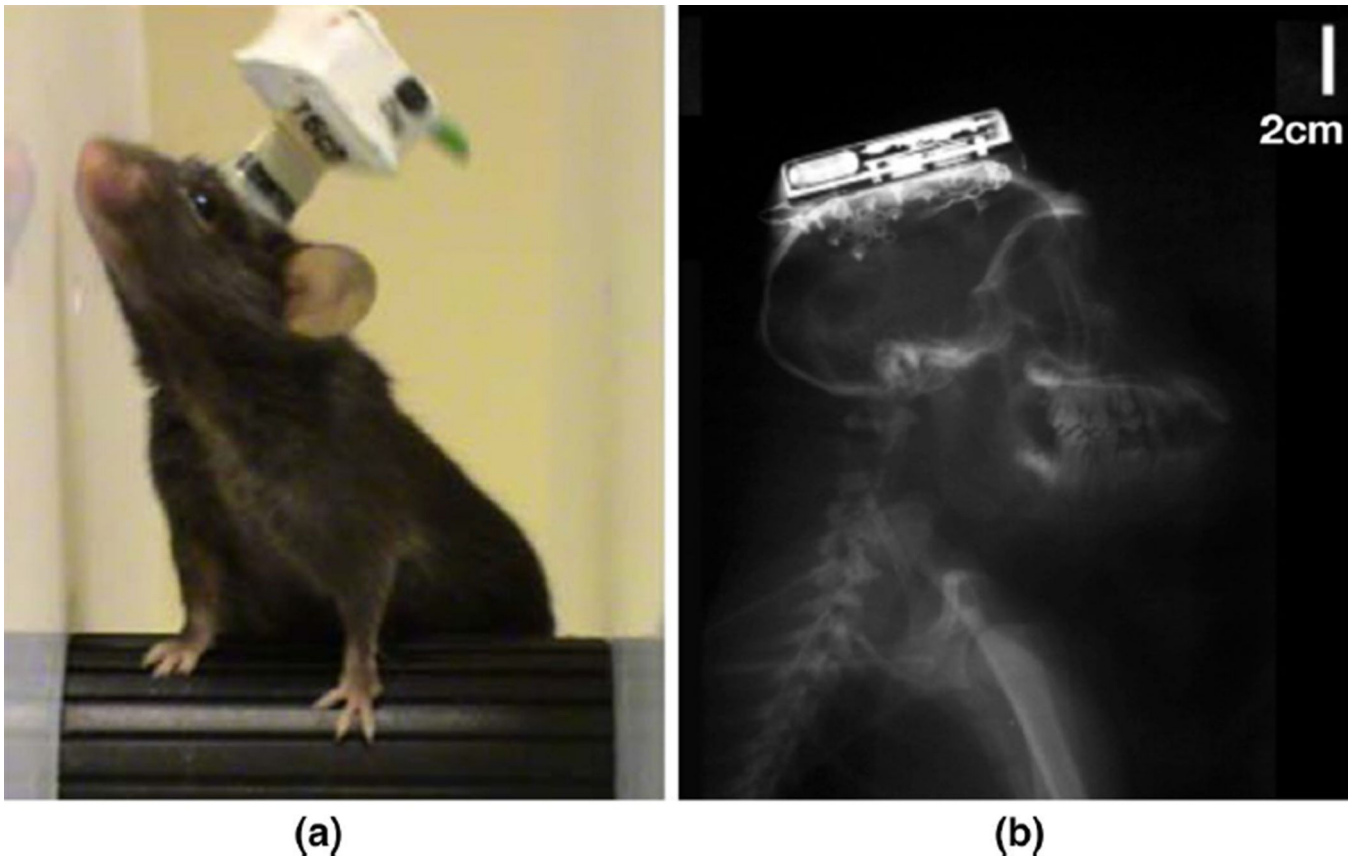

Fig. 8.

a A neural recording system with an RF transceiver for brain studies in a rodent model, as reported by Fan et al. [36]. **b** A similar system for performing CNS studies in a macaque model reported by Borton et al. [12]. (a) Reproduced with permission from IEEE (b) © IOP Publishing. Reproduced with permission. All rights reserved

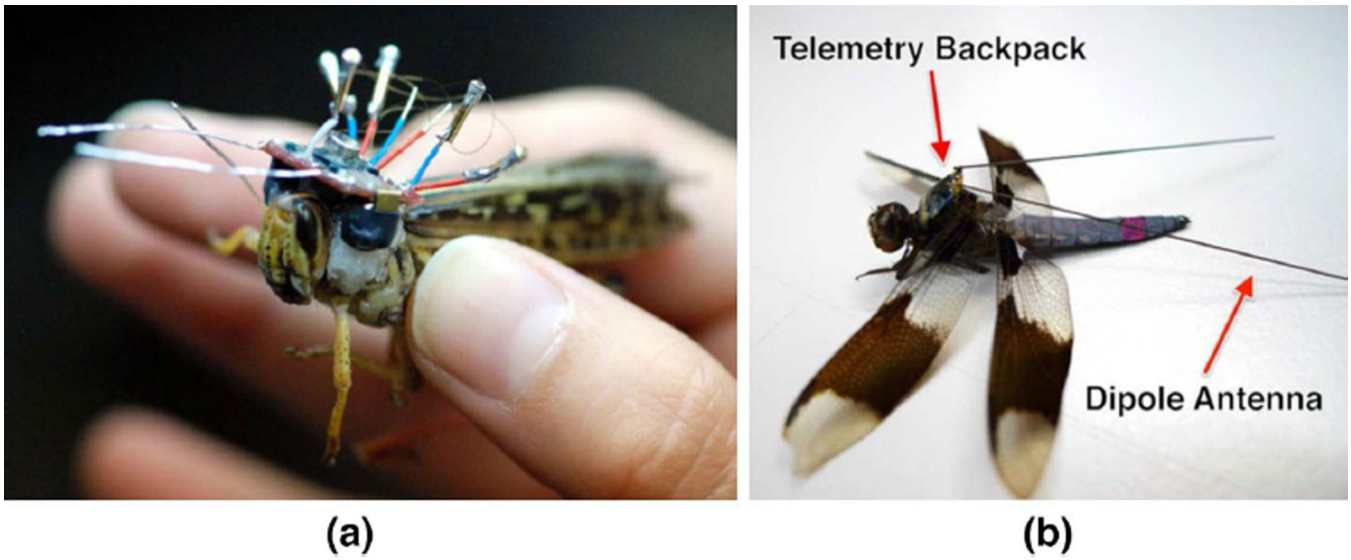

Fig. 9.

Neural recording systems for very small subjects, such as **a** a locust [55] and **b** a dragonfly [135]. Reproduced with permission from IEEE

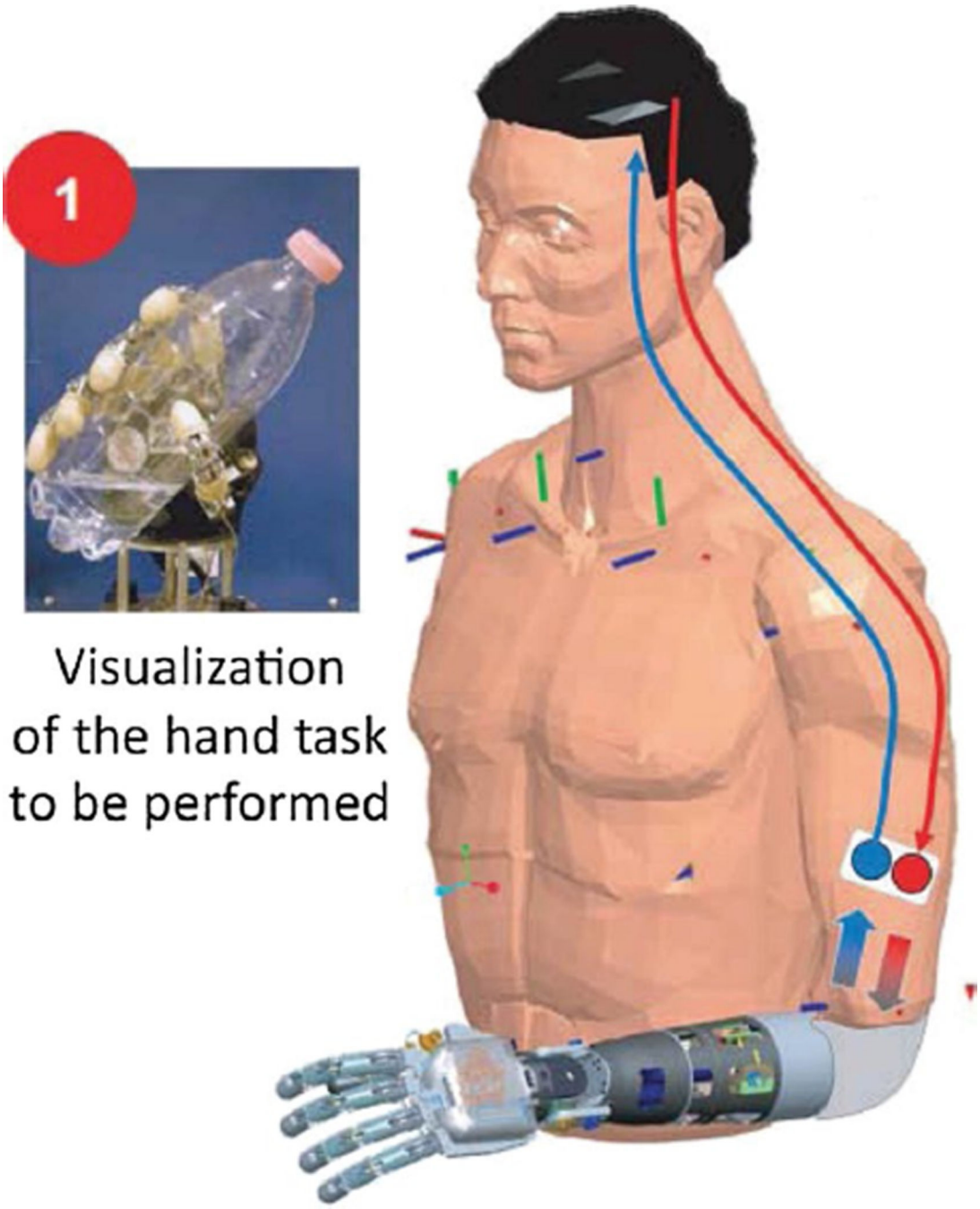

Fig. 10.
A peripheral nerve prosthesis applied to an amputee for a period of 4 weeks [82]. Reproduced with kind permission from Professor Silvestro Micera, EPFL

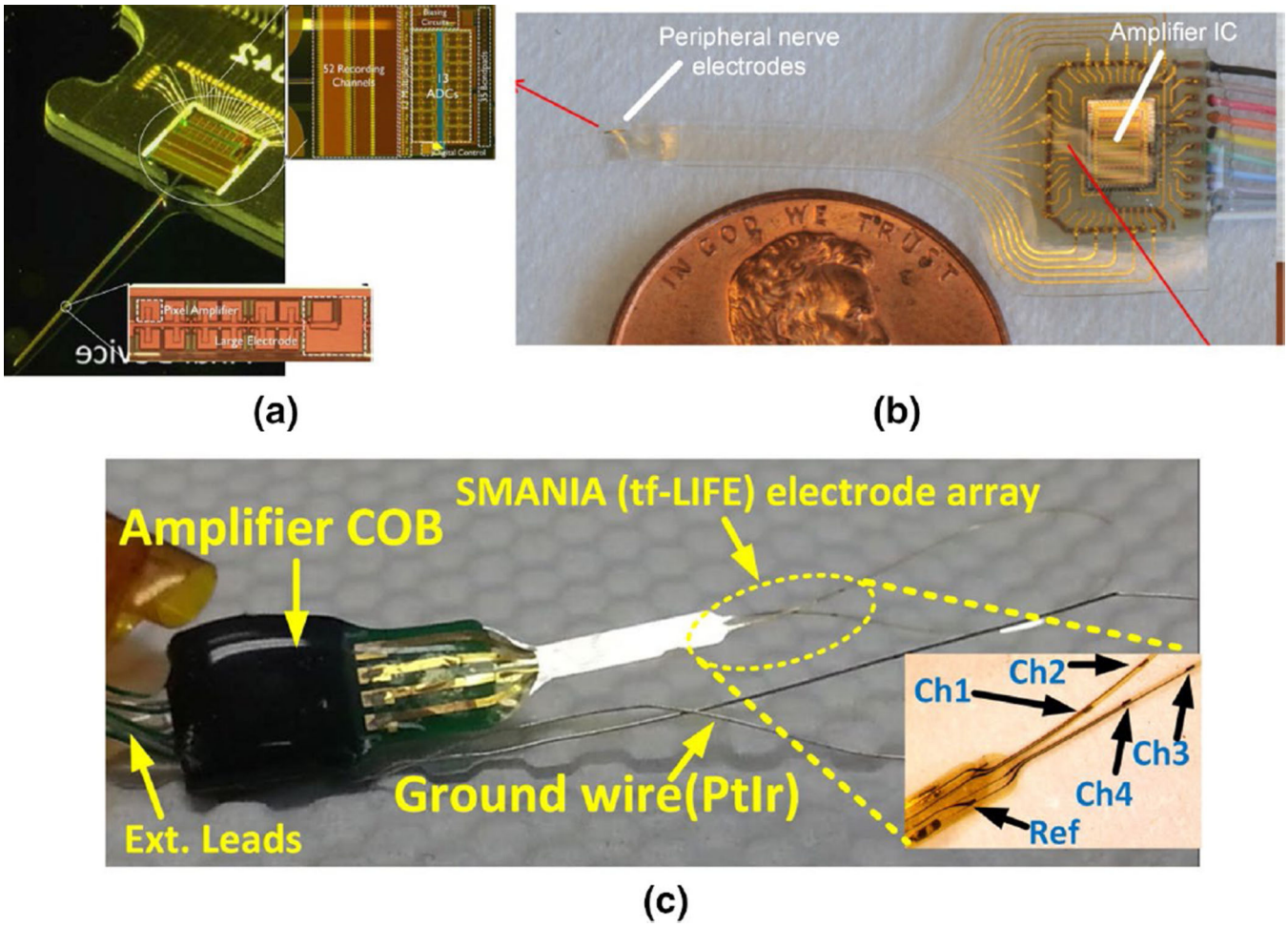

Fig. 11.

Integration of amplifiers and electrodes **a** for cortical interfacing [77], **b** for extrafascicular peripheral nerve interfacing [45] and **c** intrafascicular peripheral nerve interfacing [95]. Reproduced with permission from IEEE

Table 1

Recent works on full chip neural amplifier systems for CNS recording applications

References	**[54]**	**[16]**	**[6]**	**[141]**	**[49]**	**[156]**	**[77]**
Year	2007	2009	2009	2011	2013	2013	2014
CMOS process	0.5 μm	0.35 μm	0.35 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Chip size(mm^2)	27.73	63.3	15.75	9.9	25	28.2	9.6
No. of channels	100	128	256	32	100	100	455(52)
Power (mW)	13.5	6	5.04	0.325	0.094	1.16	1.45
Supply voltage (V)	3.6	3.0	3.0	1.8	0.45	1.8	1.8
Signal bandwidth (Hz)	30–35 k	0.1–20 k	0.01–5 k	0.13–11.7 k	1–10 k	0.38–5.1 k	0.5–6 k
Input-referred noise (μV_{rms})	5.1	4.9	7.0	5.4–11.2	3.2	4.0	3.2
ADC resolution (bits)	10	6–9	None	8	9	9.5	10
Read-out	ASK + FSK telemetry	UWB	Analog	Digital	Digital	Digital	Digital

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