

Quasi-ballistic carbon nanotube array transistors with current density exceeding Si and GaAs

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Carbon nanotubes (CNTs) are tantalizing candidates for semiconductor electronics because of their exceptional charge transport properties and one-dimensional electrostatics. Ballistic transport approaching the quantum conductance limit of $2G_0 = 4e^2/h$ has been achieved in field-effect transistors (FETs) containing one CNT. However, constraints in CNT sorting, processing, alignment, and contacts give rise to nonidealities when CNTs are implemented in densely packed parallel arrays such as those needed for technology, resulting in a conductance per CNT far from $2G_0$. The consequence has been that, whereas CNTs are ultimately expected to yield FETs that are more conductive than conventional semiconductors, CNTs, instead, have underperformed channel materials, such as Si, by sixfold or more. We report quasi-ballistic CNT array FETs at a density of $47 \text{ CNTs } \mu\text{m}^{-1}$, fabricated through a combination of CNT purification, solution-based assembly, and CNT treatment. The conductance is as high as $0.46 G_0$ per CNT. In parallel, the conductance of the arrays reaches $1.7 \text{ mS } \mu\text{m}^{-1}$, which is seven times higher than the previous state-of-the-art CNT array FETs made by other methods. The saturated on-state current density is as high as $900 \mu\text{A } \mu\text{m}^{-1}$ and is similar to or exceeds that of Si FETs when compared at an equivalent gate oxide thickness and at the same off-state current density. The on-state current density exceeds that of GaAs FETs as well. This breakthrough in CNT array performance is a critical advance toward the exploitation of CNTs in logic, high-speed communications, and other semiconductor electronics technologies.

INTRODUCTION

Semiconducting single-walled carbon nanotubes (CNTs) are desirable materials for the active channels of field-effect transistors (FETs) because of their high current-carrying capacity (1), high carrier velocity (2, 3), and exceptional electrostatics due to their ultrathin body (4). Room-temperature ballistic transport approaching the quantum conductance limit of $2G_0 = 4e^2/h = 155 \mu\text{S}$ was first realized in FETs containing single semiconducting CNTs more than a decade ago, demonstrating the exceptional charge transport characteristics of CNTs (5, 6). Realistic approaches for miniaturizing CNT FETs to cutting-edge dimensions that are similar to or smaller than state-of-the-art Si FETs have been established for single CNT FETs with sub-10-nm channel lengths and covalently bonded end contacts that enable aggressively scaled-down electrodes (1, 7).

Future electronic devices made from CNTs will require multiple CNTs per FET. Modeling based on extrapolation of individual CNT characteristics to parallel, aligned arrays of densely packed but well-spaced semiconducting CNTs ($\sim 100 \text{ CNTs } \mu\text{m}^{-1}$) has shown that CNT arrays will outperform conventional semiconductors such as single-crystalline Si in logic devices and radio frequency (RF) amplifiers (8, 9). CNT array FETs are specifically expected to lead to at least a two- to fivefold gain in the energy-delay product of logic devices (8, 10) (thereby enabling faster switching and lower power consumption) while allowing for particularly high-speed RF amplifier devices with excellent linearity (9) (thereby enabling increased data throughput and lower power consumption). These advances in single CNT FETs and the projected characteristics of array FETs have made it clear that CNTs are prime candidates for next-generation semiconductor electronics that promise substantial performance gains.

Recent progress in the alignment of CNTs from solution (11) and via chemical vapor deposition (CVD) (12, 13) processes demonstrates promising scalability; however, achieving the optimal packing density of CNTs in an array and a high conductance per CNT remains to be a challenge. The ideal morphology of CNTs in an array FET consists of a relatively sparse layer of aligned CNTs with a pitch of more than 5 nm (10). It is difficult to form highly conductive contacts to more tightly packed arrays (14), and deleterious inter-CNT interactions arise in tightly packed arrays, which cause screening effects that can decrease both conductance and on/off ratio ($I_{\text{on}}/I_{\text{off}}$) (15). In addition, the ideal CNT array consists of purely semiconducting-type CNTs with a homogeneous band gap. Even a single metallic CNT impurity can short-circuit the FET and lower the $I_{\text{on}}/I_{\text{off}}$ by several orders of magnitude (16).

As a result of these materials science challenges, it has not been possible to approach the quantum conductance limit in FETs based on dense arrays of CNTs while maintaining a high $I_{\text{on}}/I_{\text{off}}$. For example, arrays of semiconducting CNTs, sorted using anionic surfactants, have been aligned and deposited onto substrates from solution via Langmuir-Schaefer assembly at a high density of $1100 \text{ CNTs } \mu\text{m}^{-1}$ and have demonstrated a conductance of $0.25 \text{ mS } \mu\text{m}^{-1}$, corresponding to $0.003 G_0$ or $0.23 \mu\text{S}$ per CNT (17). Wu *et al.* have organized surfactant-dispersed CNTs into aligned rafts with a density of $30 \text{ CNTs } \mu\text{m}^{-1}$, demonstrating a conductance of $0.08 \text{ mS } \mu\text{m}^{-1}$, corresponding to $0.04 G_0$ or $3.2 \mu\text{S}$ per CNT (18). Aligned arrays of CNTs at a density of $100 \text{ CNTs } \mu\text{m}^{-1}$ grown by CVD and purified via selective Joule heating to remove metallic CNTs have demonstrated a conductance of $0.12 \text{ mS } \mu\text{m}^{-1}$, which corresponds to $0.015 G_0$ or $1.2 \mu\text{S}$ per CNT (19). Recent work has also advanced the performance of surfactant-encapsulated and conjugated polymer-wrapped CNTs in aligned arrays prepared by dielectrophoresis (20) and shear-casting (21); however, the conductance has not exceeded $0.01 \text{ mS } \mu\text{m}^{-1}$ in these cases

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(although the L_{ch} of these types of devices has yet to be aggressively scaled). Advances in the performance of random-network thin-film FETs with L_{ch} on the order of micrometers have been realized (22–25); however, inter-CNT interactions and contact-resistance challenges have limited both the on-state conductance and the $I_{\text{on}}/I_{\text{off}}$ of random-network FETs when L_{ch} is reduced to hundreds of nanometers (26, 27). In each scenario, the result has been that, whereas CNTs are ultimately expected to yield FETs that are more conductive than conventional semiconductor materials, such as Si, by sixfold or more. Likewise, in RF applications, depressed on-state conductance and imperfect saturation characteristics arising from metallic CNTs and inter-CNT interactions have limited the maximum frequency of oscillation and linearity (9, 27–29).

Here, we report on quasi-ballistic CNT array FETs at a density of 50 CNTs μm^{-1} prepared through the deposition of highly purified polyfluorene-sorted semiconducting CNTs from solution into aligned arrays on substrates via the scalable process of floating evaporative self-assembly (FESA) (30–32). The arrays achieve exceptional performance because of three reasons. The (i) outstanding alignment and spacing of the CNTs in the arrays afforded by FESA and the (ii) postdeposition treatment of the arrays to remove solvent residues and the insulating side chains of the polyfluorene wrappers enable the realization of highly conductive electrical contacts to each CNT in the arrays and a highly conductive channel. As a result, the device conductance reaches 1.7 mS μm^{-1} at an L_{ch} of 100 nm and as high as 0.46 G_0 or 35 μS per CNT. At the same time, the (iii) exceptional electronic-type purity of the semiconducting CNTs afforded by the use of polyfluorenes as CNT-differentiating agents leads to a high $I_{\text{on}}/I_{\text{off}}$. The saturated on-state current density reaches 900 $\mu\text{A} \mu\text{m}^{-1}$ and exceeds that of Si FETs when compared at an equivalent gate oxide thickness and at the same off-state current density.

RESULTS

FET architecture

The FETs are fabricated by isolating semiconducting CNTs first using a large excess of the conjugated polymer poly[[9,9-dioctylfluorenyl-2,7-diyl]-*alt-co*-(6,60-(2,20-bipyridine))] (PFO-BPy) in toluene to selectively wrap the semiconducting species (33). Recent work has shown that polyfluorenes (34), polythiophenes (35), and related copolymers (36) can selectively isolate semiconducting CNTs to high purities, and advances in the detection of metallic CNTs via electronic (21, 31) and spectroscopic (37) measurement indicate that the electronic-type purity of these polymer-sorted CNTs is >99.98% semiconducting. The CNTs are deposited onto Si wafers with 15 nm of thermally grown SiO_2 via FESA, which yields dense arrays of CNTs that remain predominantly isolated. FETs are fabricated from the CNTs after three different stages of postdeposition treatment: (i) immediately after FESA deposition (“as-deposited”), (ii) after extensive solvent rinsing (“rinsed”), and (iii) after extensive solvent rinsing followed by an additional thermal annealing step in high vacuum (“rinsed + annealed”). Previous work has shown that postdeposition rinsing (38–40) and annealing, for example, in vacuum (17, 18) or oxidizing environments (41), can be used to desorb and/or decompose spurious adsorbates and surfactants from the surfaces of CNTs. Here, these postdeposition treatments are implemented to specifically remove residues arising from solution processing in chloroform and

to partially decompose the polymer wrappers, with the goals of improving the CNT conductance and electrical contacts, as detailed below.

The schematic in Fig. 1A and the scanning electron microscopy (SEM) image in Fig. 1B depict the device architecture. The SiO_2 and Si substrate are used as the FET back-gate dielectric and gate electrode, respectively. The source and drain electrodes consist of thermally deposited and patterned 30-nm-thick layers of Pd. The length over which each metal contact overlaps the CNT array (L_c) is $6.8 \pm 0.4 \mu\text{m}$, the channel width (W_{ch}) is 4 μm , and L_{ch} varies from 95 to 340 nm. The high-resolution SEM image of a representative channel in Fig. 1B demonstrates that the semiconducting CNTs are well aligned and predominantly isolated at a density of $47 \pm 3 \text{ CNTs} \mu\text{m}^{-1}$. The electrode regions are characterized via cross-sectional transmission electron (Fig. 1C) and atomic force micrographs (Fig. 1D), which show that the Pd conforms to the CNT arrays and the underlying SiO_2 substrate.

Current-voltage characteristics

The $I_{\text{DS}}-V_{\text{GS}}$ and $I_{\text{DS}}-V_{\text{DS}}$ characteristics presented in Fig. 2 (A and B, respectively) demonstrate the behavior of a typical “rinsed + annealed” array FET at an L_{ch} of 100 nm (full sweep $I_{\text{DS}}-V_{\text{GS}}$ characteristics presented in fig. S1). I_{DS} increases nearly linearly with V_{GS} for V_{GS} less than a threshold voltage (V_{T}) of roughly -4 V (Fig. 2A) and ohmically with V_{DS} from 0 to -0.3 V . I_{DS} then increases sublinearly for $V_{\text{DS}} > -0.3 \text{ V}$, with current saturation at $V_{\text{DS}} = -1 \text{ V}$ (Fig. 2B). Saturation has been reported previously in single CNT FETs at similar biases and L_{ch} and has been attributed to optical phonon scattering that occurs at high fields (5).

To compare the effect of the different postdeposition CNT treatments, the on-state conductance (G_{on}) is extracted from the transfer characteristics at $V_{\text{DS}} = -0.1 \text{ V}$ and $V_{\text{GS}} = -10 \text{ V}$, and the transconductance ($g_{\text{m}} = dI_{\text{DS}}/dV_{\text{GS}}$) is extracted by performing a linear fit to $I_{\text{DS}}-V_{\text{GS}}$ curves measured at $V_{\text{DS}} = -1 \text{ V}$ in the linear region where $V_{\text{GS}} < V_{\text{T}}$. G_{on} , in some cases, is so high that the lead resistance (R_{leads}) is nonnegligible, approaching 23% of the on-state device resistance, and is measured and then subtracted to determine the intrinsic FET characteristics (as detailed in fig. S2). Both G_{on} and g_{m} generally increase with decreasing L_{ch} for all three postdeposition treatments. When analyzed at similar L_{ch} , the postdeposition treatments increase G_{on} sevenfold (Fig. 2C) and g_{m} threefold (Fig. 2D) in total. G_{on} reaches as high as 1.7 mS μm^{-1} following the “rinsed + annealed” treatment at $L_{\text{ch}} = 100 \text{ nm}$ while maintaining an $I_{\text{on}}/I_{\text{off}}$ of 10^5 at $V_{\text{DS}} = -0.1 \text{ V}$. A g_{m} of 170 $\mu\text{S} \mu\text{m}^{-1}$ and a saturation current (I_{sat}) of 900 $\mu\text{A} \mu\text{m}^{-1}$ are achieved in the same device at $V_{\text{DS}} = -1 \text{ V}$, although at a lower $I_{\text{on}}/I_{\text{off}}$ of $10^{2.7}$. When all 88 “rinsed + annealed” FETs plotted in Fig. 2 (C and D) with an L_{ch} of $190 \pm 60 \text{ nm}$ are considered, we obtain a G_{on} of $0.8 \pm 0.3 \text{ mS} \mu\text{m}^{-1}$ at an $I_{\text{on}}/I_{\text{off}}$ of $10^{5.5 \pm 1.3}$ for a V_{DS} of -0.1 V . Likewise, we obtain a g_{m} of $99 \pm 25 \mu\text{S} \mu\text{m}^{-1}$ and an I_{sat} of $490 \pm 140 \mu\text{A} \mu\text{m}^{-1}$ at an $I_{\text{on}}/I_{\text{off}}$ of $10^{3.9 \pm 1.0}$ for a V_{DS} of -1 V . The lower $I_{\text{on}}/I_{\text{off}}$ at higher V_{DS} is attributed to increased electron injection and ambipolar behavior, possibly originating from inter-CNT crosstalk effects that may affect injection at the CNT-drain interface for $V_{\text{GS}} > V_{\text{T}}$ (15, 42). Nonetheless, for 60% of “rinsed + annealed” CNT array FETs measured at $V_{\text{DS}} = -1 \text{ V}$, the I_{off} is still lower than 0.1 $\mu\text{A} \mu\text{m}^{-1}$, approaching the off-state needed for high-performance logic applications (8, 43). The $I_{\text{on}}/I_{\text{off}}$ at low V_{DS} is more indicative of the metal-semiconducting CNT purity. For the “rinsed + annealed” devices, the $I_{\text{on}}/I_{\text{off}}$ at low V_{DS} exceeds 10^3 in 87 of 88 devices measured, indicating that the purity of the semiconducting CNTs is at least 99.99%.

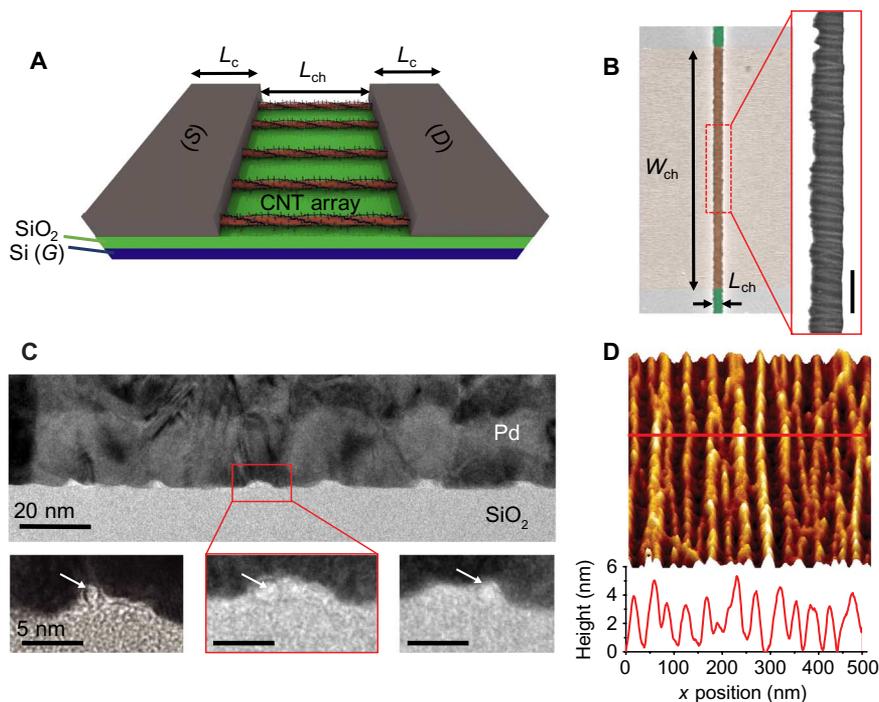


Fig. 1. FETs constructed from densely packed semiconducting CNT arrays. (A) Schematic of CNT array sitting on a SiO₂/Si back gate (G) with top Pd source (S) and drain (D) electrodes. (B) False-colored SEM image of a representative FET highlighting where the contacts overlap the CNT array (light orange) and the CNT array channel (dark orange), with $W_{\text{ch}} = 4.1 \mu\text{m}$ and $L_{\text{ch}} = 150 \text{ nm}$. Inset SEM image (scale bar, 200 nm) shows the CNT array, with 47 CNTs μm^{-1} and a high degree of alignment. (C) TEM cross-sectional image of Pd/CNT/SiO₂ electrode stack where the “humps” in the Pd correspond to CNTs in the array. High-resolution TEM images reveal individual CNTs underneath the Pd “humps” with a diameter of 1.3 to 1.9 nm. (D) Atomic force microscopy image of 30 nm of Pd overcoating a CNT array, evidencing the conformity of the Pd to the individual CNTs.

The majority of the devices (70%) exhibit excellent $I_{\text{on}}/I_{\text{off}}$ greater than 10^5 .

Critically, these high $I_{\text{on}}/I_{\text{off}}$ ratios are obtained without the need for metallic CNT burnout techniques, such as Joule self-heating (12, 44), which can degrade the conductance of remaining semiconducting CNTs and become increasingly difficult to implement with increasing CNT packing density. It is also important to note that the high $I_{\text{on}}/I_{\text{off}}$ ratios obtained here are not the result of the preferential etching or removal of metallic CNTs during the rinsing or annealing treatments. For example, the off-state conductance is similar in devices fabricated without and with 400°C annealing treatment, reaching $10^{-8.2 \pm 1.8}$ and $10^{-8.7 \pm 1.2} \text{ S } \mu\text{m}^{-1}$, respectively. Additional discussion of the semiconducting purity and of the factors that may affect the $I_{\text{on}}/I_{\text{off}}$ is further elaborated in the Supplementary Materials and in figs. S3 to S5.

The G_{on} versus L_{ch} dependencies for each of the postdeposition treatments in Fig. 2C are fit to extract the mean free path (L_{MFP}) according to

$$G_{\text{on}}^{-1} = R_{\text{on}} = \frac{h}{4e^2} \frac{L_{\text{ch}}}{L_{\text{MFP}}} + 2R_{\text{c}} \quad (1)$$

where $h/4e^2$ is the quantum resistance for two modes (45) and $2R_{\text{c}}$ is the total CNT-Pd contact resistance at both source and drain electrodes. The fit L_{MFP} are 3, 21, and 42 nm for the “as-deposited,” “rinsed,” and “rinsed + annealed” CNTs, respectively. From these results, we

postulate that charge transport in the “as-deposited” CNT arrays is significantly limited by impurity scattering and that postdeposition treatments reduce impurities (that is, increase L_{MFP}). Moreover, whereas the CNT-Pd contacts are nonohmic in the “as-deposited” FETs, possibly indicating the presence of a Schottky barrier (46, 47), the contacts become ohmic in “rinsed + annealed” devices (fig. S6).

Characterization of postdeposition treatments

In general, optimizing the performance of FETs fabricated from solution-deposited CNTs is challenging because (i) solution-processed CNTs are coated with relatively insulating surfactant/polymer wrappers that can interfere with contacts (48) and (ii) the exposure of the CNTs to solvent and the ultrasonic processing used to disperse the CNTs can physically and chemically modify their surfaces and properties, potentially decreasing L_{MFP} and conductance (49, 50). X-ray photoelectron spectroscopy (XPS), optical absorption, and Fourier transform infrared (FTIR) spectroscopy are used to characterize the modification of our CNTs in their “as-deposited” state and to show that this modification is largely reversible through postdeposition treatment.

In the “as-deposited” CNT arrays, the atomic ratio of C/N measured by XPS is 39:1 (Fig. 3A), which is similar to the ratio of 41:1 measured from the optical absorbance spectra of the polymer-wrapped CNTs in solution (fig. S7) using known optical cross sections to determine relative concentrations. These data indicate that the PFO-BPy polymer wrapper and the CNTs are nearly equally abundant in the “as-deposited” arrays by mass, corresponding to up to six polymer

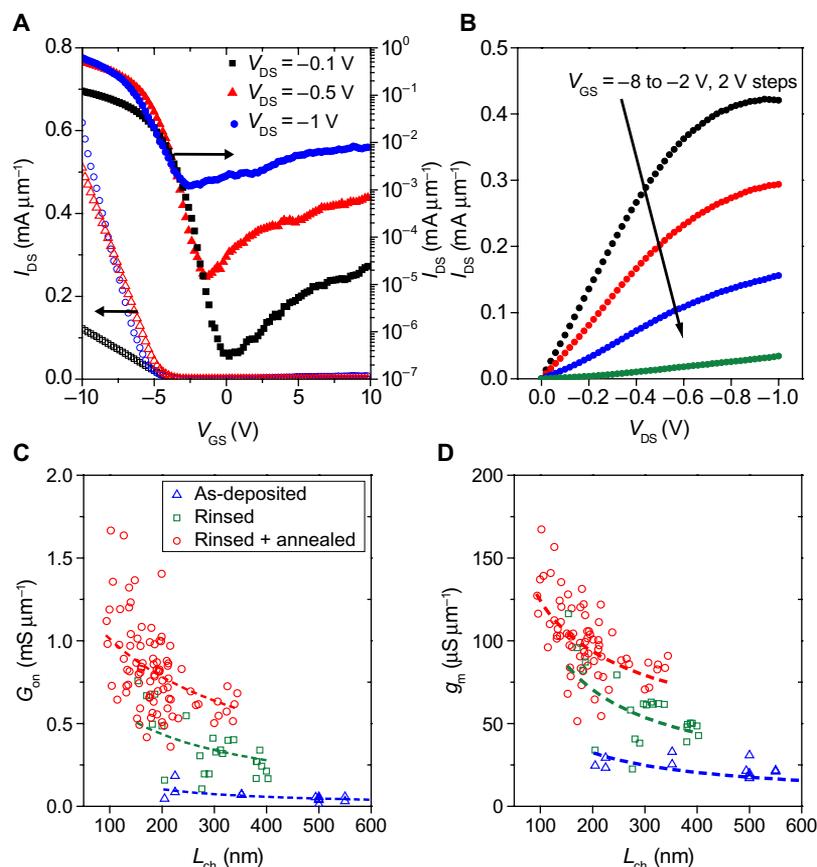


Fig. 2. Electrical properties of CNT array FETs and influence of postdeposition treatment on conductance. (A) I_{DS} - V_{GS} curves forward sweep for a representative "rinsed + annealed" FET with $L_{ch} = 100$ nm where the open and filled symbols are plotted on linear and logarithmic scales, respectively. (B) I_{DS} - V_{DS} output curves for the same device as in (A). (C) G_{on} versus L_{ch} obtained from CNT arrays that have undergone the three different postdeposition treatment conditions, fit to Eq. 1, with a sevenfold total increase in G_{on} resulting from the "rinsed + annealed" treatment. (D) g_m versus L_{ch} for each surface treatment fit to $g_m \propto L_{ch}^{-1}$ as a guide to the eye, with a threefold total increase in g_m resulting from the "rinsed + annealed" treatment.

chains wrapping around a given CNT cross section. Cl residues are also detected at a concentration of $(1.7 \pm 0.5) \times 10^{13} \text{ cm}^{-2}$ or a C/Cl ratio of 160:1. Moreover, the CNT excitonic S_{11} absorption peak is heavily bleached, indicating the chemical modification and/or doping of the CNTs (51). Previous work has shown that processing in chlorinated solvents can partially chlorinate CNTs (49, 52), potentially explaining the excess Cl residues, the doping, and, therefore, the poor L_{MFP} . The protocols used to quantify atomic concentrations from XPS and optical absorbance spectra and a summary of these concentrations are given in figs. S7 and S8 and table S1.

Postdeposition rinsing and vacuum annealing treatments are investigated as means for minimizing/decomposing the insulating polymer wrapper and for removing the Cl residues. The S_{11} peak is largely restored, and $54 \pm 5\%$ of the Cl is removed in "rinsed" arrays. However, only minor amounts of C and N of $8.5 \pm 2.5\%$ and $8.9 \pm 3.2\%$, respectively, are removed, indicating that most of the CNTs and the polymer wrapper remain on the substrate surface during this rinsing. Annealing in vacuum is next explored. High-vacuum (as opposed to oxidizing) conditions are used to preserve the pristine nature of the CNTs. The FTIR spectra in Fig. 3C and fig. S9 indicate loss of the

polymer's alkyl side chains (53) between 300° and 400°C (as assessed from C-H stretch modes at 2855 and 2926 cm^{-1}) in "rinsed + annealed" arrays. Annealing at 400°C also eliminates all signatures of Cl and maximizes the S_{11} . Thus, vacuum annealing at 400°C is chosen as the annealing condition here. XPS and FTIR show that the backbone of the PFO-BPy wrapper is still partly intact under this condition (Fig. 3A and fig. S9). Nonetheless, the "rinsed + annealed" treatment has a combined effect of removing adsorbed Cl, reversing the chemical modification of the CNTs, and removing the insulating side chains of the polymer. These effects increase the L_{MFP} from 3 to 42 nm while also leading to ohmic CNT-Pd contacts, giving rise to the seven- and threefold improvements in G_{on} and g_m , respectively.

Further increasing the annealing temperature to 500°C does not yield additional improvements in G_{on} . For example, G_{on} is statistically invariant, changing from 0.8 ± 0.3 to 0.7 ± 0.3 when the annealing temperature is increased from 400° to 500°C , respectively, for devices with L_{ch} in the range of 100 to 300 nm. G_{on} is invariant despite the observation that the carbon-carbon double bond stretch arising from the polymer backbone at 1450 cm^{-1} begins to decay between 400° and 500°C (fig. S9). The lack of improvement in G_{on}

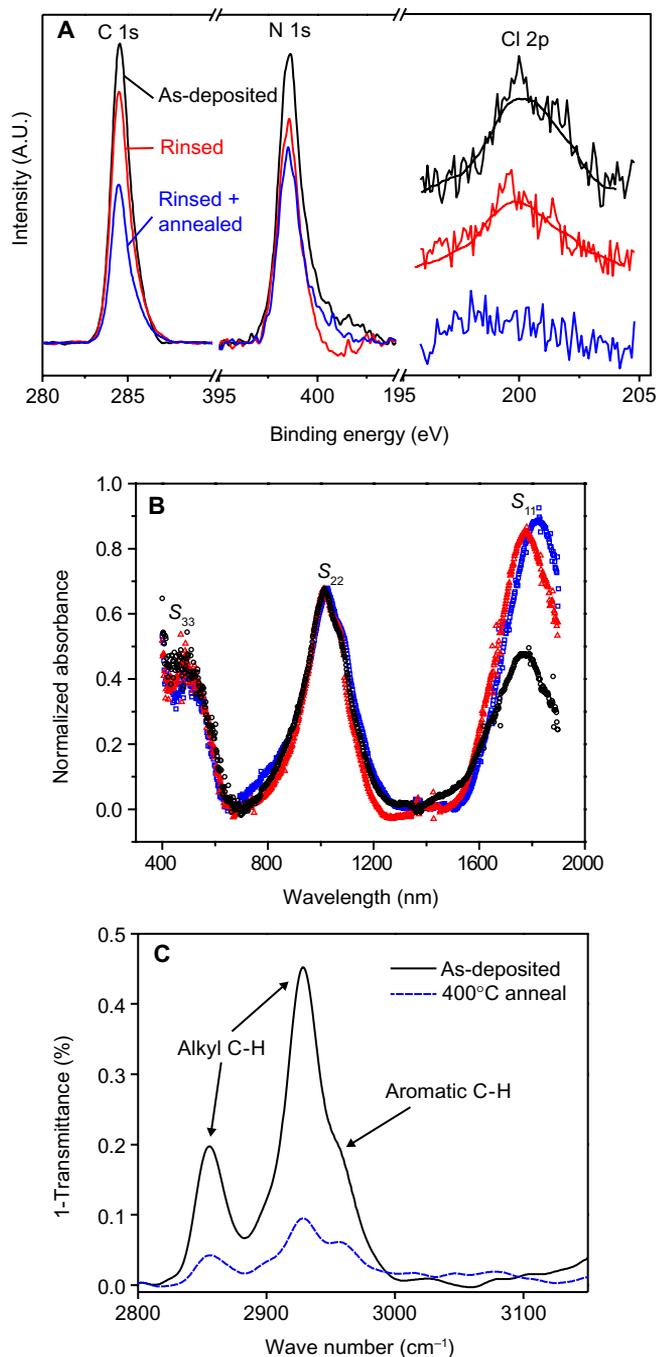


Fig. 3. Spectroscopic characterization of postdeposition treatments. (A) XPS of CNT arrays showing C 1s, N 1s, and Cl 2p peaks following solvent rinsing and vacuum annealing. A.U., arbitrary units. (B) Optical absorbance spectra of CNT array films deposited on quartz with the approximate spectral windows corresponding to the first three CNT S_{ii} transitions marked for clarity. Black open circles correspond to “as-deposited,” red open triangles correspond to “rinsed,” and blue open squares correspond to “rinsed + annealed” treatments. (C) FTIR spectroscopy of 10-nm-thick PFO-BPy films. Vacuum annealing reduces the alkyl C–H stretching modes centered at 2855 and 2926 cm^{-1} , corresponding to loss of the polymer side chains.

using a 500°C anneal suggests that the removal of the spurious Cl and polymer side chains between 300° and 400°C is the main factor responsible for the conductance increase observed during annealing. Additional studies show that annealing at 400°C without rinsing first also effectively removes the Cl and side chains and that “annealed-only” devices demonstrate a similar G_{on} to “rinsed + annealed” FETs (fig. S10). Regardless, the rinsing treatment provides a valuable route to improve device performance for applications that require low-temperature processing (for example, plastic electronics).

DISCUSSION

FET benchmarking compared to CNT FETs

The performance of the CNT arrays measured in this work are compared (i) to state-of-the-art single CNT FETs on a per-tube basis in Fig. 4 and (ii) to commercially fabricated Si metal oxide semiconductor FETs (MOSFETs) in Fig. 5. The highest reported conductance in a CVD-grown single CNT FET is $1.4 G_0$ with a $2R_c$ of 10 kilohm-tube and an L_{MFP} of 200 nm at an L_{ch} of 15 nm (54). For comparison, the highest reported conductance in a solution-processed single CNT FET is $0.58 G_0$ with a $2R_c$ of 20 kilohm-tube and an L_{MFP} of 28 nm at an L_{ch} of 15 nm (55). The conductance per tube of three champion CNT array FETs from this study are presented in Fig. 4 as a function of V_{GS} at a $V_{\text{DS}} = -0.1$ V. The conductance per tube reaches $0.46 G_0$ at a much longer L_{ch} of 130 nm. The average conductance per tube is $0.31 \pm 0.08 G_0$ for $L_{\text{ch}} < 150$ nm (measurement and comparison to previous state-of-the-art CNT arrays are further detailed in fig. S11 and table S2). Analysis of more than 88 devices at different L_{ch} via the transmission line and Y-function methods in fig. S12 indicates that the characteristic $2R_c$ of these devices falls within the range of 28 to 40 kilohm-tube, whereas the L_{MFP} varies from 33 to 56 nm, corresponding to drift-diffusion mobility in the range of 1130 to 1912 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. Scaling of the L_{ch} below the L_{MFP} (<30 nm) should lead to further increases in the channel conductance, thereby approaching the performance of state-of-the-art CVD-grown single CNT FETs, but in a many-CNT array that is more useful for commercial technologies.

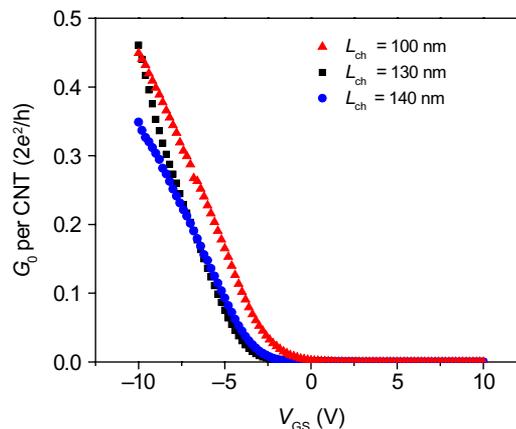


Fig. 4. CNT array FETs with conductance per tube approaching the fundamental quantum conductance limit $2G_0 = 4e^2/h$. Three champion devices with conductance reaching $0.46 G_0$. All three devices also exhibit high $I_{\text{on}}/I_{\text{off}} > 10^4$.

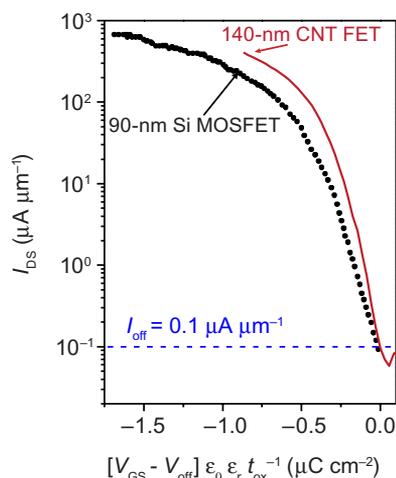


Fig. 5. Benchmarking CNT array FET performance against Si MOSFETs.

I_{sat} of a champion CNT array FET ($V_{\text{DS}} = -1$ V; $L_{\text{ch}} = 140$ nm) and 90-nm node Si MOSFET (43) ($V_{\text{DS}} = -1.2$ V) versus $V_{\text{GS}} - V_{\text{off}}$, normalized by the dielectric constant of the gate dielectric ($\epsilon_r \epsilon_0$) and the gate oxide thickness (t_{ox}), where $V_{\text{GS}} - V_{\text{off}}$ is 0 V at an I_{off} of $0.1 \mu\text{A} \mu\text{m}^{-1}$. Oxide parameters for the CNT array FET are $t_{\text{ox}} = 15$ nm and $\epsilon_r = (\epsilon_{\text{air}} + \epsilon_{\text{SiO}_2})/2 = 2.45$ for the $\text{SiO}_2/\text{CNT}/\text{air}$ dielectric stack (31, 62). Oxide parameters for the Si MOSFET are $t_{\text{ox}} = t_{\text{eff}} = 2.4$ nm [effective oxide thickness accounting for inversion capacitance (63)] and $\epsilon_r = \epsilon_{\text{SiO}_2} = 3.9$. The champion CNT array FET exhibits an I_{sat} that is 1.9-fold higher when measured at an equivalent charge density ($V_{\text{GS}} - V_{\text{off}}$) $\epsilon_r \epsilon_0 t_{\text{ox}}^{-1}$ of $-0.85 \mu\text{C} \text{cm}^{-2}$.

FET benchmarking compared to Si FETs

Comparison of CNT FETs to Si MOSFETs has become a useful benchmarking tool for evaluating the fundamental limits of scaling the channel length (l), contact length (7, 48), and CNT density of CNT FETs (19). For digital logic applications, a high drive current and a high transconductance are required to maximize speed (that is, logic transitions per second), whereas the subthreshold slope must be high to minimize leakage current when the device is switched off (56). We benchmark the saturated on-state current and the subthreshold behaviors of CNT array FETs against a 90-nm node Si P-channel MOSFET (43) at an equivalent oxide thickness and an off-state current density of $0.1 \mu\text{A} \mu\text{m}^{-1}$ in Fig. 5. The CNT array FET exhibits a more rapid rise in I_{DS} than the Si MOSFET, indicative of the excellent electrostatic properties of the thin-body CNTs. The CNT array FET also shows significant improvements in the on-state where, at an equivalent charge density ($V_{\text{GS}} - V_{\text{off}}$) $\epsilon_r \epsilon_0 t_{\text{ox}}^{-1}$ of $-0.85 \mu\text{C} \text{cm}^{-2}$, CNT array FETs reach an I_{sat} of $392 \mu\text{A} \mu\text{m}^{-1}$, which is 1.9 times higher than the MOSFET I_{sat} of $204 \mu\text{A} \mu\text{m}^{-1}$. We also note that the champion 100-nm L_{ch} CNT array FET with a current density of $900 \mu\text{A} \mu\text{m}^{-1}$ exceeds the $630 \mu\text{A} \mu\text{m}^{-1}$ that has been demonstrated for the GaAs pseudomorphic high-electron mobility transistor (pHEMT) technology (57, 58).

CONCLUSIONS

Ballistic transport with an on-state conductance approaching $2G_0$ has been previously realized in single CNT FETs but has been difficult to achieve in FETs constructed from densely packed arrays of CNTs, such as those needed for most technologies. CNT array FETs are demon-

strated here with an on-state conductance of $1.7 \text{ mS} \mu\text{m}^{-1}$ and a conductance per CNT as high as $0.46 G_0$, which is seven times higher than previous state-of-the-art CNT array FETs made by other methods. These FETs are nearing the performance of state-of-the-art single CNT FETs but in the format of an array in which quasi-ballistic transport is simultaneously driven through many, tightly packed CNTs in parallel, substantially improving the absolute current drive of the FETs and, therefore, their utility in technologies.

The exceptional performance of the arrays achieved here is attributed to the combined outstanding alignment and spacing of the CNTs, the postdeposition treatment of the arrays to remove solvent residues and the insulating side chains of the polymers that wrap the CNTs, and the exceptional electronic-type purity of the semiconducting CNTs afforded by the use of polyfluorenes as CNT-differentiating agents. The performance of previous CNT array FETs has not been as high, likely because these FETs have not simultaneously met all of these attributes. For example, the alignment and postdeposition treatment of CNTs alone are insufficient but must be coupled with the proper CNT array packing density and morphology to avoid inter-CNT interactions that can lower G_{on} and on-off switching, high semiconducting purity to avoid leakage currents from metallic CNTs, and the use of CNTs that have not undergone significant chemical modification to achieve a long L_{MFP} and high channel conductance. As a result of the excellent alignment and spacing, postdeposition treatment, and high electronic-type purity achieved here, on-state and subthreshold behaviors that are comparable to or that exceed those of state-of-the-art Si MOSFETs are realized, when compared at an equivalent gate oxide thickness and at the same off-state current density.

A number of challenges remain, including reducing hysteresis (22), improving device-to-device reproducibility (59), reducing leakage current (60), and scaling contact length for both N- and P-channel FETs (7). However, recent successes in overcoming these challenges in single CNT (7, 60, 61) and random-network CNT (22, 59) devices should translate well to the array CNT FETs presented here, providing an increasingly realistic pathway toward the development of CNT electronics and the application of these exceptional one-dimensional semiconductors in next-generation logic, high-speed communications, and semiconductor electronics technologies.

MATERIALS AND METHODS

Preparation of PFO-BPy-wrapped semiconducting CNT solutions

Semiconducting CNTs were extracted from arc-discharge CNT soot (750514, Sigma-Aldrich). A 1:1 weight ratio of PFO-BPy (2 mg ml^{-1} ; ADS153UV, American Dye Source) and CNTs was mixed in 60 ml of toluene. Raw CNT solution was ultrasonicated using a Fisher sonic dismembrator model 500 (400 W) at 40% amplitude for 5 min. Next, the solution was divided into six tubes that were centrifuged with a swing bucket rotor (Sorvall WX, TH-641, Thermo Scientific) at $300,000g$ for 10 min to remove soot and undispersed CNTs. The upper 90% of the supernatant was collected and centrifuged again at $300,000g$ for 1 hour. This process was repeated for up to six batches, and then the supernatants were collected, combined, and distilled down to a volume of 60 ml. The concentrated solution was next centrifuged to form a pellet that was then collected and redispersed in toluene, and the PFO-BPy-rich supernatant was discarded. This pelleting and

redispersion process was repeated until a 1:1 mass ratio of PFO-BPy to CNT was achieved. After the initial sorting and polymer washing steps, the PFO-BPy-wrapped CNT pellets were dispersed in chloroform (stabilized with ethanol, used as is from Fisher Scientific, #C606SK-1) at a concentration of $10 \mu\text{g ml}^{-1}$. The concentration of the CNTs was determined using known optical cross sections at the S_{22} transition (33), as explained in the Supplementary Materials. The concentration of PFO-BPy was optically determined from a series of reference samples of known concentration.

Deposition of CNT arrays

The CNT ink suspended in chloroform was delivered to substrates via FESA (30) in discrete ~ 0.6 - to 1.2 - μl doses onto the surface of a water subphase every 0.2 to 0.4 s using a syringe pump. Simultaneously, a receiving substrate that was partially submerged in the aqueous subphase was pulled out at a constant lift rate of 5 mm min^{-1} . The ink droplets spread on the water, wet the surface of the receiving substrate, and then evaporated. Each dose of ink resulted in the deposition of a band of aligned CNTs that was approximately $100 \mu\text{m}$ tall and spanned the entire width of the substrate, which was typically $\sim 25 \text{ mm}$ wide.

Fabrication of CNT FETs

The CNT channels of neighboring FETs were isolated from one another by patterning the deposited films of aligned CNTs before postdeposition treatments. The channels were protected by $4 \mu\text{m} \times 10 \mu\text{m}$ regions of polymethylmethacrylate (PMMA) that were patterned using electron-beam lithography. An oxygen reactive ion etch was used to etch the unwanted regions of CNTs, and then the remaining PMMA was lifted off with acetone. After the postdeposition treatments, a second electron-beam lithography step was performed to define source-drain electrodes with various channel lengths. Contacts were formed via thermal deposition of Pd (30 nm) and lift-off in acetone. The devices were measured under ambient conditions directly after electrode patterning with no further treatments. There is hysteresis in the I - V characteristics (fig. S1), which is expected for unencapsulated CNT FETs exposed to ambient conditions. Negative to positive sweeps (V_G) are shown in Figs. 2, 4, and 5.

Postdeposition treatment of the CNT arrays

The “rinsed” samples were treated by submerging the patterned CNT arrays in a vial of toluene at 60°C for 1 hour. Upon completion, the sample was transferred immediately into a room-temperature isopropyl bath for 30 s, followed by drying in an air stream. The “rinsed + annealed” samples underwent the “rinsed” treatment followed by annealing in vacuum at a base pressure of 5×10^{-6} torr and temperature of 400°C for 1 hour.

X-ray photoelectron spectroscopy

CNT arrays were prepared via FESA, as described above. Each substrate was broken into four equivalent parts, which underwent “as-deposited,” “rinsed,” “annealed,” and “rinsed + annealed” treatments. The XPS spectra were measured using a Thermo K-Alpha XPS with an x-ray spot size of $400 \mu\text{m}$ and monochromatic Al $K\alpha$ radiation (1486.7 eV). Survey and individual spectra were acquired using analyzer pass energies of 188 and 50 eV, respectively.

Fourier transform infrared spectroscopy

PFO-BPy thin films were prepared for FTIR analysis by spin-casting a solution of PFO-BPy (3 mg ml^{-1}) in chlorobenzene at a rate of

2000 rpm onto double-side polished Si/SiO₂ substrates. FTIR spectra were measured in transmission mode using a Bruker Vertex 70 with a Hyperion 2000 microscope having an approximately $250 \mu\text{m} \times 250 \mu\text{m}$ spot size.

Cross-sectional TEM imaging

CNT arrays were prepared via FESA on SiO₂ (90 nm)/Si substrates. The cross section was prepared using the in situ focused ion beam (FIB) lift-out technique on an FEI Dual Beam FIB/SEM. The sample was capped with Ir and ePt/I Pt before prep and imaged with a FEI Tecnai TF-20 field emission gun/TEM operated at 200 kV in bright-field and high-resolution TEM mode (Evans Analytical Group).

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at <http://advances.sciencemag.org/cgi/content/full/2/9/e1601240/DC1>

Supplementary Text

fig. S1. Full sweep transfer characteristics.

fig. S2. Lead resistance subtraction.

fig. S3. Optical spectroscopy evidence of high semiconducting purity.

fig. S4. Effect of annealing on I_{on}/I_{off} .

fig. S5. I_{off} variability.

fig. S6. Postdeposition treatment effect on output characteristics.

fig. S7. Optical absorbance spectra used to verify XPS atomic concentrations and CNT diameter distribution.

fig. S8. Atomic force microscopy height measurement used to quantify packing density for XPS calibration.

fig. S9. Temperature-dependent FTIR measurement of PFO-BPy side chains and backbone.

fig. S10. On-conductance comparison of “annealed” versus “rinsed + annealed” treatments.

fig. S11. Conductance per tube measured for FETs with $L_{ch} < 150 \text{ nm}$.

fig. S12. Contact resistance and mean free path extraction.

table S1. Surface treatment XPS summary.

table S2. CNT FET performance comparisons.

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