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## A 176-Channel 0.5cm<sup>3</sup> 0.7g Wireless Implant for Motor Function Recovery after Spinal Cord Injury

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Epidural spinal stimulation has shown effectiveness in recovering the motor function of spinal cord transected rats by modulating neural networks in lumbosacral spinal segments [1, 2]. The state-of-the-art neuromodulation implant [3] reports a 4-channel stimulator with wireless data and power links for small animal experiments, yet weighs 6g and has a volume of 3cm<sup>3</sup>. It is preferable that the implant package has a comparable size to its bioelectronics and a high-density stimulator to support stimulation with high spatial resolution.

Furthermore, the epidural electrode should be soft and flexible because a mechanical mismatch exists at the tissue-electrode interface [1]. Unlike other implant/SoCs that stimulate with pre-loaded patterns [4–5], the implant for motor function recovery should be capable of adaptively adjusting its stimulation patterns at run time in response to the subject's varying physiological states [2]. Measuring the electrode-tissue impedance is also critical to ensure safe stimulation. Deriving the equivalent circuit model of the electrode-tissue interface determines the safe stimulation boundary (i.e. pulse width and intensity) to ensure the electrode overpotential is within the water window [6]. However, an SoC implementation of this function has not been reported.

Figure 22.2.1 illustrates the implantable system performing simultaneous stimulation and full-duplex data telemetry using a rat model. The rat carries a rendezvous device that wirelessly powers the implant and links the implant and a remote device (e.g. smart phone). The implant is miniaturized to 0.5cm<sup>3</sup> and 0.7g. A thin (8μm), flexible polyimide based platinum electrode array is placed into the epidural space, and EMG (electromyography) wire electrodes (AS632 Cooner wire, Chatsworth CA) are sutured onto leg muscles.

The core of the implant is a mixed-signal, multi-voltage SoC performing high-voltage (HV) 160-channel current stimulation, 16-channel recording, and 48-channel bio-impedance characterization with fully integrated power/data telemetry (Fig. 22.2.2). Improved upon [7], a power converter generates 4 different voltages to power the implant, with added capability of adjusting the supply voltages for stimulators ( $\pm 6/8/10/12$  V) to accommodate various bioimpedances. A new quasi full-duplex data transceiver links the SoC and the rendezvous device at 2Mb/s. The NECSIS (Neural Command Signal Interface System) controller determines the implant operation based on the received commands (CMDs). Stimulation of 160 channels is achieved by 40 stimulation current drivers, each with a 1:4 Demux [7]. For impedance measurement, 12 out of 40 Demux inputs are selectively connected to the 16:1 MUX made of HV transistors, allowing 48 electrodes to be characterized. HV MUX is also connected to the power converter outputs and two of the MUX inputs are reserved for

inertial and temperature sensors. This SoC supports chip clustering using a 2-bit ID control. By sharing the same coils, a four-SoC cluster can provide 640-channel stimulation, 64-channel recording, as well as 192-channel impedance characterization.

Figure 22.2.3 shows the operation of the quasi full-duplex data link and its implementation. Realizing a high data rate reverse link with a power coil is disadvantageous because high wireless power transfer efficiency and high Qfactor requirements limit the data rate. A low-Q data coil is thus used for both the forward and reverse links. In the reverse telemetry, the SoC transmits the recorded data in packets separated by programmable time gaps. Each packet contains a header, digitized data, and an end marker. Once the rendezvous device recognizes the end marker, it can send a CMD to the SoC within this time gap (Fig. 22.2.3 bottom panel). The SoC consists of a DPSK receiver for its good immunity to interference [7] and a LSK transmitter for low-power consumption ( $< 4\mu\text{W}$ ). The test result shows both forward DPSK and reverse LSK signals can co-exist on the same coil without contention. The LSK signal may result in error bits at the DPSK-demodulated output, but they fail the CMD header check and are discarded.

Characterizing bio-impedance across a broad spectrum requires sophisticated equipment and is time-consuming, but doing so at a fixed frequency provides limited information. We propose and implement a hardware-efficient time-domain method to characterize the Randles cell electrode model. First, a biphasic, low-intensity current stimulus with inter-pulse delay is applied to an electrode. Then, by measuring the electrode overpotentials  $V_0$ ,  $V_1$ , and  $V_2$ , tissue resistance ( $R_S$ ), double layer capacitance ( $C_{dl}$ ), and charge transfer resistance ( $R_{CT}$ ) are accordingly derived. Low-intensity stimulus ensures  $R_{CT}$  does not complicate the  $C_{dl}$  computation. Inter-pulse delay provides a passive discharge period for  $R_{CT}$  acquisition (Fig. 22.2.4 top). In the circuit implementation, both recording and impedance characterization circuits share the same ADC, whose input voltage is confined by voltage-clamp diodes. A Stim\_flag bit is inserted into the serialized ADC output to denote the stimulation onset. The impedance characterization module then searches for  $V_0$ ,  $V_1$ , and  $V_2$  based on the Stim\_flag bit and the given stimulation parameters (Fig. 22.2.4 bottom panel).

Figure 22.2.5 illustrates the prototype employing thin film polymer process with a special bump pad design. An  $8\mu\text{m}$  thick polyimide substrate with an epidural electrode array serves as an interposer to connect coils, passive components, wire electrodes, and the CMOS pads via gold bumps. The prototype integrates 172 epidural electrodes, 4 EMG wire electrodes, 2 coils, 6 0201-SMD capacitors, and the SoC into a 0.7g,  $0.5\text{cm}^3$  package. Cyclic voltammetry characterization shows the fabricated epidural electrode has a charge storage capacity of  $6.74\mu\text{C}$ . The electrode *in-vivo* test results demonstrate  $< 1.5\text{k}\Omega$  impedance standard deviations during the 52-day post-surgery period.

Figure 22.2.6 shows the SoC test results, its highlighted features, and the *in-vivo* EMG recording when stimulating the lumbosacral region of the spine in both normal and spinal cord transected rats. Stimulation-induced EMG middle responses and spontaneous onset of motor unit are observed in the leg muscles of the normal rat. Stimulating the paralyzed rat

results in consistent EMG patterns required for standing. A stronger stimulation current is applied on the paralyzed rat as its brain-spinal network is injured.

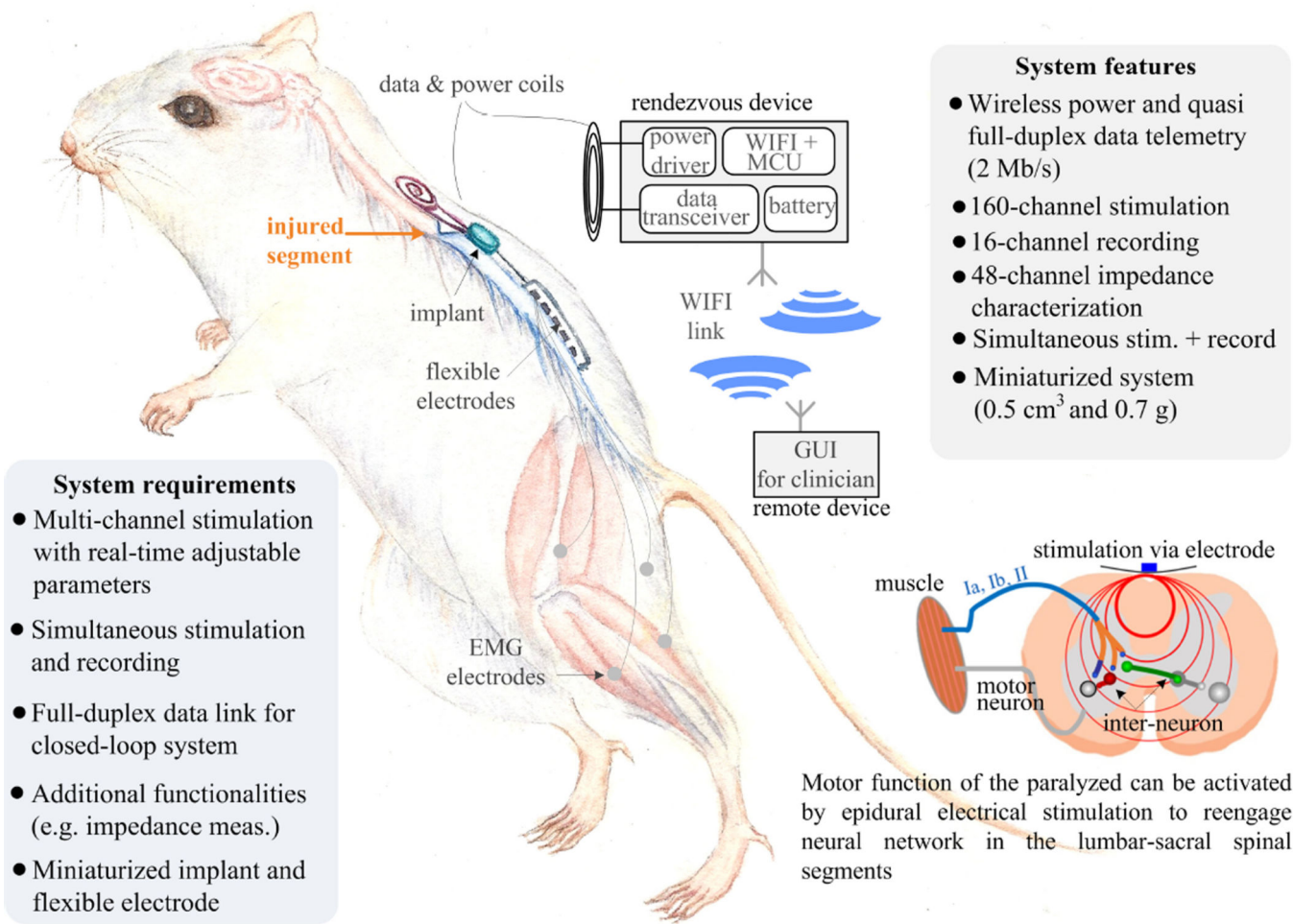
This SoC is implemented in HV 0.18 $\mu\text{m}$  CMOS with an area of 5.7.4.4mm<sup>2</sup>. The table of comparison with prior works is shown in Fig. 22.2.7. This SoC implant targets motor function recovery after spinal cord injury. Its versatile functionalities and highly compact form factor (0.5cm<sup>3</sup> and 0.7g) also make it applicable in future implants for various medical applications.

## Acknowledgments

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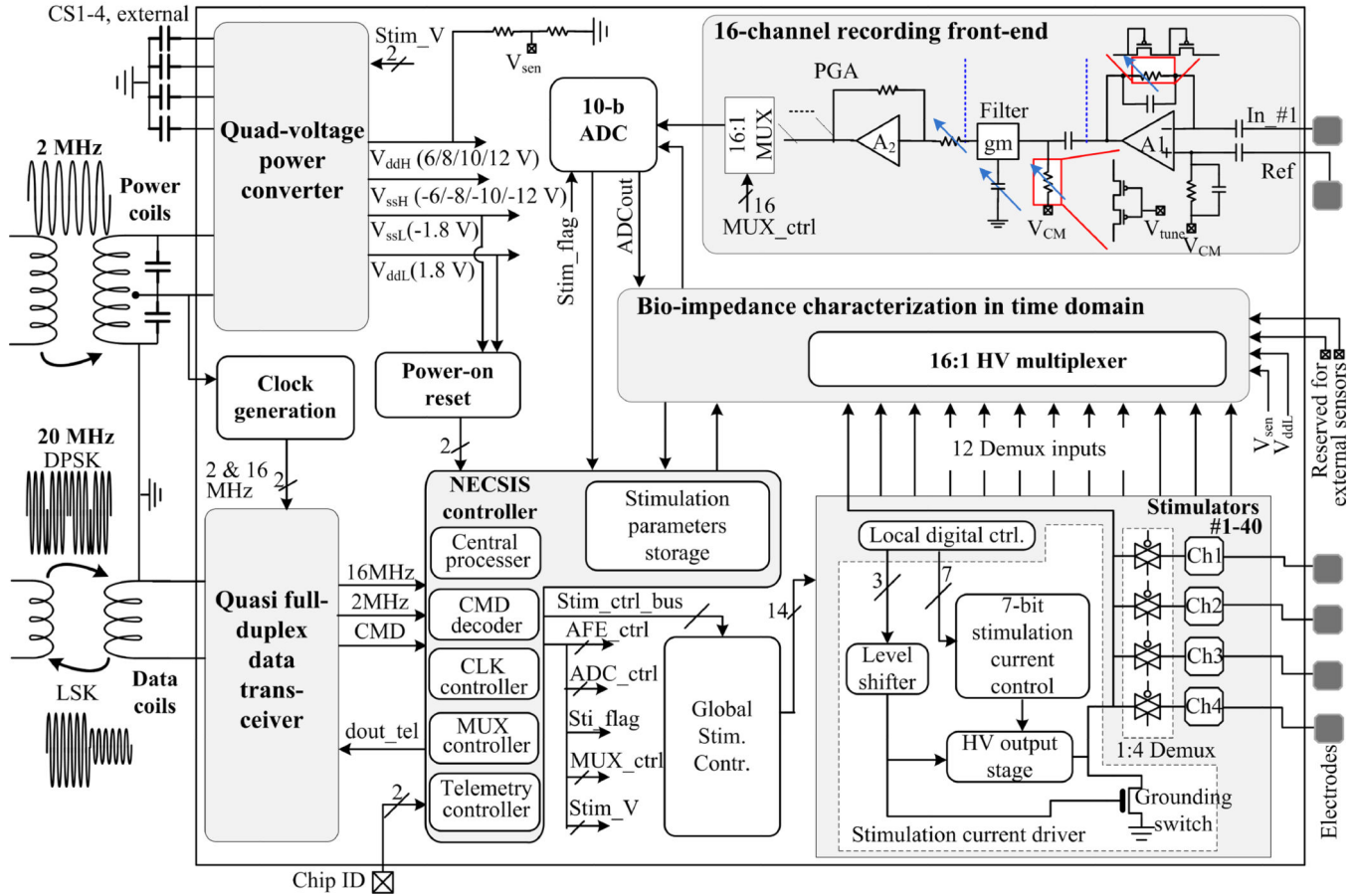
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**Figure 22.2.1.** Illustration of the implantable system and the biological mechanism for motor function recovery.

**System Diagram of the SoC**



**Figure 22.2.2.** System diagram of the SoC. Power converter, data transceiver, NECSIS controller, stimulators, and impedance characterization circuits are all integrated in the SoC. The SoC and the external device are linked inductively.

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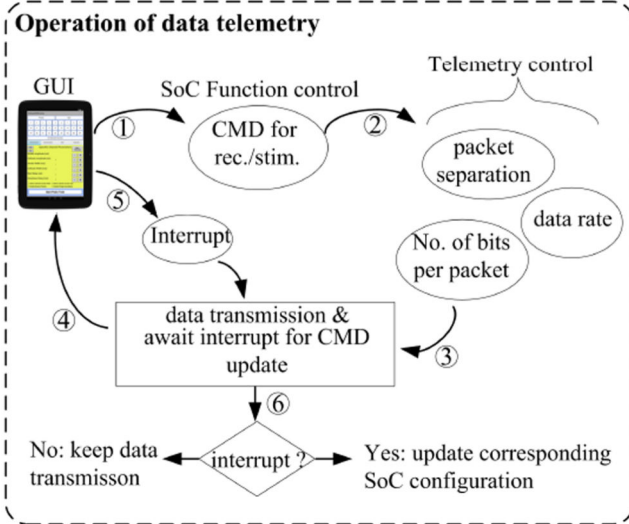
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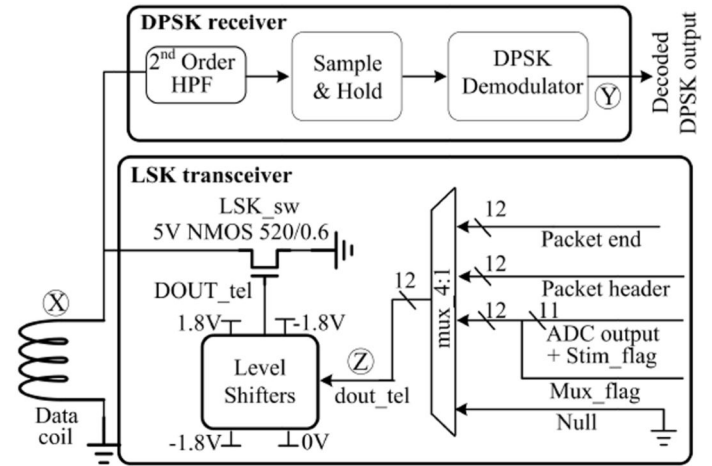
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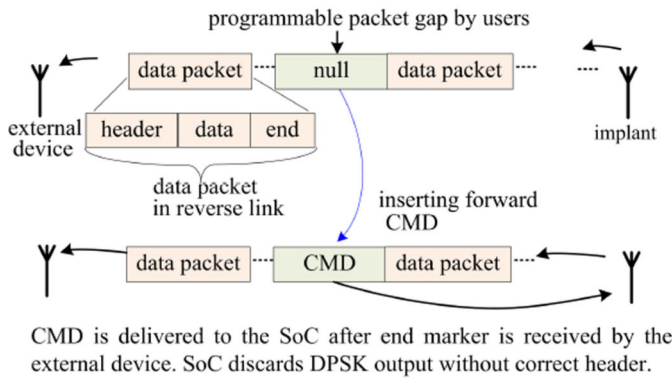
### Quasi Full-Duplex Data Telemetry



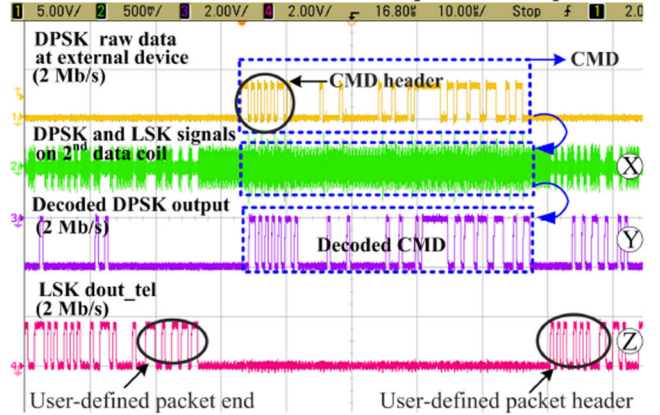
### Schematic of the quasi full-duplex transceiver



### Quasi full-duplex mode to support closed-loop system



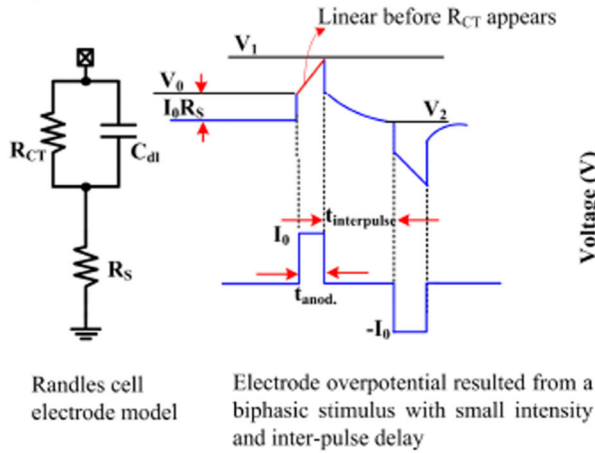
### Measured bi-directional data link under quasi full-duplex mode



**Figure 22.2.3.** Operation flow and block diagram of the quasi full-duplex data link based on DPSK (forward link) and LSK (reverse link).

### In-situ Bio-impedance Characterization

#### Proposed method



#### Recorded *in situ* electrode overpotential from paralyzed rat

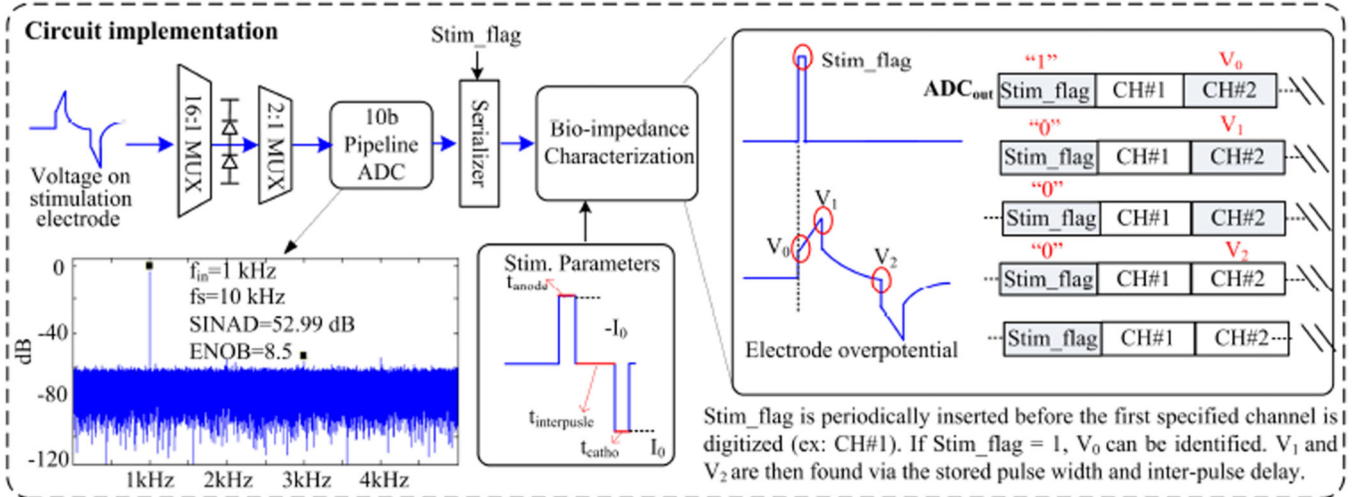
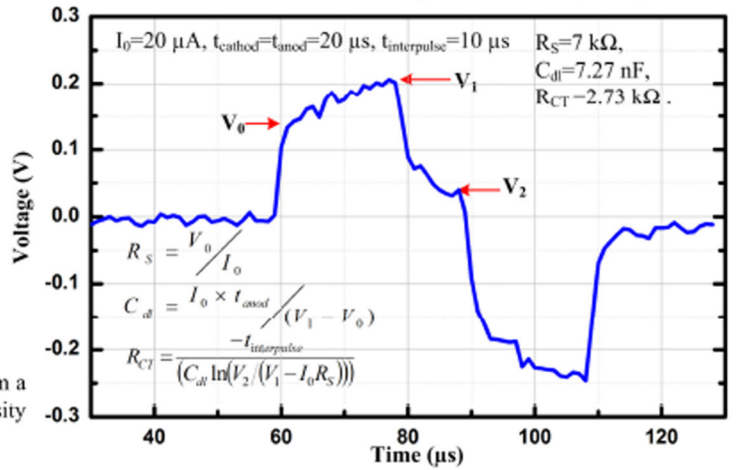
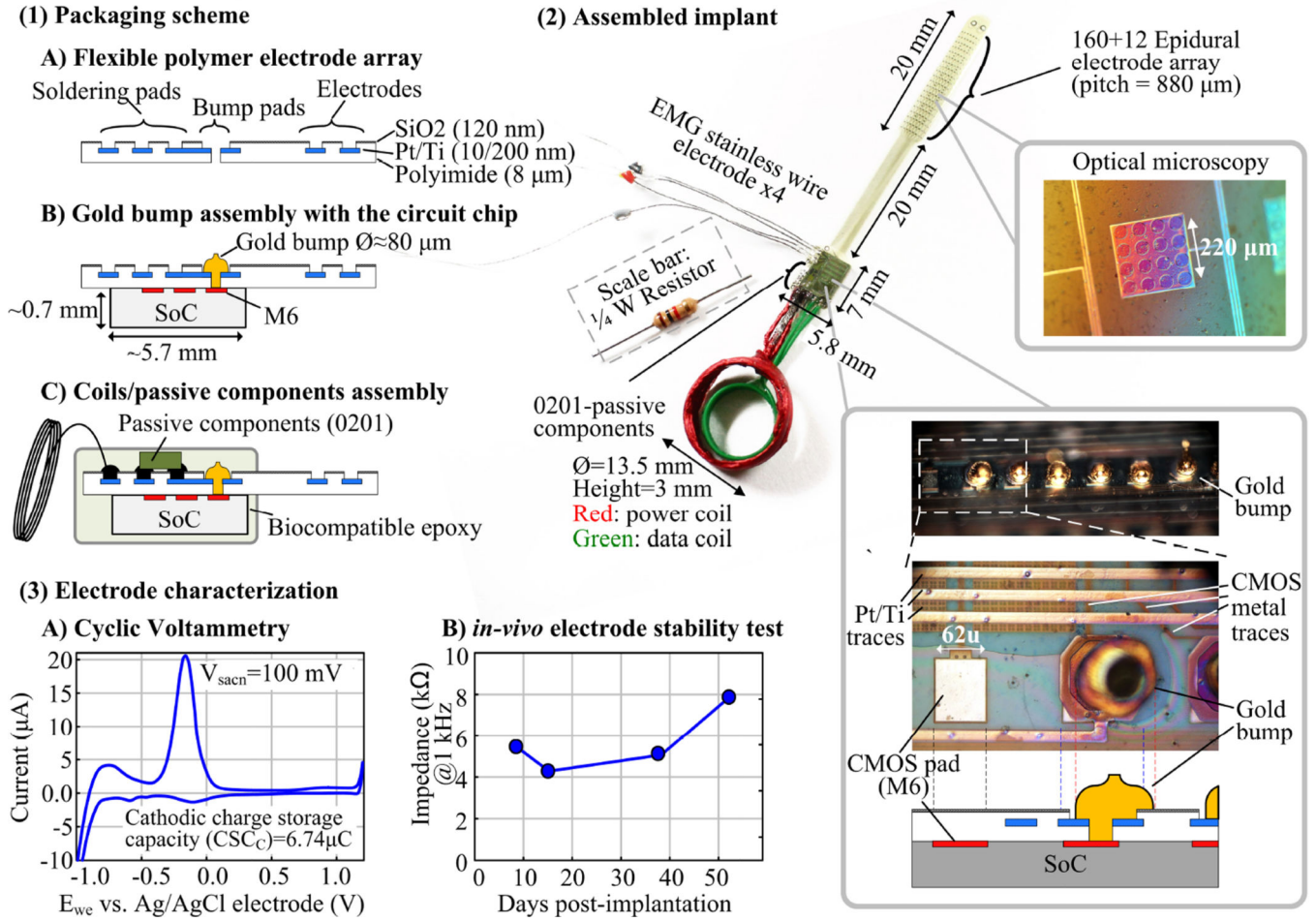


Figure 22.2.4.

Method and block diagram of bio-impedance characterization. Randles cell model is derived in the time domain.

### Thin Film Polymer Packaging Prototype

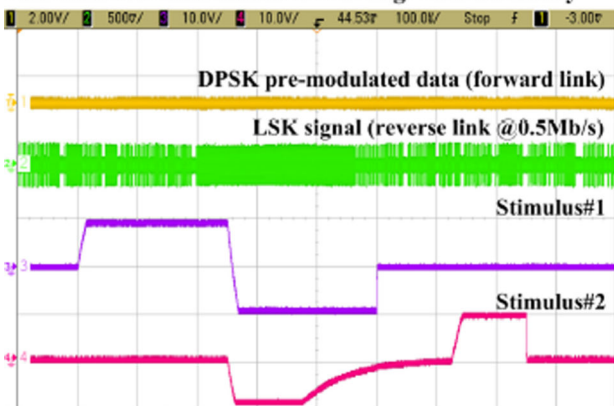


**Figure 22.2.5.**  
Thin film polymer packaging prototype.



### Results and Summary

#### Simultaneous stimulation+recording+data telemetry

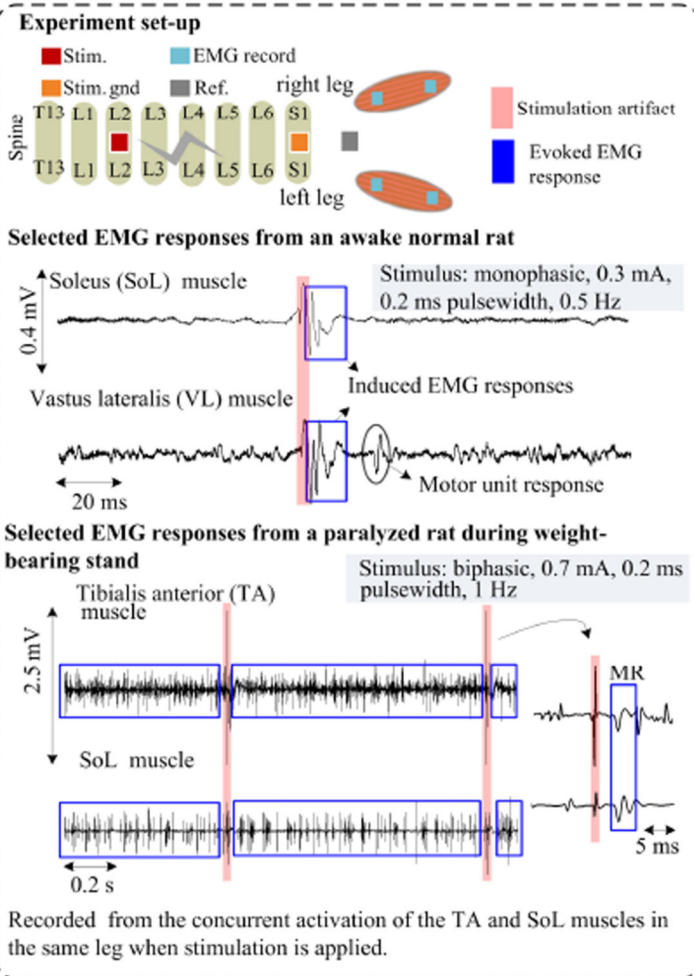


Stimulus#1: 0.25mA, 0.25ms pulsewidth (40kΩ load resistor); Stimulus#2: 0.25mA, 0.1ms pulsewidth, 0.25ms interpulse delay, 0.25ms starting delay ( 40kΩ resistor + 2.5nF capacitor load). No updated CMD is issued and grounding switch is enabled after stimulation.

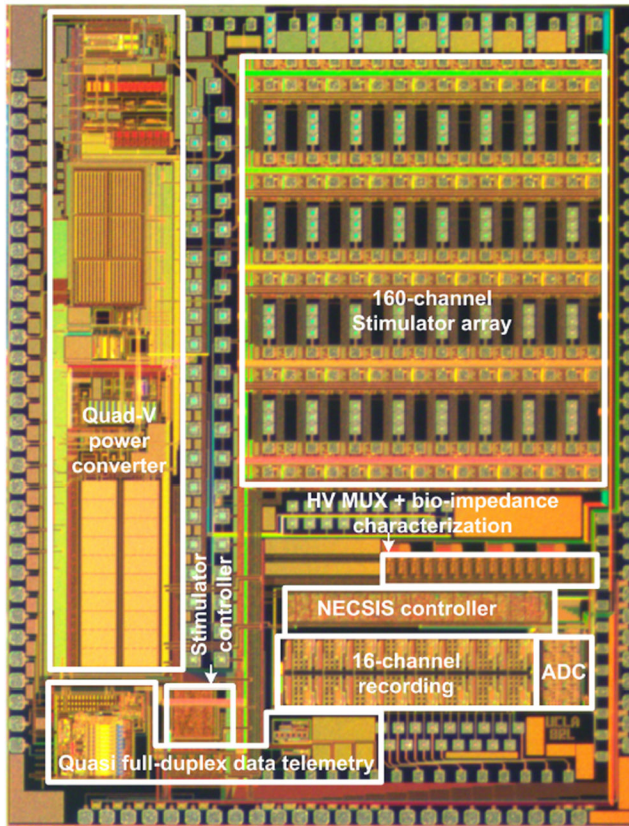
#### SoC Highlight

Application specific for closed-loop motor function recovery	
Simultaneous stim. & record	160-ch, 16-ch
Flexible stimulation parameters current/ freq./pulsewidth	Up to 0.5mA (7 bit) /up to 20kHz /up to 8ms (10μs resolution)
Wireless data link	2Mb/s full-duplex
In-situ impedance characterization	Time domain analysis
Impedance model resolution	~3.5Ω, ~17.1pF
Wireless powering	On-chip quad-voltage generation
External components	6 0201-SMD caps & 2 coils.

#### Measured stimulation-induced EMG



**Figure 22.2.6.** Experimental results and SoC performance summary.



Chip size:  $4384 \mu\text{m} \times 5694 \mu\text{m}$

<sup>a</sup>Stimulation parameters must be programmed before starting wireless recording.

<sup>b</sup>Estimated data rate.

<sup>c</sup>5 V for its stimulator is from battery.

<sup>d</sup>Defined as “(No. of stimulation + recording channel)  $\times$  (reverse + forward data rate (Mb/s))/(chip size ( $\text{mm}^2$ ))”.

<sup>e</sup>6 discrete capacitors, electrodes and 2 coils are included while [3] does not include electrodes.

	[3]	[4]	[5]	This work
Application target	Peripheral nerve	Cortex	Cortex	Spinal cord
No. of stim. channels	4	10	8	160
Stim. mode	Current	Current	Voltage	Current
Max current (mA)/ resolution (bit)	25/10	4.1/6	0.23/5	0.5/7
Stim. freq (Hz)/ PW(ms)	0.15-8.3k/ 0.01-12.8	15.4/1 (fixed)	60-220/ 0.04-0.44	Up-to 20k /0.01-8
Residual charge cancellation	N/A	N/A	N/A	Yes/ electrode grounding
No. of recording channels		4	8	16
Gain (dB)/ BW (Hz)		54/ 0.64-6k	60-74/ 0.5-3k	40-62/ 5-7k
ADC ENoB (bit)		8	6.5	8.5
Noise ( $\mu\text{V}_{\text{rms}}$ )/NEF/ power ( $\mu\text{W}/\text{Ch}$ )		6.3/3.76/ 16	1.97/2.9/ 8.6	7.68/6.2 /5.4
Full-fuplex data telemetry		N/A	N/A <sup>a</sup>	Yes
Forward data rate (Mb/s)	0.175 <sup>b</sup>	0.1	0.1	2 (DPSK)
Reverse data rate (Mb/s)	N/A	0.8	2	2 (LSK)
Impedance characterization	N/A	N/A	N/A	48 Ch., Randles cell model
Power telemetry	Yes	Yes	Yes	Yes
CMOS process (nm)	800 HV	180	180	180 HV
Supply voltage (V)	>10	1.8/ 5 <sup>c</sup> (Stim.)	1/ 4.5 (Stim.)	$\pm 1.8$ / $\pm 6$ - $\pm 12$ (Stim.)
Chip size (mm $\times$ mm)	$7.35 \times 6.8$	$2 \times 2$	$3.06 \times 2.53$	$4.4 \times 5.7$
Performance metric <sup>d</sup>	0.014	3.15	4.34	28
Implant size ( $\text{cm}^3$ )/ weight (g)	3/6	N/A	N/A	0.5/0.7 <sup>e</sup>

**Figure 22.2.7.**  
SoC micrograph and table of comparison.