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Monolithic Integration of a Silicon Nanowire Field-Effect Transistors Array on a Complementary Metal-Oxide Semiconductor Chip for Biochemical Sensor Applications

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Abstract

We present a monolithic complementary metal-oxide semiconductor (CMOS)-based sensor system comprising an array of silicon nanowire field-effect transistors (FETs) and the signal-conditioning circuitry on the same chip. The silicon nanowires were fabricated by chemical vapor deposition methods and then transferred to the CMOS chip, where Ti/Pd/Ti contacts had been patterned via e-beam lithography. The on-chip circuitry measures the current flowing through each nanowire FET upon applying a constant source-drain voltage. The analog signal is digitized on chip and then transmitted to a receiving unit. The system has been successfully fabricated and tested by acquiring $I-V$ curves of the bare nanowire-based FETs. Furthermore, the sensing capabilities of the complete system have been demonstrated by recording current changes upon nanowire exposure to solutions of different pHs, as well as by detecting different concentrations of Troponin T biomarkers (cTnT) through antibody-functionalized nanowire FETs.

There is a growing demand for sensor devices offering rapid and portable analytical functionality in real time as well as massively parallel capabilities with very high sensitivity down to the single-molecule level. Such devices are essential to facilitate research and foster advances in fields, such as drug discovery, proteomics, medical diagnostics, systems biology, or environmental monitoring.

The development of reliable and flexible sensor systems at reasonable cost, with adequate selectivity and sensitivity, is a challenging task.1 Methods requiring biochemical labeling or amplification of the target analyte are costly and time-consuming. They additionally bear the risk of altering the target analyte molecules, and thereby affecting the detection process, which is an important issue, for instance, in gene expression assessment via DNA microarrays.2 Label-free techniques are, therefore, preferable. Methods involving optical

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detection, such as surface plasmon resonance, have demonstrated their efficiency in affinity sensors.3,4 Optical techniques, however, remain difficult to integrate at large scale, as required for the production of low-cost, portable sensing devices, for applications in, e.g., personalized medicine or smart wearable systems for life-quality improvement.

Nanoscale electronic transducers based on ion-sensitive field-effect transistors (ISFETs) that can be integrated in a CMOS platform have emerged as promising devices. ISFETs were introduced in the 1970s, with the perspective of directly integrating chemical sensing into electronic devices.5 In an ISFET, the metallic gate electrode is replaced by an analyte solution whose potential is controlled by a reference electrode, e.g., Ag/AgCl. Charge carriers or ions in the liquid phase atop the gate lead to an electrostatic potential buildup. This potential depends on the nature and concentrations of the charged species, adsorbed on the oxide surface of the FET, and modifies the gate voltage or threshold voltage.6 The device architecture of ISFETs was later also adopted for nanowire-based FET devices.7 The high interest in nanowire-based ISFETs is driven by multiple arguments. Most obvious is the small dimensions of the nanowire and the size compatibility between the sensor unit and some of the sensed analytes. This aspect is crucial, for instance, in the study of biophysical mechanisms at the single molecule or single organelle level.8 Another aspect is the high surface-to-volume ratio, which enhances the sensitivity of the sensor,9 allowing for the detection of low analyte concentrations (down to the attomolar range),10–12 or of a small number of biomolecules such as proteins.13 The small size of the sensing unit results in small capacitances and, therefore, a fast response time. Not only does this small size permit local measurements with high spatial resolution, but it also allows for the integration of the sensors into large-scale arrays. Last but not least, detection systems with high sensitivity (in terms of, e.g., minimum detectable relative resistance change or threshold voltage shift) need real-time signal-conditioning circuits to improve the signal-to-noise ratio.

The use of CMOS technology to design circuits that can interface to nanowire-based sensors is an obvious choice, as it brings several advantages: (1) The integration of several circuits on the same chip, which enables the simultaneous readout of different nanowires with low noise and high temporal resolution; (2) the capability of simultaneously reading out an array of sensors, offering the possibility to correlate measurements in time and space for identical sensors13 and to conduct multiple measurements by means of arrays with differently functionalized sensors; the latter approach is important to ensure, e.g., reliable disease marker detection or disease diagnosis, which often requires the identification of multiple molecular markers.14 (3) The performance of the nanowire sensors can be improved by alleviating some nonidealities of the sensors, e.g., hysteresis.15 Ideally, the nanowire sensor and the readout circuit should be monolithically integrated on the same substrate, as this allows the sensor signal to be amplified and digitized right where the sensor is. By also including analog-to-digital conversion units, only digital signals are sent off-chip, thus avoiding lengthy analog connections between the sensor and the readout chip. As digital connections are much more robust against noise and parasitic effects, the overall performance of the sensing system is enhanced. Furthermore, small-size devices with reduced costs and increased mobility can be obtained.

CMOS readout chips for silicon nanowire (SiNW) sensors have been previously reported, being however mostly limited to a two-chip approach.16,17 Papers demonstrating monolithic integration of nanostructures over a CMOS chip have also been presented, failing though to either show one-dimensional nanoscale devices needed to achieve high sensitivity or to integrate sensor arrays. The works in Narayanan et al.18 and Evoy et al.19 use dielectrophoretic forces to align rhodium nanorods with electrodes that were previously fabricated on a CMOS chip featuring a readout circuit. Even though such an approach is quite simple and allows for the fabrication of nanodevice arrays, the diameter of each nanostructure is larger than 150 nm and no sensing experiments have been shown. Previous work from our group20 included an array of gold nanowires patterned directly over a CMOS chip including the readout circuits. Cross sections smaller than 31 × 15 nm^2 could, however, not be reached so that only very small signal changes could be observed upon sensor exposure, which rendered metal nanowires not the best choice for many sensor applications. The work reported by Yen et al.,21 Huang et al.,22 and Huang et al.23 relies on a modified standard 0.35 μm CMOS process to fabricate a single poly-Si nanowire together with a readout circuit. The cross-section of the poly-Si NWs is, however, relatively large (170 × 625 nm^2), and sensor arrays have not been demonstrated.

The work in this paper makes use of cylindrical 20 nm diameter-SiNWs that have been chemically synthesized by the bottom-up vapor−liquid−solid (VLS) growth mechanism, rather than using standard top-down microfabrication processes.24 Chemically synthesized SiNWs can be prepared as single-crystal structures, with controllable diameters as small as 2−3 nm, with complementary p- and n-type doping.25–30 Some limitations of planar SiNW FETs can be overcome by FETs based on chemically synthesized SiNWs: their one-dimensional morphology and nanometer-scale cross-section allows for effective depletion or accumulation of charges upon binding of a species to the surface across the whole cross-section of the device; in planar devices, instead, only the surface region can be depleted or accumulated.8,10,31–33 This unique feature of chemically synthesized SiNWs has allowed for the detection of single particles.8 The chemical synthesis of SiNWs is straightforward34 and requires only nanowire bottom-up assembly together with a single-step lithography to define the metal contacts on the device chip. Furthermore, chemically synthesized SiNWs can be assembled on a wide variety of surfaces, regardless of the bulk material. Chemically synthesized SiNWs are, therefore, the perfect candidate for a monolithic integration of high-sensitivity sensors on a fully developed CMOS chip.

Experimental Methods

We present a prototype of a complete sensing system, featuring the monolithic integration of an array of 16 chemically synthesized SiNW FETs with a CMOS chip that hosts all needed electronics to simultaneously read out all the nanowires. Each SiNW has a diameter of 20 nm and has a dedicated readout circuit that digitizes the sensor signal. A new packaging scheme has also been developed and used, in order to include a microfluidic channel over the sensing area, while at the same time protecting the electronics. This allows for the use of small liquid volumes and for shorter response times, as the target analyte is directly brought to the sensor surface and does not have to first diffuse through big reservoirs.21,22

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The sensing experiment results demonstrate the successful integration of the nanowire elements on the chip and show measured responses upon exposure of the nanowire-based FETs to solutions of different pH-values. Finally, the system has also been validated by measuring different concentrations of the human cardiac marker Troponin T (cTnT) at concentrations down to 1 nM with antibody-functionalized FET devices.

System Description

A schematic view of the overall system presented in this work is shown in Figure 1A. The system comprises a CMOS chip, featuring both the readout electronics and the SiNW-based FET array, and an FPGA (field-programmable gate array) for data processing and communication to a host PC through a USB connection.

All the blocks have been assembled on a custom-designed printed circuit board (PCB), which also provides analog reference voltages and digital settings for configuration of the readout circuits. Moreover, the PCB includes two circuits realized with discrete components that convert the 5 V supply from the USB connection into two independent and low-noise 3.3 V voltages that are used to power the analog and digital circuits in the CMOS chip. A novel PDMS-based package for the CMOS chip has also been developed to deliver the liquid solution to the sensing area and to protect the interface electronics. Each block is described in more detail in the following sections.

A Graphical User Interface (GUI) was developed by using the programming language C#. The developed program allows for real-time plotting and recording of the received data on the host PC. The data are saved in a file using a high-priority thread. The real-time plots are updated every second.

CMOS Chip

The CMOS electronics have been characterized in a two-chip scenario, where the CMOS chip on a PCB was successfully interfaced to a separate sensor chip, which was mounted on a second PCB and featured an array of SiNW FET sensors.15 Therefore, we here only abstract the features and performance parameters of the CMOS chip that are relevant to monolithic integration.

The CMOS readout chip consists of two parts: (i) the conditioning circuitry and (ii) 16 pairs of platinum contacts. The circuitry includes 16 voltage buffers that define the voltage on one side of the contacts, 8 sigma-delta (Σ−Δ) modulators and 8 current-to-frequency (ItoF) converters. The latter two circuits are used to maintain a defined voltage on the other side of the contacts while measuring and digitizing the current.

Each voltage buffer consists of an operational amplifier, configured in unity-gain feedback, which can provide voltages between 500 mV and 2.5 V to one side of the contacts. The employed operational amplifier has a class-AB output stage, providing a good driving capability, i.e., loads as big as 20 nF can be driven, at low power consumption. Each ItoF converter comprises an input current conveyor, an integrating capacitor, and a comparator. The circuit schematic of the ItoF converter is shown in the Supporting Information in Figure

SF1. Together with an external counter, the ItoF converter implements an analog-to-digital converter (ADC).

The current conveyor buffers the current flowing from the integrated contacts, while the voltage is fixed due to the low input impedance of the conveyor. The current is then integrated on a capacitor and converted to a voltage. This voltage is compared to a reference voltage: each time it crosses the reference voltage, a reset pulse is created and the integrating capacitor is discharged. As a result, a train of output pulses is generated that all have the same duration: the frequency of these pulses then encodes the input measurement current.

Three different integrating capacitors are included on the chip and can be adjusted according to different current ranges: 200 fF (for the range 200 pA to 400 nA), 1 pF (for the range 400 nA to 1.4 μA), and 10 pF (for the range 1.4 μA to 3 μA). By having three different integrating capacitors, the range of the measured input current can be extended without losing resolution, which renders the system suitable for a wide range of applications. Two different bandwidths can be selected by changing the conversion time in the FPGA, i.e., either 100 ms (slow-mode) or 1 ms (fast-mode).

The ItoF converter achieves a resolution of about 11 effective number of bits (ENOBs) (in the slow-mode) and of 7 ENOBs (in the fast-mode) in the current range from 200 pA to 3 μA. The highest measured noise in the slow-mode is 38 pA_{RMS} with an integrating capacitor of 10 pF and input current of 3 μA. The noise decreases to only 8.2 pA for a smaller input current (50 nA) by using the 200 fF integrating capacitor. Each ItoF converter consumes 230 μW and occupies an area of 490 × 105 μm^2.

Each Σ−Δ modulator features a second-order architecture with two switched-capacitor integrators.35 The circuit schematic of the Σ−Δ modulator is shown in the Supporting Information, SF1. The output of the Σ−Δ modulator is a train of pulses, whose time duration is different. The pulses are sampled at a fixed frequency.

The Σ−Δ modulator provides high resolution (more than 13 bits) in a very wide input current range (±2 μA) at a signal bandwidth of 1 kHz; it requires, however, a 1 MHz clock and an oversampling ratio of 256. The RMS noise level is 250 pA. Lower noise levels can be achieved by trading bandwidth with input current range; as an example, the RMS noise decreases to 16.8 pA in the ±100 nA range at a bandwidth of 1 kHz, whereas the RMS noise is only 220 fA in the smallest range of ±100pA at a bandwidth of 100 Hz.35 Each Σ−Δ modulator consumes 1.47 mW and occupies a chip area of 660 × 203 μm^2.

An important issue for monolithic integration of nanostructures onto a processed CMOS chip, which usually has a corrugated surface topography, is to provide a sufficiently large featureless and flat area to accommodate the nanowires as well as stable electrical contacts. For the used 0.35-μm CMOS technology (X-Fab Erfurt, Germany) with 4 metal layers, the layer stack is polished after metal 3 to achieve a flat surface for the remaining steps and layers. We designed the CMOS chip to not feature any metal layer and, in particular, no metal-4 layer in the nanostructure area between the metal contacts so as to ensure maximum flatness obtainable with the given CMOS technology (schematic in Figure 2A and cross-sectional SEM image in Figure 2B).

A total of 16 integrated platinum contact pairs were used to connect the nanowires to be placed on the chip surface to the readout circuits. After the CMOS fabrication, the passivation deposited by the CMOS fab has first been opened in order to gain access to the top metal layer (shown in Figure 2B at the right, where the post-CMOS Pt is in contact with CMOS metal 4). Then, the platinum contacts were formed by blanket deposition and subsequent ion beam etching (IBE) or patterning of a metal layer stack consisting of 50 nm tungsten−titanium (WTi) and 270 nm platinum (Pt). An in-house passivation stack of SiO_2 and Si_3N_4 was then deposited in order to protect the chip surface and circuits underneath. Finally, the in-house passivation layer was removed in the area between the contacts and at the contacts by reactive ion etching (RIE). Each contact at the chip surface has an area of 50 × 50 μm^2, the distance between two contacts is 400 μm, and the contact pair spacing is 50 μm. In between the contact pairs the surface stays flat, which facilitates the nanowire integration over the chip. The chip total area is 3.4 × 4 mm^2.

A summary of the main features of the presented CMOS chip is shown in Table 1, where also a comparison with other relevant systems that have been recently published can be found. A photograph of the chip is shown in Figure 1B. Figure 2A shows a micrograph of the chip with a zoom-in on the 16 contact pairs (before the Pt deposition).

Silicon Nanowire Array

The SiNWs were synthesized by chemical vapor deposition (CVD), as previously described. 36 20 nm gold nanoparticles, which served as catalyst sites for the vapor−liquid−solid (VLS)-CVD growth of Si nanowires, were initially deposited on Si (100) growth substrates. The diameter of the gold nanoparticle catalyst defines the diameter of the resulting SiNWs. To promote the adhesion of the gold nanoparticles to the silicon substrate, a poly-L-lysine solution was applied to the bare silicon wafer as an electrostatic binding agent. The nanoparticle-coated wafer was then placed in a horizontal tube furnace for the growth of the SiNWs. Silane and diborane were used as reactants during the growth, to provide boron as a p-type dopant with a B/Si ratio of 1:4000.

After the synthesis, the SiNWs were transferred to the CMOS chip. First, the CMOS chip was cleaned with plasma oxygen at 50 W for 3 min. SiNWs were then deposited by random dispersion in the area between the 16 integrated platinum contact pairs. The dispersion process involves removal of the SiNWs from the growth substrate into ethanol solution by sonication, and the subsequent deposition of droplets of the NWs−ethanol suspension onto the CMOS substrate. The SiNWs were then electrically connected to the source and drain platinum contact pairs of the CMOS chip by e-beam lithography. A multilayer of resists, consisting of methyl methacrylate (MMA) and polymethyl methacrylate (PMMA), was used for e-beam writing, followed by e-beam evaporation of 5 nm chromium (Cr) to avoid charging effects. After the e-beam writing, the chip was immersed in Cr etchant, followed by development of the electrode pattern in methyl isobutyl ketone (MIBK). The contacts were metallized by e-beam evaporation of Ti/Pd/Ti (5/60/8 nm, respectively) and were passivated with an insulating layer of Si_3N_4 (100 nm thick), deposited by plasma-enhanced chemical vapor deposition (PECVD). The distance between the electrodes was 3 μm for each SiNW. The e-beam resist was then removed via lift-off by immersing the chip in acetone for a few

hours. Figure 1B shows photographs and SEM images of the SiNWs deposited on the CMOS chip.

CMOS Chip Packaging

A package allowing for measurements in the liquid phase was developed. The readout circuits needed to be protected from the liquid phase. At the same time a microfluidic channel was required to bring a precisely controlled small volume of liquid onto the nanowire-based FET devices area. Furthermore, since the chip is glued and bonded to a printed circuit board (PCB), the bond wires must be protected as well. In order to achieve these goals, a PDMS block was designed and fabricated by using a SU-8 mold. The PDMS block includes two microchannels, both roughly 550 μm high: a wide one (about 4 mm) to cover the bond wires; a smaller one (200 μm wide, 1.6 mm long), connected to an inlet and an outlet, to bring the liquid solution to the nanowires. The CMOS chip is submerged and embedded into the PCB in order to avoid chip misalignment (with respect to the PCB), to reduce the height of the bond wires, and to get an almost flat surface over chip and PCB, which facilitates a good adhesion of the PDMS block. A sketch of the chip that has been embedded in the PCB and covered by the PDMS block is shown in Figure SF2-C in the Supporting Information.

Figure SF2-A shows a photograph of a fabricated PDMS block: the microfluidic channel is filled with a red liquid, whereas black lines indicate the chamber protecting the bond wires and the CMOS circuit area of the chip. Figure SF2-B shows a micrograph of the microfluidic channel placed over the CMOS chip filled with red liquid. Finally, a PMMA cover mechanically clamps the PDMS block onto the PCB. Figure 2C shows a completely packaged chip, ready for experiments in the liquid phase. The inlet and outlet tubes for liquid handling can also be seen.

Results and Discussion

Electrical Characterization

The first measurements were performed without liquid, to verify proper connection of the SiNWs to the readout circuits. Figure 3A shows the drain current flowing through 27 different SiNWs (patterned over two separate CMOS chips), as a function of the drain-source voltage applied across them. As expected from previous experiments, using similar SiNWs,36 the curves show a linear behavior in the applied voltage range, and the values of the measured current match with previous results.35 Furthermore, the conductance of each SiNW was computed from the value of the drain current measured at a drain-source voltage of 600 mV and was then used to normalize the measured drain currents of all SiNWs. This way, differences in nanowire responses as a consequence of different SiNW lengths (between 25 and 30 μm) could be accounted for. Such a calibrated response is plotted as a function of the drain-source voltage in Figure 3B. This graph shows how the electrical response of the SiNWs, except for three of them, is quite uniform, even across two different chips.

The second experiment was carried out in liquid solution (PBS) by applying a voltage to the liquid in order to verify whether the SiNW FETs could be properly gated or not. The PBS electrolyte solution was brought onto the SiNW surfaces by using the microfluidic channel. A flow-through Ag/AgCl reference electrode was utilized to regulate the voltage of the liquid solution, which acts as a gate voltage for the SiNW FETs. During this experiment the drain-source voltage was fixed at 200 mV, and the gate voltage, i.e., the voltage applied to the reference electrode, was swept from −500 mV to 300 mV, while the drain current was measured. Figure 3C shows the results acquired from nine different SiNW FETs patterned on the same chip. As expected, the curves show the typical dependence of the drain current on the gate voltage observed for standard p-type FETs. Also in this case, the conductance of each SiNW was computed (from the value of the drain current measured at a gate voltage of −200 mV) and used as a factor to normalize the measured drain currents of all SiNWs. Such a calibrated response is plotted as a function of the gate voltage in Figure 3D. This graph shows that the electrical response of all SiNWs is very uniform.

pH Sensing Experiments

In order to validate the sensor response of the system, experiments with liquid solutions of different pH values were performed in a first step. A pump was used to control the flow rate of the liquid solution, and the flow-through Ag/AgCl reference electrode was utilized to control the voltage of the liquid solution, i.e., the gate voltage.

The pH sensitivity of the Si-nanowires comes from the silanol groups (Si−OH) of the native Si-oxide layer on the surface of the SiNWs: at high pH values (>7) the silanol groups get deprotonated, providing negative charges on the gate, whereas at low pH values (<7) the silanol groups get protonated, providing therefore positive charges on the gate. The SiNWs used in this work were p-doped, i.e., p-channel devices, therefore pH-values larger than 7 will cause an increase in the threshold voltage and in the drain current (for a fixed gate voltage), whereas pH-values lower than 7 will result in a decrease of the threshold voltage and of the drain current (for a fixed gate voltage).

There are, therefore, two ways to perform a pH measurement: (1) measuring the threshold voltage of the SiNW and (2) measuring the current flowing through the SiNW. In the first scenario, the curve showing the dependence of the drain current on the gate voltage must be acquired for each SiNW FET and for each pH value: the gate voltage applied through the reference electrode is swept, while the drain current is measured. The drain-source voltage across the SiNW was kept constant (200 mV). pH-measurements are shown in Figure 4A, where the measured drain current of one SiNW FET for three different pH values (4, 7, and 9) has been plotted on a logarithmic scale as a function of the gate voltage applied through the reference electrode. The curves show an almost linear shift obtained at the different pH values (~35 mV/pH), which confirms the theory laid out above and demonstrates the sensing characteristics of the fabricated SiNWs.

For the second measurement method, the voltage on the reference electrode was maintained, and the drain current was continuously measured over time, while the pH values of the solution were varied. The voltage applied to the reference electrode (700 mV) was chosen in order to bias the SiNW FET in the weak inversion regime, as this was demonstrated to be the

regime with the highest sensitivity.36 The experimental result is shown in Figure 4B, where the drain current changes, ΔI_d, per pH value are plotted versus time (the current measured for a pH of 4 has been taken as the zero level). In the graph of Figure 4B it is also possible to observe the effect of air bubbles that accidentally entered the microfluidic channel upon changing the liquid solution: The air bubbles screen the gate voltage applied through the reference electrode and render the system electrochemically unstable so that large peaks in the measured currents occurred.

cTnT Measurement

Once the correct functioning of the complete setup was verified also with liquid experiments, the potential of the sensing system to detect proteins at low concentration was verified by measuring the human cardiac marker Troponin T (cTnT). The Troponin complex protein is a key player in the regulation of cardiac muscle contraction. Specifically, the cardiac troponin T (cTnT) and the cardiac troponin I (cTnI) are widely used in the diagnosis of acute myocardial infarction (AMI). These two markers have been detected in patients' blood between 3 and 6 h after the onset of chest pain, with a very high concentration in blood samples detected up to 10 days after onset of the symptoms.38 Since cardiovascular diseases are among the most lethal ones in the Western World, a portable device that is able to predict the early onset of such a disease is of great relevance.

In order to perform cTnT detection experiments, the surface of the SiNWs needed to be chemically functionalized. Antibodies specific to cTnT were bound to the oxide surface of the nanowires by conventional silane chemistry. This way the surface can bind cTnT molecules in solution. The functionalization steps are described in depth in the Supporting Information of Elnathan et al.38 Briefly, amine groups were introduced to the nanowire surface by using (3-aminopropyl)-triethoxysilane (APTES), then the antibodies were attached to the nanowire surface through their free amine groups by a glutaric dialdehyde cross-linking step, and then, the unreacted aldehyde terminal surface groups were passivated. Both the cTnT and the specific antibodies were commercially purchased. Four solutions with different concentrations of cTnT (20 nM, 10 nM, 5 nM, and 1 nM) were prepared by diluting the cTnT into diluted PBS (0.1 mM PBS). By using diluted PBS, the ionic strength of the liquid solution could be reduced, increasing therefore the Debye screening length (i.e., the distance at which the surface potential of the nanowire sensor is completely screened, resulting in no response to the analytes in the liquid solution).38 This way, the sensitivity of the nanowire sensors can be enhanced. The four solutions had the same pH value (8.4), and were kept at room temperature during the experiment.

Using the same setup employed for the pH measurements, the solutions with different concentrations of cTnT (starting with 1 nM) were pumped over the SiNW-based FET devices. The voltage on the reference electrode was fixed at 0 V (weak inversion regime for higher sensitivity37); the drain-source voltage across the nanowires was instead fixed at 200 mV. The gate voltages applied for the experiments shown in Figures 3C,D and 4A and for the cTnT detection are not the same, because different chips have been used for the different experiments, all having different threshold voltages and, therefore, requiring different gate voltage ranges.

Figure 5 shows the average calibrated response with standard deviation (the error bars) measured for 10 nanowires upon injection of the different concentrations of cTnT. Each point in the graph of Figure 5 was computed as the difference between the response measured when the signal stabilized after the injection of the cTnT and the response measured when only sensing buffer (i.e., 0.1 mM PBS at pH 8.4) was injected.

The calibrated response was computed according to the same procedure described above, i.e., dividing the measured drain current by the computed conductance of each nanowire. The graph in Figure 5 clearly shows how the response increases, as expected, for increasing concentrations of cTnT: even at a concentration as low as 1 nM, a response of about 170 mV can be observed.

The inset of Figure 5 shows how the current measured over time for one nanowire changes according to the injection of the different concentrations of cTnT. The sensing buffer was first injected, whereas the protein was always injected after 120 s. As the graph shows, after injection of cTnT, the drain current consistently increases. Since the isoelectric point of cTnT is around 6, at pH 8.4 the net charge associated with the protein is negative. The SiNWs used in this experiment are p-type FETs, therefore an increase in negative charge on the surface will result in a current increase, as correctly observed. The initial value was measured during injection of only sensing buffer (0.1 mM PBS at pH 8.4); each protein concentration was injected at 120 s.

Conclusions

The monolithic integration of an array of chemically synthesized SiNWs (20 nm diameter) over a CMOS chip with the interface circuitry has been shown for the first time. The complete sensing system has been successfully fabricated and tested.

The CMOS chip can regulate the voltage across the SiNWs, while measuring the current flowing through them. Two different ADCs have been implemented and successfully used in experiments, which confirmed the versatility and the good performance of the circuits shown in Livi et al.15 The ItoF converter can cover a very wide input current range while featuring a very good resolution of 11 bits and noise levels as low as to 8.2 pA_{RMS}. Although the Σ−Δ can provide even higher resolution and better noise performance, the ItoF converter is about 60% smaller and consumes 84% less power. The ItoF is, therefore, the best choice for fully integrated sensor systems that require small footprints and operation with very low power budgets, which is the case for all portable devices.

The SiNWs were successfully transferred to the chip after CMOS fabrication, and leads to the nanowires were realized on the CMOS chip by means of e-beam lithography. The integrated SiNWs on the CMOS chip showed the same basic characteristics as on other substrates before, as has been confirmed in measurements.

A new packaging scheme has been successfully applied, which includes a PDMS block with a microfluidic channel for liquid exposure and a cavity that protects the bond wires. The required liquid volume can be minimized, and the sensor response becomes very fast. A

small volume is also beneficial in case the analyte is costly or one wants to run several analyses with a small overall analyte volume.

The SiNWs could be successfully gated through the liquid solution using a flow-through Ag/AgCl reference electrode. The sensing characteristics of the SiNWs were assessed by measuring aqueous solutions of different pH values and different concentrations (down to 1 nM) of cTnT, a relevant human cardiac marker used for acute myocardial infarction detection.

In comparison to other relevant systems (including a CMOS readout chip and nanowire-based sensor arrays) recently published in the literature, the CMOS microsystem presented in this paper features the largest input range while having the lowest noise levels, the highest resolution, and the largest bandwidth (see Table 1). Furthermore, it is the only system that is suitable for the monolithic integration of a nanowire sensor array directly on the CMOS chip.

The presented work is a successful proof-of-concept, showing the attractive prospects of combining SiNW FETs with CMOS technology for biochemical sensing applications. The presented system represents a first prototype of potentially very compact and low-power diagnostic device.

Supporting Information

Refer to Web version on PubMed Central for supplementary material.

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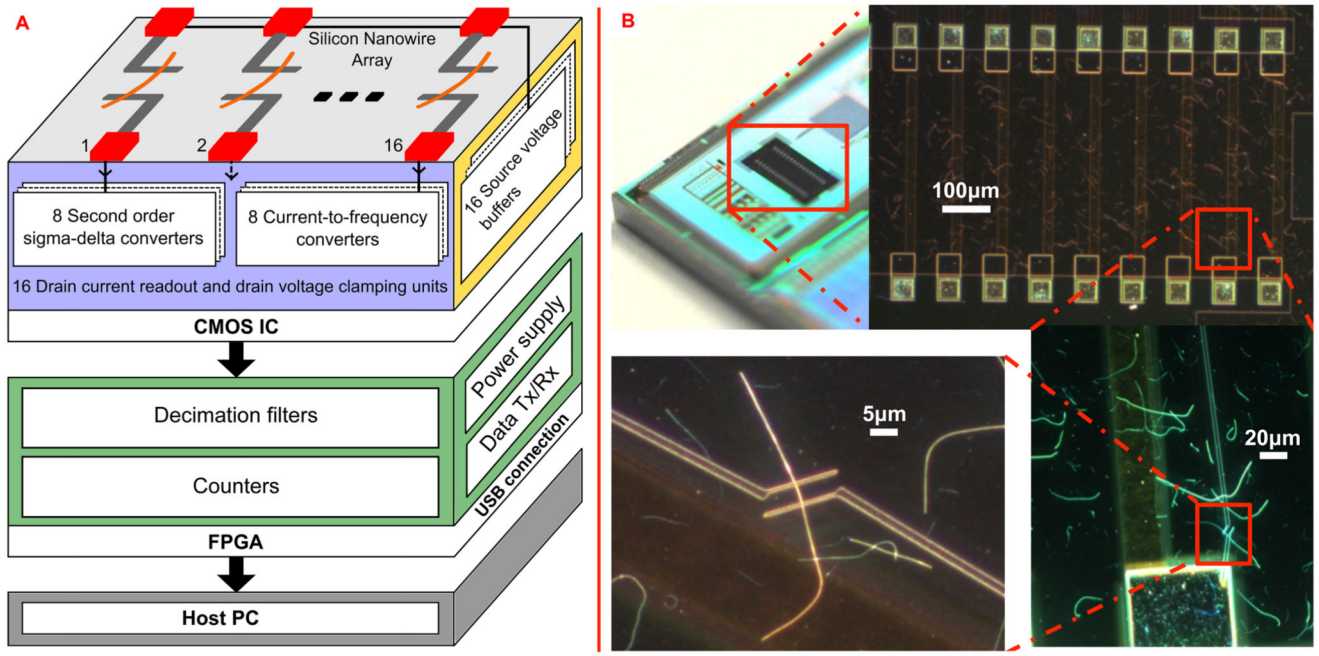

Figure 1.

(A) Building blocks of the overall sensing system and circuitry units of the CMOS readout chip. The nanowire sensor array is monolithically integrated directly on the CMOS chip, which has been mounted on a printed circuit board (PCB). The CMOS chip outputs are processed and then transmitted to a host PC by a FPGA. The acquired data are visualized and stored on the host PC with the help of a C# software interface. (B) Photograph of the CMOS chip highlighting the area where the SiNWs have been transferred to. SEM images at different magnifications of the SiNWs and of the electron-beam patterned Ti/Pd/Ti leads are shown. The diameters of the SiNWs amount to 20 nm.

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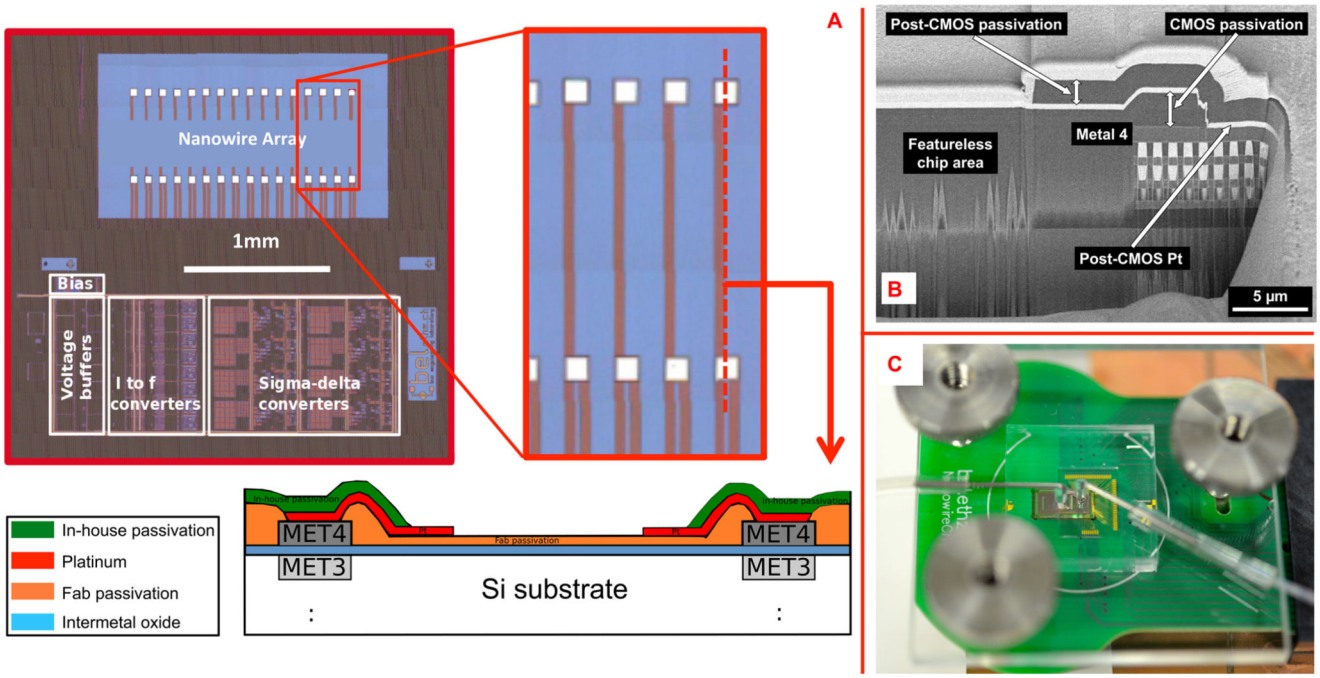

Figure 2.

(A) Micrograph of the fabricated CMOS chip with zoom-in on the integrated contacts (before the Pt deposition) used to connect the SiNWs to the circuitry. A sketch of the cross-section between a contact pair is also shown. (B) Focused-ion beam (FIB) cut through the CMOS chip in vicinity to the nanowire contacts: (left) featureless area between the contacts for deposition of nanostructures; (right) the 4 aluminum metal layers including vias of the CMOS chip and the post-CMOS Pt layer, which then serves as an inert electrical contact to the nanostructures in the featureless area. The bright top Pt layer has only been deposited for the FIB cutting. (C) Photograph of a complete and packaged system for experiments with liquid solutions. A PMMA cover clamps the PDMS block onto the chip/PCB surface; the inlet and outlet liquid ports are also visible.

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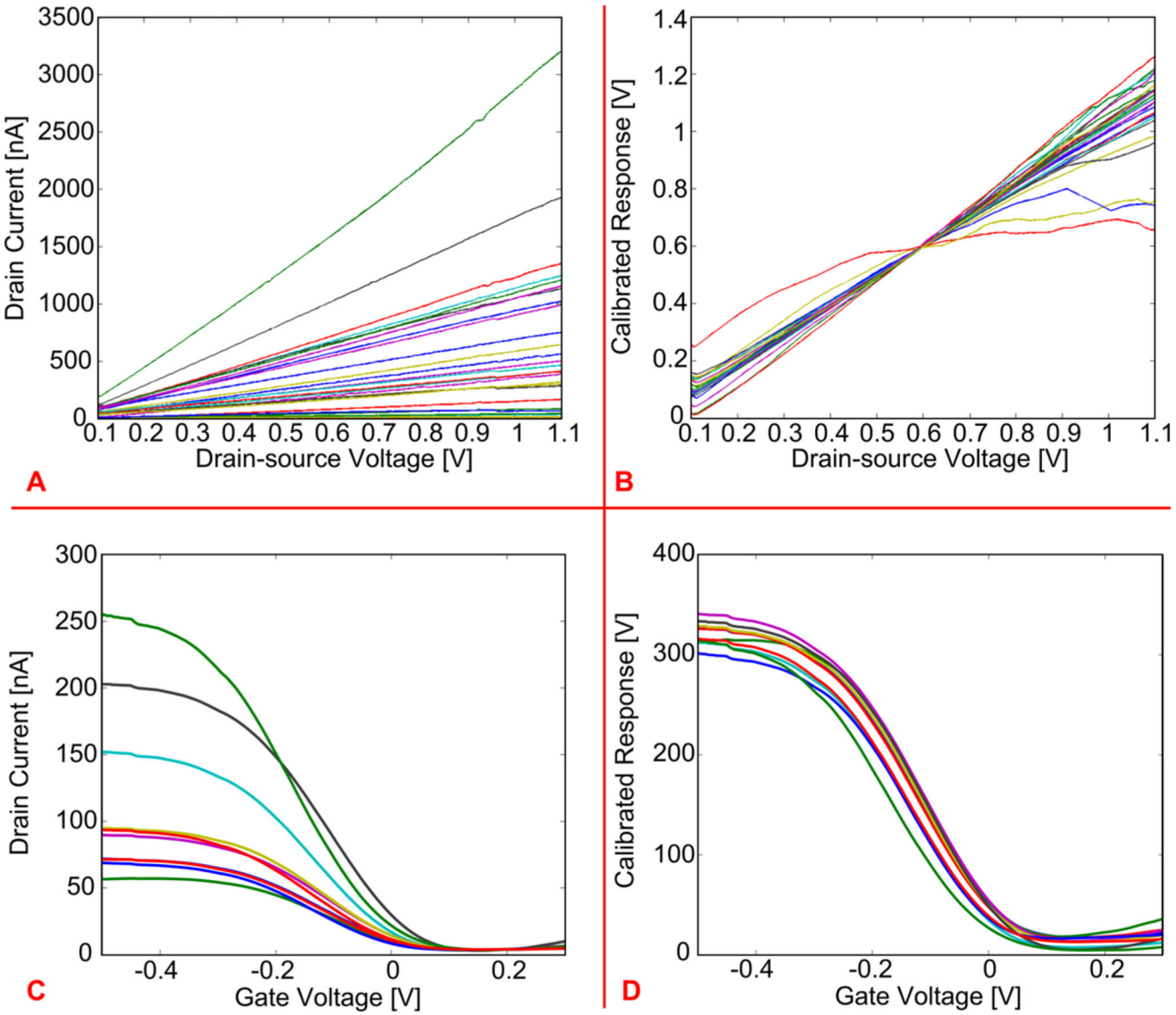

Figure 3.

(A) Drain current as a function of drain-source voltage of 27 SiNWs fabricated on two separate chips. (B) Normalization of the curves in part A according to the conductance computed per each SiNW. (C) Drain current of 9 SiNWs as a function of the gate voltage, i.e., voltage applied through a Ag/AgCl reference electrode to a liquid solution (PBS) over the SiNWs. (D) Normalization of the curves in part C according to the conductance computed per each SiNW.

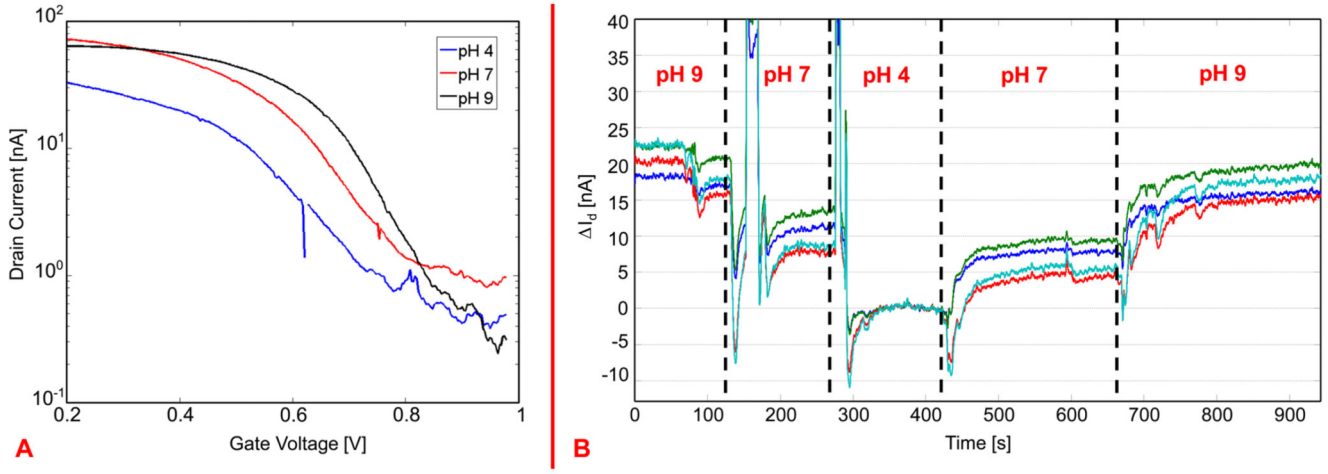

Figure 4.

(A) Measured drain currents (plotted in log scale) of one SiNW FET as a function of the gate voltage, i.e., voltage applied to the reference electrode in the liquid solution, for different pH values. The plot shows the threshold voltage shifts induced by the pH changes. (B) Drain current changes versus time as a function of different pH values as measured simultaneously from 4 SiNWs; the current measured at pH 4 is taken as the zero level, and the current differences, ΔI_d, in reference to the current values at pH 4 are plotted.

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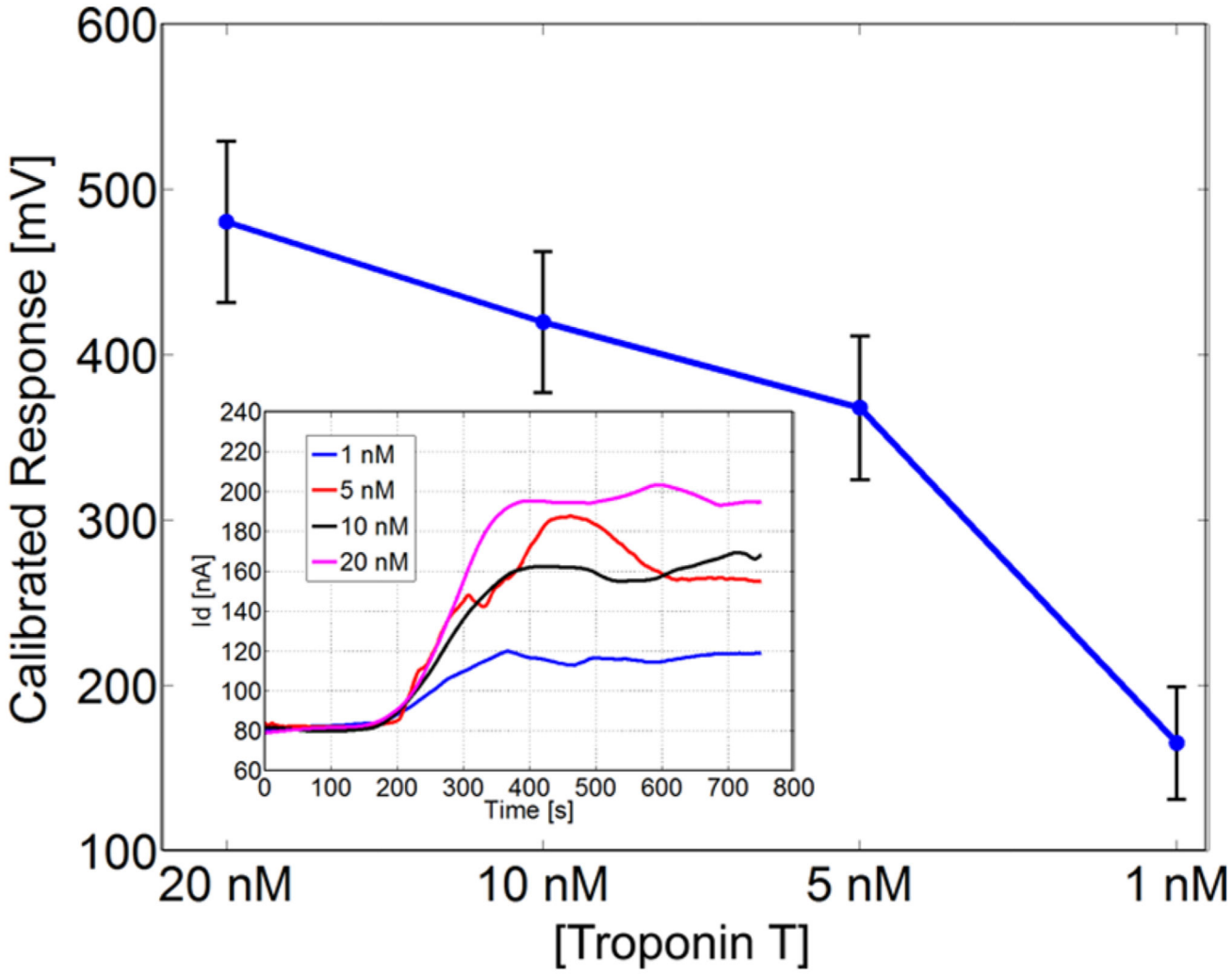

Figure 5.

Average calibrated response with standard deviation (error bars) measured for 10 nanowires upon injection of different concentrations of human cardiac troponin T (cTnT). Inset: Drain current changes versus time as a function of different cTnT concentrations for one nanowire. The initial value was measured during injection of only sensing buffer (0.1 mM PBS at pH 8.4); each protein concentration was injected at 120s.

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Table 1

Comparison between the Presented CMOS-Based Nanowire Sensing System and Other Relevant CMOS Systems Recently Published in the Literature

	ref 16	ref 17	ref 23	this work
technology	0.18 μm	0.18 μm	0.35 μm	0.35 μm
readout scheme	Res. to Freq converter	TIA + single slope ADC	V amp. + SAR ADC	$\Delta\Sigma$ + I to Freq converter
input range	100 kΩ to 1 GΩ	100 pA to 5.3 nA	n.a.	20 pA to μA (7 kΩ to 7.5 GΩ)
channel count	1	64	1	16
multiplexed	yes	no	only 1 sensor	no
min/max resolution	5/7 bits	10 bits	9.4 bits	6.6/13.3 bits
min/max noise	n.a.	$7pA_{RMS}$	n.a.	$0.54/250pA_{RMS}$
bandwidth	100 Hz	300 Hz	100 kHz	1 kHz (max)
power supply	1.8 V	1.8 V	3.3 V	3.3 V
power consumption	396 μW	1.8 mW	600 μW	35 mW
chip size	200 × 200 μm^2	4.3 × 4.3 mm^2	6.2 mm^2	3.4 × 4 mm^2
notes	2 chips	2 chips	monolithic (1 NW)	2 chips and monolithic