Resonant Rectifier ICs for Piezoelectric Energy Harvesting Using Low-Voltage Drop Diode Equivalents

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Abstract: Herein, we present the design technique of a resonant rectifier for piezoelectric (PE) energy harvesting. We propose two diode equivalents to reduce the voltage drop in the rectifier operation, a minuscule-drop-diode equivalent (MDDE) and a low-drop-diode equivalent (LDDE). The diode equivalents are embedded in resonant rectifier integrated circuits (ICs), which use symmetric bias-flip to reduce the power used for charging and discharging the internal capacitance of a PE transducer. The self-startup function is supported by synchronously generating control pulses for the bias-flip from the PE transducer. Two resonant rectifier ICs, using both MDDE and LDDE, are fabricated in a 0.18 µm CMOS process and their performances are characterized under external and self-power conditions. Under the external-power condition, the rectifier using LDDE delivers an output power P_{OUT} of 564 µW and a rectifier output voltage V_{RECT} of 3.36 V with a power transfer efficiency of 68.1%. Under self-power conditions, the rectifier using MDDE delivers a P_{OUT} of 288 µW and a V_{RECT} of 2.4 V with a corresponding efficiency of 78.4%. Using the proposed bias-flip technique, the power extraction capability of the proposed rectifier is 5.9 and 3.0 times higher than that of a conventional full-bridge rectifier.

Keywords: AC-DC converters; energy harvesting; piezoelectric; rectifier

1. Introduction

There is increasing demand for autonomous sensing devices, deployed in various applications, such as medical, healthcare, and environmental monitoring [1]. To enable uninterrupted data gathering from a large population of sensing devices, e.g., the Internet of Things (IoT), a long lifetime is critical. Although there are continued innovations in battery capacity, battery lifetime is still finite. To extend the lifetime of sensing devices, energy can be acquired from ambient sources. There exist various sources from which energy can be extracted, including thermal, solar, vibrations, and wind. Among those energy sources, vibrations can provide a relatively large amount of energy through highly-efficient piezoelectric (PE) transducers.

The equivalent electrical model of a PE transducer is represented as a sinusoidal current source $I_P(t) = I_P\sin(\omega_p t)$ in parallel with a capacitor C_p and a resistor R_p, where $\omega_p = 2\pi f_p$ is the angular frequency. In general, R_p is very large during low-frequency transducer operation, and the open-circuit voltage can be expressed as $V_p = I_P/\omega_p C_p$. The output of a PE transducer is alternating current (AC) and, thus, needs conversion to direct current (DC). The commonly used AC-DC converters are full-bridge rectifiers (FBRs) and voltage doubler rectifiers (VDRs). Both FBR and VDR deliver a similar maximum output power when ideal diodes are used [2]. The operation of an FBR is well understood, which

provides current for every half-cycle only after charging C_p to $\pm(V_{RECT} + 2V_D)$. Here, V_{RECT} is the rectified output voltage and V_D is the diode voltage drop. The VDR provides current to the output only during the positive half-cycle. In the negative half-cycle, a diode in parallel with the PE transducer provides a path to discharge C_p to the ground. During the positive half-cycle, I_P only needs to charge C_p from $-V_D$ to $(V_{RECT} + V_D)$ before current can flow into the output.

In the rectifier, a commonly used figure-of-merit is the power transfer efficiency, which is defined as the ratio of the output power P_{OUT} to the input power P_{IN}, which can be delivered by the PE transducer. Rectifying a low voltage from a PE transducer may induce significant power losses due to the diode voltage drop. An effective way to increase the efficiency of the rectifier is (1) reducing the diode's voltage drop; and (2) increasing the input voltage by implementing the bias-flip strategy.

Figure 1 shows several reported techniques for improving the efficiency [2–6]. The switch-only rectifier is introduced to reduce the power to charge C_p (not delivered to output) during the negative cycle of the VDR. In this approach, a switch M_1 is shunted across the PE transducer, as shown in Figure 1a. The purpose of this switch is to discharge C_p instantaneously when I_P crosses zero. Since the switch is on at the zero crossing, the initial voltage to charge C_p starts from 0 rather than $-V_D$. This modification reduces the charge which is not delivered to the output and increases the extracted power.
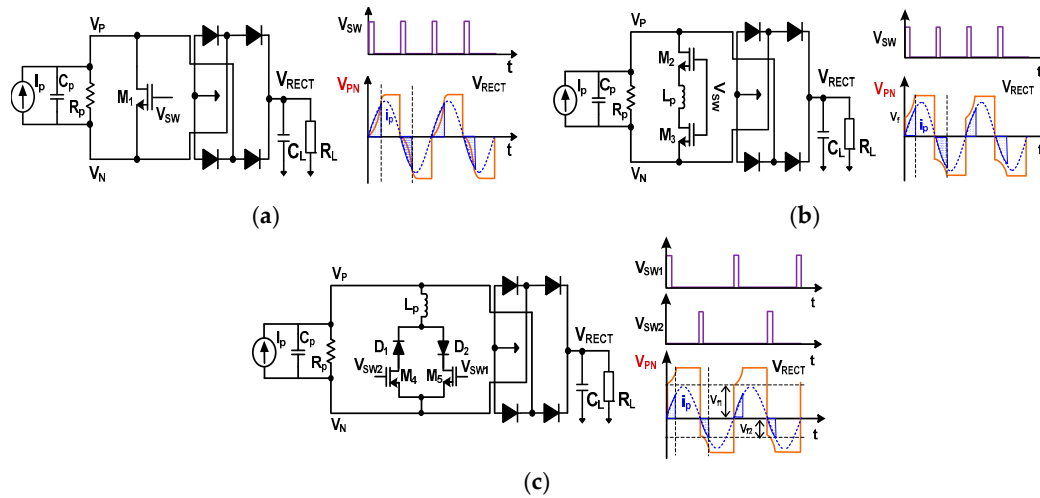

Figure 1. Schematics of the rectifiers for piezoelectric energy harvesting utilizing (**a**) switch-only; (**b**) bias-flip using an inductor; and (**c**) bias-flip using two switches and diodes with an inductor. The output load includes C_L and R_L.

During the period when C_p is charged, however, there is still a large portion of I_P that is not delivered to the output. The highlighted portion of I_P, shown in Figure 1a, indicates the portion of I_P, which is used to charge C_p from 0 to $\pm(V_{RECT} + 2V_D)$. To reduce the charge, the work in [2] introduces a bias-flip technique, shown in Figure 1b. An inductor L_P is shunted across the PE transducer through the switches realized with M_2 and M_3. When I_P crosses zero, the pulse signal V_{SW} briefly turns M_2 and M_3 on. At this time, the resonant loop formed by C_p and L_P flips the voltage, $V_{PN} = V_P - V_N$ across the transducer. Then, the charging starts from the flip-voltage V_f rather than from 0 V. Since flipping reduces the amount needed to charge C_p from 0 to V_f, this technique increases the extracted power. However, we note that there exists power loss from the voltage drop of the two switches. In addition, the body diode of switches may be conducting for a large V_{PN} (This observation also applies to M_1 in Figure 1a. To reduce the voltage drop, current paths for positive and negative cycles are split [4–6]. Sharing a single inductor L_P as shown in Figure 1c, this approach provides two branches for the bias-flip using two diodes and two shunt switches. The transducer voltage is flipped alternatively through two paths. Then, the voltage drop by the switch is reduced from two to one, but with an additional diode voltage drop. The drawback of this approach is that the two bias-flip voltages, V_{f1}

and V_{f2} for positive and negative cycles, respectively, are different, i.e., $V_{f1} \neq V_{f2}$. This is because the impedance at V_P and V_N seen from the flipping path is different, and we observe asymmetric flipping in the waveform. The asymmetry results in fluctuation of the extracted power and increased output ripple.

The diode voltage drop V_D existing in the rectifier loop is the third reason for the low efficiency. The V_D drop can be reduced by adding a bias voltage between the gate and drain terminal of a transistor [7]. To generate the bias voltages for a multi-stage rectifier, an extra bias distributor is required, which increases circuit complexity and the losses associated with it. In [3], an active diode, based on an op-amp with a pre-set DC offset, is used to reduce V_D and the leakage current. Another method to reduce V_D is by using a comparator-controlled switch [8]. This approach requires approximately one threshold voltage V_{TH} plus two overdrive voltages to power up, limiting the input voltage for start-up to 1.2 V using a 0.35 µm CMOS process. Usually, the comparator is powered up from the output storage capacitor. If there is not enough voltage to power up, the comparator will not be readily activated.

Herein, we propose two resonant rectifiers using low-voltage drop diode equivalents to overcome the limitations that exist in previous studies. We propose two diode equivalents, a minuscule-drop-diode equivalent (MDDE) and a low-drop-diode equivalent (LDDE), which effectively reduces the V_D of the rectifying stage. The diode equivalents are efficiently combined with a symmetric and low-loss resonant loop to realize the bias-flip technique. Harnessing MDDE and LDDE, two resonant rectifier integrated circuits (ICs) having self-startup capabilities are designed. To improve the efficiency under the self-power condition, the rectifier using MDDE includes synchronous bootstrap pulse generators (SBPGs). The SBPG provides boosted bias-flipping pulses that are synchronized with the frequency of the PE transducer. Two resonant rectifier ICs using both MDDE and LDDE, are fabricated in a 0.18 µm CMOS process. The rectifier using LDDE shows measured P_{OUT} of 564 µW under an external-powered condition with a corresponding efficiency of 68.1%. The rectifier using MDDE shows enhanced efficiency under the self-powered condition. It delivers a P_{OUT} of 288 µW with a corresponding efficiency of 78.4% and this result compares favorably with results from previous works.

2. Design

For an energy harvester, the capability for self-startup is one of the critical functions and several techniques have been reported [9–12]. In [9], the authors introduce a cold startup technique using a transformer. For high voltage boosting, this approach needs a transformer with a large turn ratio, which can increase the overall size of the harvester. In [10], the authors propose a mechanical switch that provides an instant power jerk to kick start the harvester. In [11], the authors present a low-voltage startup technique using a V_{TH}-tuned oscillator and a capacitor pass-on technique. Although a low startup voltage of 95 mV is achieved, the drawback is that this approach requires external programming of a body voltage after fabrication. In [12], a charge pump with a switched body-biasing technique is presented. Since the body terminal of a transistor is connected to a high voltage when it is turned off, the reverse leakage is effectively suppressed. In these previous works, except [11], the self-startup function, which is vital to autonomous operation, is not fully supported. In this work, we embed a simple, yet efficient, approach for self-startup into the two resonant rectifiers.

2.1. Resonant Rectifier Using LDDE

Figure 2a shows the block diagram of the resonant rectifier IC using LDDE. The rectifier consists of a three-stage voltage multiplier (VM), an oscillator (OSC), a bootstrap pulse generator (BPG), a symmetric bias-flip circuit, and a full-bridge rectifying stage. The BPG provides the bootstrapped pulse signals V_{SW1} and V_{SW2} for the bias-flip circuit. The clock (CLK) signal for the BPG is generated by the OSC with a frequency that can be tuned using a ring oscillator. The supply voltage of the OSC is driven by the output V_{VM} of the voltage multiplier shown in Figure 2b. For efficient operation, the

VM uses Schottky diodes (D_{V1}–D_{V6}) realized in a standard CMOS process, which shows a low V_D of 160 mV at 1 μA [13]. Since the VM and OSC are powered from the PE transducer, the rectifier provides the self-startup function.
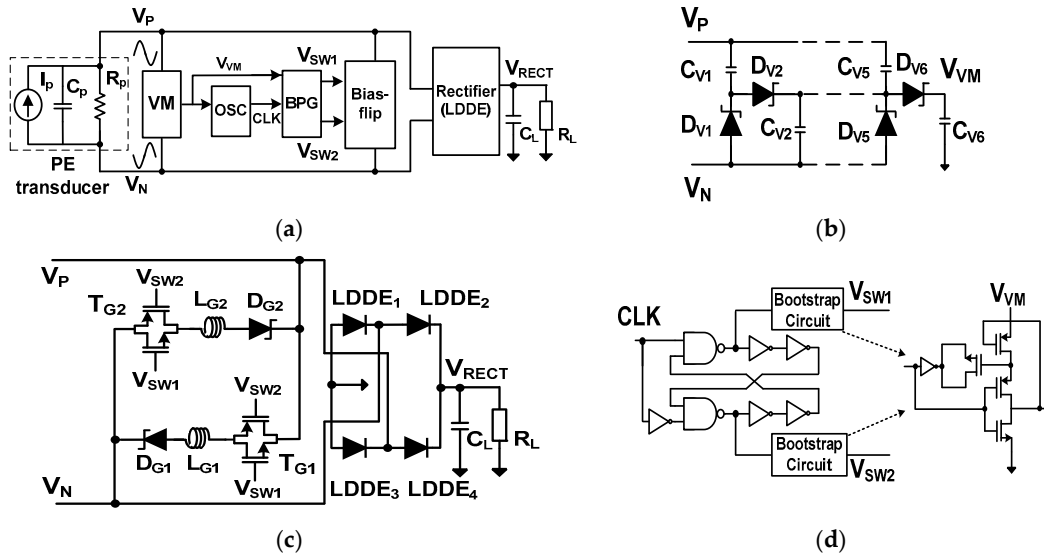

Figure 2. (**a**) Block diagram of the proposed resonant rectifier IC using LDDE; (**b**) voltage multiplier; (**c**) bootstrap pulse generator; and (**d**) the symmetric bias-flip circuit and rectifying stage using LDDEs.

Figure 2c shows the schematic of the BPG which generates V_{SW1} and V_{SW2}. The amplitudes of these signals are increased to almost $2V_{VM}$, which provide the high overdrive voltage needed to fully turn on the switches in the bias-flip circuit, shown in Figure 2d. The bias-flip circuit consists of Schottky diodes (D_{G1}, D_{G2}), inductors (L_{G1}, L_{G2}), and transmission (T)-gate transistors (T_{G1}, T_{G2}). The T-gate is used to reduce the on-resistance of the switch [14]. The size of NMOS and PMOS transistors in the T-gate are W/L = 1000 μm/0.2 μm and 2000 μm/0.18 μm, respectively, with values optimized by using a circuit simulator. When I_P crosses zero, the bias-flip circuit changes the polarity of V_{PN} using two separate paths. The positive cycle uses the path formed by T_{G1}, L_{G1}, and D_{G1}, while the path formed by T_{G2}, L_{G2}, and D_{G2} is used in the negative cycle. Inductors are bulky and expensive; the bias-flip circuit shown in Figure 2d is improved to use only one inductor (see Section 2.2).

Figure 3 shows a detailed schematic of the rectifying stage using four LDDEs. $LDDE_{1,3}$ are NMOS-based LDDEs and the $LDDE_{2,4}$ are PMOS-based LDDEs. When $V_P > V_N$, $LDDE_1$ and $LDDE_4$ conduct and form a closed loop. $LDDE_4$ consists of a main transmission transistor MP_1 and control circuit (MP_2, MN_1, and MN_2). The $LDDE_1$ consists of the main transistor MN_3 and control circuit (MN_4, MP_3, and MP_4). In a previous work [15], the control circuit for the LDDE is implemented using discrete bipolar junction transistors (BJTs). In this work, we remove the base current of the BJT using metal-oxide field effect transistors (MOSFETs) realized in IC technology. A voltage polarity sense circuit is formed by the diodes D_{S1}–D_{S4} and C_S. The circuit detects the positive ($V_P > V_N$) and negative ($V_P < V_N$) cycles using four terminal voltages, V_{R1}, V_{R2}, V_{C1}, and V_{C2}. Using the four voltages, the sense circuit controls the conduction of the main transistor while blocking reverse leakage current. The voltage at nodes V_{C1} and V_{C2} control the conduction of $LDDE_1$ and $LDDE_4$ in the positive cycle ($LDDE_2$ and $LDDE_3$ in the negative cycle), respectively. The voltage at nodes V_{R1} and V_{R2} blocks reverse conduction of $LDDE_4$ and $LDDE_1$ in the negative cycle ($LDDE_3$ and $LDDE_2$ in the positive cycle), respectively.

The operation of the LDDE is described using four states, shown in Figure 3b. When I_P crosses zero from negative to positive, D_{S2} and D_{S4} are forward-biased forming the conducting path $D_{S2} - C_S - D_{S4}$. The terminal voltages detected by the sense circuit satisfy the condition ($V_{C1} = V_P$) > ($V_{R2} = V_P - V_{D1}$)

> $(V_{R1} = V_N + V_{D1}) > (V_{C2} = V_N)$, where V_{D1} is the forward voltage drop of a diode in the sense circuit. We consider four operation states for LDDE$_4$ as follows.

(1) State-1: In the positive cycle when $V_P > V_N$, we have the condition of $(V_P = V_{C1}) > (V_{C2} = V_N)$. Terminal V_{C2} is connected to the negative terminal V_N of the PE transducer through MN$_2$. Then MP$_2$ turns on and subsequently turns on MN$_2$, as well. The C$_{SG}$ of MP$_1$ is charged by V_{PN}.

(2) State-2: The source and gate terminals of MP$_1$ are approximately V_P and $V_N + V_{DS,MN2}$, respectively. Here, $V_{DS,MN2}$ is the drain-source voltage of MN$_2$. The voltage at node V_P keeps increasing. Then, MP$_1$ begins conducting when $V_{SG} > |V_{TH}|$. The voltage across C$_{SG}$ of MP$_1$ keeps increasing and MP$_1$ enters the triode from the saturation mode. Using the rectifier operation, V_{RECT} increases. Then, the condition $(V_{PN} - V_{DS,MN2} - |V_{TH}|) > (V_P - V_{RECT})$ allows MP$_1$ to enter the triode mode, which can be written as $V_{RECT} > (V_N + |V_{TH}| + V_{DS,MN2})$.

(3) State-3: When the V_{SD} of MP$_1$ decreases by increasing V_{RECT}, it turns MP$_2$ off. When MP$_2$ is off, C$_{SG}$ of MP$_1$ stops charging and it maintains the V_{SG} of MP$_1$. This allows MP$_1$ to continue conducting in the triode mode. When MP$_2$ is off, the gate of MN$_2$ has no path to conduct and, therefore, MN$_2$ is kept on. This state is different from the BJT version of the LDDE [15]; the base current of a BJT provides a path to discharge while the MOSFET MN$_2$ is kept on.

(4) State-4: When i_p changes direction $(V_P < V_N)$, the current direction in the sense circuit is reversed. Then, the terminal voltages detected by the sense circuit satisfy the condition $(V_{C2} = V_N) > (V_{R1} = V_N - V_{D1}) > (V_{R2} = V_P + V_{D1}) > (V_{C1} = V_P)$. This condition turns on MN$_1$. By discharging the C_{GD} of MP$_1$, MN$_1$ subsequently turns off MP$_1$ to prevent reverse leakage. Since V_{C2} is positive and increasing, MN$_2$ is turned off, which prevents the discharging of V_{RECT} through MN$_1$.

In the case of $V_P < V_N$, LDDE$_2$ and LDDE$_3$ conduct. During the zero-crossing of I_P from positive to negative, D$_{S1}$ and D$_{S3}$ are forward-biased, forming the conduction path D$_{S3}$–C$_S$–D$_{S1}$. The operation of LDDE$_2$ and LDDE$_3$ follow four states in a manner similar to that described above. As other sensor-free bias-flip rectifiers, the frequency control method of the rectifier using LDDE is not adaptive to the f_p of PE transducer. If f_p changes by aging or other reasons, the bias-flip operation may not occur at the exact zero crossing of I_P. To handle this issue, a simple yet effective frequency tracking method is implemented in the rectifier using MDDE, as explained in the next section.
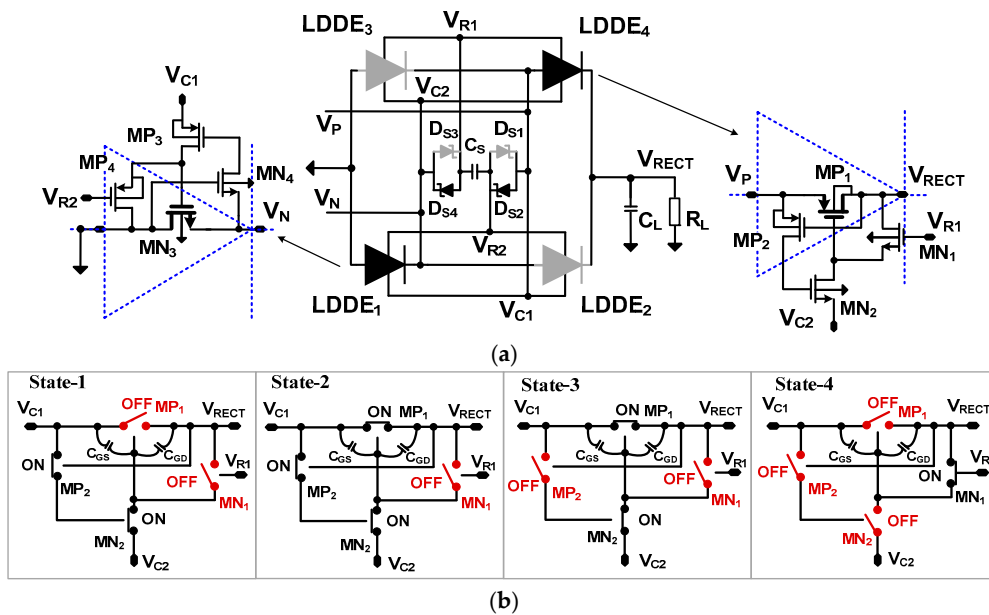

Figure 3. (**a**) Schematic of the rectifier loop using LDDEs; and (**b**) four operation states described using LDDE$_4$.

2.2. Resonant Rectifier Using MDDE

Figure 4a shows the block diagram of the resonant rectifier using MDDE. The rectifier IC includes two synchronous bootstrap pulse generators (SBPGs), dual voltage doublers, a symmetric bias-flip circuit, and a rectifying stage using MDDE. Instead of using VM and OSC for frequency generation, the pulse signals V_{SW1} and V_{SW2} for the bias-flip circuit are directly derived from the PE transducer. For efficient bias-flipping, the V_{SW1} and V_{SW2} are bootstrapped by the SBPG, which is driven by the output V_{DBL} from a voltage doubler. The dual voltage doublers are realized using the Schottky diodes D_{D1}–D_{D4}. Without an external power supply, the SBPG and doublers are driven by the PE transducer, realizing the self-startup function.

Figure 4b shows a schematic of the SBPG. The two SBPGs operate in a complementary manner, generating two opposite phase pulse signals, V_{SW1} and V_{SW2}. In the SBPG, V_P is compared with V_N and the output of the comparator $C_{MP1,2}$ drives the BPG. In this way, the voltages V_{SW1} and V_{SW2} for the bias-flip circuit are generated in sync with the f_p of the PE transducer. The comparator $C_{MP1,2}$ is realized using a differential amplifier with a latched load for increased gain. It achieves an open-loop gain of 35 dB by consuming 770 nA. Two diodes, D_{C1} and D_{C2}, are used to prevent reverse leakage current. By the BPG, the amplitudes of V_{SW1} and V_{SW2} are increased by about twice that of V_{DBL}, which effectively flips the voltage across the nodes V_P and V_N.
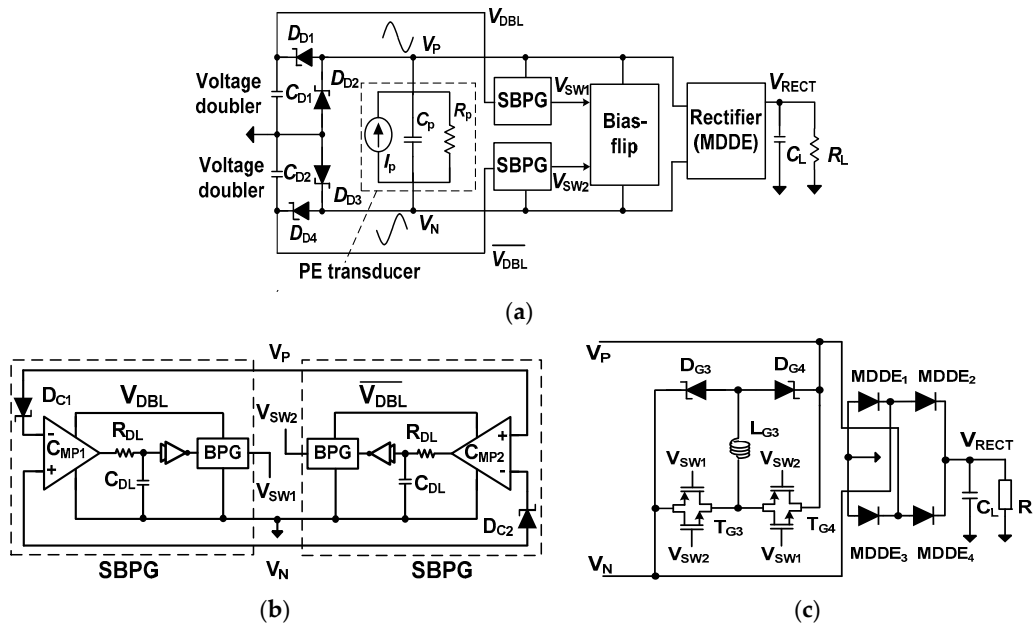

(**a**)

(**b**)

(**c**)

Figure 4. (**a**) Block diagram of the proposed resonant rectifier IC using MDDE; (**b**) synchronous bootstrap pulse generator; and (**c**) bias-flip circuit and rectifying stage using MDDE.

To compensate the time delay between $V_{SW1,2}$ and V_{PN}, a delay line consisting of R_{DL} and C_{DL} is added. This allows fine tuning of the delay, which aligns the pulses V_{SW1} and V_{SW2} with the zero crossing of I_P. Due to the power constraint for self-startup, the values of R_{DL} and C_{DL}, which depend on transducer parameters (R_L, I_P and f_P), are externally controlled (Table 1). We perform circuit simulations and the results show that the f_P from 100 to 800 Hz can be handled using this approach. The minimum delay determined by the comparator, a buffer, and BPG sets the 800 Hz as the maximum input frequency. Figure 4c shows the schematic of the bias-flip circuit and the rectifying stage using the MDDEs. To control the path for bias-flip, the Schottky diodes D_{G3} and D_{G4} are used. Using a single inductor L_{G3}, two separate and symmetric paths are created for the positive (a path along T_{G4}, L_{G3}, and D_{G3}) and negative (a path along T_{G3}, L_{G3} and D_{G4}) cycles. Compared to the bias-flip circuit for the rectifier using LDDE, the circuit for the MDDE is improved to use one shared inductor.

Table 1. Values of the delay line depending on R_L, I_P, and f_P.

f_p (Hz)		200			300			400	
R_L (KΩ)		100	50	20	100	50	20	100	50	20
R_{DL} (MΩ)/C_{DL} (nF)										
	200	8/1	8/1	10/1	8/1	8/1	8/1	8/1	8/1	8/1
I_P (μA)	300	10/1	14/1	12/1	8/1	4/1.5	4/1.5	5/0.5	5/0.5	5/0.5
	400	10/1	14/1	14/1	8/1	8/1	5/1	8/0.5	8/0.5	3/1.2
	600	16/1	16/1	14/1	8/1.5	8/1.5	7/1.5	8/1	8/1	5/1.2

Figure 5 shows the operation of the rectifying stage using MDDEs. The bridge-type stage consists of two PMOS and NMOS-based MDDEs. MDDE$_{2,4}$ are PMOS-based MDDEs, where TP$_2$ and TP$_4$ are the main transmission transistors. MDDE$_{1,3}$ are NMOS-based MDDEs, where TN$_1$ and TN$_3$ are the main transistors. The control circuit, which consists of a diode and a transistor in each MDDE, reduces the V_D of the main transistor via the deep-triode mode while blocking the reverse leakage current. In the positive cycle ($V_P > V_N$), MDDE$_2$ and MDDE$_3$ close the loop, as shown in Figure 5a. The diode D$_2$ is forward biased, which turns on N$_2$. At this time, the gate of TP$_2$ is connected to V_N through N$_2$, which turns on TP$_2$. Since V_N is negative, it also turns on P$_3$ and D$_3$. The V_{SG} of TP$_2$ is determined by the voltage at the gate ($V_N + V_{DS,N2}$) and source (V_{RECT}). With the condition ($V_{RECT} - V_N - V_{DS,N2}$) > |$V_{TH}$|, TP$_2$ is turned on. The V_{GS} of TN$_3$ is determined by the voltage at the gate ($V_P - V_{SD,P3}$) and source ($V_{RECT} - V_{D,RL}$), where $V_{SD,P3}$ and $V_{D,RL}$ are the source-drain voltage of P$_3$ and the voltage drop across R_L, respectively. With the condition ($V_P - V_{SD,P3} - V_{RECT} + V_{D,RL}$) > V_{TH}, the TN$_3$ connects between V_N and V_{RECT}, closing the loop.
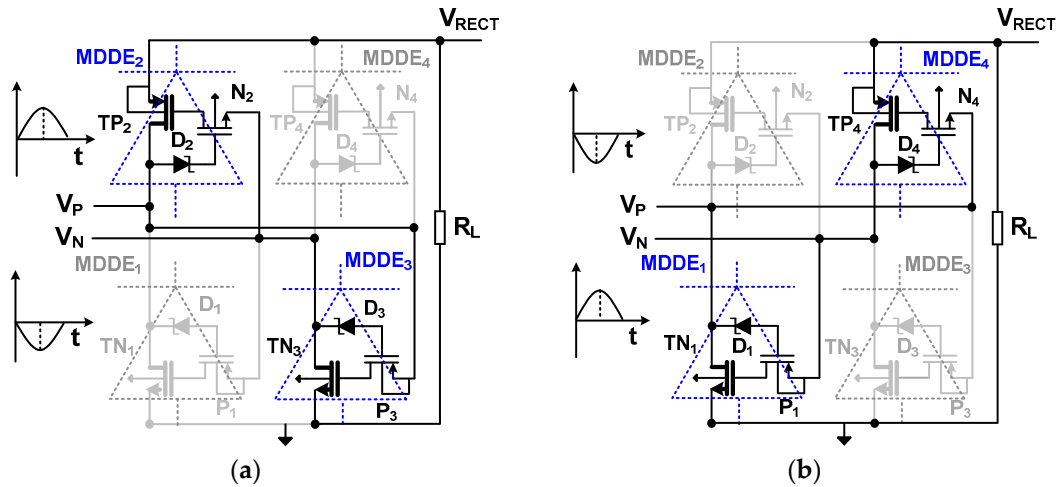
Figure 5. Schematic of the rectifier loop using MDDE and operation during (**a**) positive and (**b**) negative cycles.

Next, we find the condition for TP$_2$ and TN$_3$ to operate in triode mode. In TP$_2$, we observe that the source-drain voltage is $V_{RECT} - V_P$ and the source-gate voltage is $V_{RECT} - (V_N + V_{DS,N2})$. Therefore, the condition $V_{PN} \gg$ (|V_{TH}| + $V_{DS,N2}$) allows deep-triode operation of TP$_2$. For TN$_3$, we observe that the drain-source voltage is $V_N - (V_{RECT} - V_{D,RL})$ and the gate-source voltage is ($V_P - V_{SD,P3}) - (V_{RECT} - V_{D,RL}$). Then, the condition $V_{PN} \gg$ ($V_{TH} + V_{SD,P3}$) allows deep-triode mode operation for TN$_2$. In the negative cycle ($V_P < V_N$), D$_2$ and D$_3$ are reverse biased, and the voltage at the source terminal of N$_2$ is $V_N > 0$ (for P$_3$, it is $V_P < 0$). Therefore, both N$_2$ and P$_3$ are kept off and the reverse leakage through TP$_2$ and TN$_3$ is blocked. The operation of MDDE$_1$ and MDDE$_4$ in the negative cycle ($V_P < V_N$) can be similarly described, as shown in Figure 5b.

Figure 6 shows the comparison of V_D of the LDDE and MDDE as a function of I_P. The two R_L values and the size of the main transistor are chosen to match the result in [15]. Since the control circuit does not fully turn on with small I_P values, the results show that the V_D of both diode equivalents increases in the small I_P range from 20 to 40 µA. When I_P increases above 60 µA, V_D increases with I_P. The LDDE has a narrow window in the I_P range from 30 to 40 µA. In the case of MDDE, the V_D is below 50 mV in the I_P range from 30 to 60 µA. In order to investigate the performance for different PE transducer parameters, Figure 6b shows the comparison of V_D of the LDDE and MDDE for the different periphery. For a PE transducer having I_P = 600 µA, the V_D is 230 mV and 360 mV in case of MDDE and LDDE having the same size, respectively. The results show that the MDDE shows an overall smaller V_D than that of the LDDE over a broad range of I_P. The LDDE use three extra transistors to control the on-resistance of the main conducting transistor. In the case of the MDDE, the control is achieved using a transistor and a diode, which makes it simple, with a low loss.
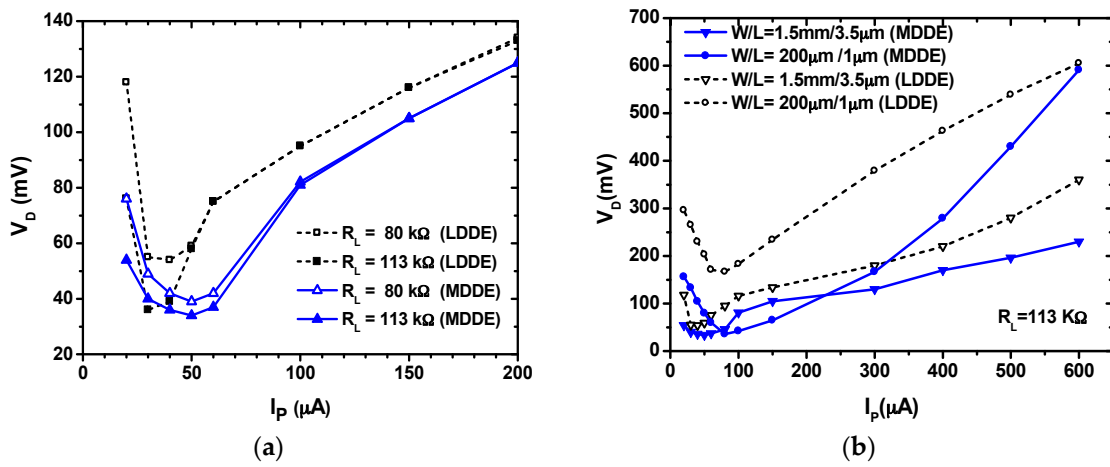

(a)   (b)

Figure 6. Comparison of the diode voltage drops as a function of I_P for (**a**) different loads; and (**b**) periphery (W/L).

2.3. Loss Calculation

Figure 7 shows the key waveforms of the resonant rectifier. When the PE element starts providing I_P, the rectifier enters a startup state. In this state, the BPG starts generating V_{SW1} and V_{SW2}, which have amplitudes that increase with V_{PN}. A steady-state is assumed after t_1. Just before time t_1, C_p is pre-recharged to $-(V_{RECT} + 2V_D)$. At time t_1, I_P changes direction and the bias-flip operation allows the charging of C_p from V_f to $(V_{RECT} + 2V_D)$ until t_2. During this period, the output current I_o starts flowing to the load. In the negative cycle, C_p is discharged from $-V_f$ to $-(V_{RECT} + 2V_D)$. The effectiveness of bias-flip is usually expressed using a flipping efficiency η_f, defined as:

$$\eta_f = \frac{V_f + V_{RECT}}{2V_{RECT}} \tag{1}$$

The amount of charge Q_{Cp} lost due to charging C_p during time interval $[t_1, t_2]$ can be expressed as:

$$Q_{Cp} = [V_{RECT} + 2V_D - V_f]C_p = [V_{RECT} + 2V_D - V_{RECT}(2\eta_f - 1)]C_p \tag{2}$$

Next, we consider the charge lost across R_p in the time interval $[t_1, t_\pi]$. Since V_{PN} varies during the time interval, we consider two cases of charge losses, Q_{Rp1} during $[t_1, t_2]$ and Q_{Rp2} during $[t_2, t_\pi]$, given by:

$$Q_{Rp} = Q_{Rp1} + Q_{Rp2} = \int_{t_1}^{t_2} \frac{V_{PN}(t)}{R_p}dt + \int_{t_2}^{t_\pi} \frac{V_{PN}(t)}{R_p}dt \tag{3}$$

During the time interval $[t_1, t_2]$, V_f is inverted via a bias-flip. In this period, $V_{PN}(t)$ can be obtained by integrating $I_P(t)$ as:

$$V_{PN}(t) = \frac{1}{C_p} \int_{t1}^{t} I_p \sin \omega t \, dt - V_f(t_1) = \frac{I_p}{\omega C_p}(\cos \omega t_1 - \cos \omega t) - V_f(t_1) \tag{4}$$

Applying the boundary conditions $V_f = V_{RECT}(2\eta_f - 1)$ and $\omega t_1 \cong 0$, Equation (4) can be expressed as:

$$V_{PN}(t) = V_p(1 - \cos \omega t) - V_{RECT}(2\eta_f - 1) \tag{5}$$

where $V_P = I_P/(\omega_p C_p)$ is the open-circuit voltage. Using Equation (5), Q_{Rp1} is obtained as:

$$Q_{Rp1} = \int_{t1}^{t2} \frac{V_p(1 - \cos \omega t) - V_{RECT}(2\eta_f - 1)}{R_p} dt \cong \frac{V_p}{\omega R_p}(\omega t_2 - \sin \omega t_2) - \frac{V_{RECT}}{\omega R_p}(2\eta_f - 1)\omega t_2 \tag{6}$$
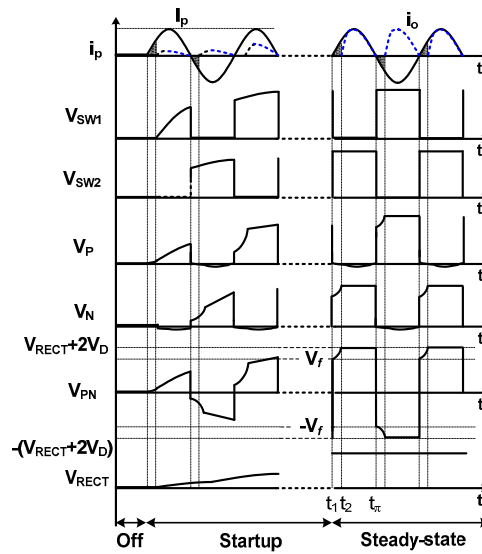

Figure 7. Key waveforms of the resonant rectifier.

To find Q_{Rp2} during the time interval $[t_2, t_\pi]$, we need the value of ωt_2 and, thus, use the following relationship:

$$I_p \sin \omega t = C_p \frac{dV_p}{dt} = \omega C_p \frac{dV_p}{d\omega t} \tag{7}$$

Integrating Equation (7) over the time interval $[t_1, t_2]$ when bias-flipping is performed, we obtain:

$$V_p(-\cos \omega t_2 + \cos \omega t_1) = V_p(t_2) - V_p(t_1) \tag{8}$$

The values of V_p can be obtained from the waveform, which are $V_p(t_1) = V_f$ and $V_p(t_2) = (V_{RECT} + 2V_D)$. Then, Equation (8) can be written as:

$$t_2 = \frac{1}{\omega} \cos^{-1}\left(\frac{V_p - 2V_{RECT} - 2V_D + V_{RECT}2\eta_f}{V_p}\right) \tag{9}$$

Using Equation (9), Q_{Rp2} is obtained as:

$$Q_{Rp2} = \frac{(V_{RECT} + 2V_D)}{R_p}(t_\pi - t_2) \tag{10}$$

where $t_\pi = \pi/\omega$.

The total charge produced by the PE transducer in every cycle is given by:

$$Q_{total} = 2I_p/\omega = 2C_p V_p \tag{11}$$

The theoretical extracted power $P_{\text{OUT,calc}}$ from the PE transducer for every cycle is obtained by taking the available charge Equation (11) minus the various loss terms given by Equations (2), (6) and (10):

$$\begin{aligned} P_{\text{OUT,calc}} &= 2f_p V_{RECT}(Q_{total} - Q_{Cp} - Q_{Rp1} - Q_{Rp2}) \\ &= 2f_p V_{RECT}\{[2V_p C_p - [V_{RECT} + 2V_D - V_{RECT}(2\eta_f - 1)]C_p - [\frac{V_p}{\omega R_p}(\omega t_2 - \sin \omega t_2) - \frac{V_{RECT}}{\omega R_p} \\ & (2\eta_f - 1)\omega t_2] - [\frac{V_{RECT}+2V_D}{R_p}(t_\pi - t_2)]\} \end{aligned} \tag{12}$$

3. Measured Results

The proposed rectifiers are fabricated in a one-poly six-metal 0.18 µm CMOS process with a top 2 µm thick metal option. Figure 8 shows the chip microphotographs. The size of the rectifiers using LDDE and MDDE are 0.26 mm × 0.19 mm and 0.51 mm × 0.46 mm, respectively. Figure 9 shows the experimental setup to characterize the rectifier using the PE transducer.

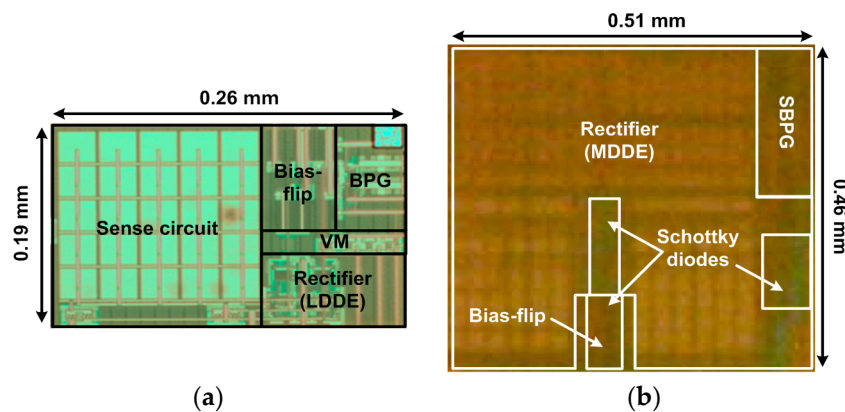**Figure 8.** Chip micrograph of the resonant rectifier ICs using (**a**) LDDE; and (**b**) MDDE.
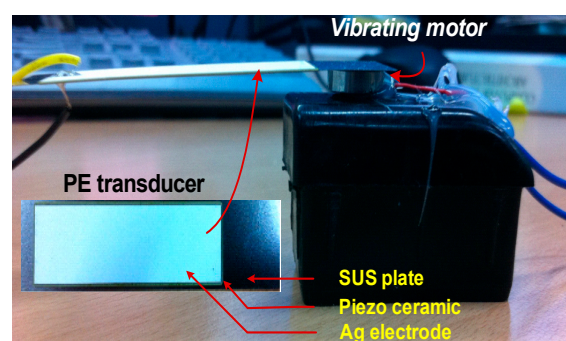

Figure 9. Experimental setup.

The bimorph of the transducer has a thickness, a length and a width of 0.33, 75, and 20 mm, respectively [16]. Each layer consists of a stainless steel (SUS) plate, a piezo ceramic, and an Ag electrode. The PE transducer is mounted on a vibrating motor for mechanical excitement [17]. The transducer is excited using 200 Hz with an acceleration of 1.8 g. Under this condition, the theoretical optimum loading resistance of the PE transducer is 7.2 kΩ. Two wires attached to both sides of the transducer are interfaced with a test board containing the rectifiers. Table 2 shows the

parameters used for the experiment. The value of the inductor for bias-flip is selected considering the trade-off between size and the Q-factor. The maximum current available from the transducer is 600 μA, which corresponds to V_p = 4.34 V at 200 Hz. The equivalent circuit of a PE transducer can be represented as a mechanical spring-mass coupled to an electrical circuit. The current in the primary mechanical side corresponds to proof mass relative velocity, which is determined by such parameters as PE material, dimension, and acceleration. By the electromechanical coupling factor, which describes the effectiveness of the conversion from mechanical to electrical energies, the maximum current is determined.

Table 2. Parameters for the experiment.

Parameters	Value
f_p	200 Hz
C_p	110 nF
R_p	1 MΩ
L_{G1}, L_{G2}, L_{G3}	1000 μH
C_L	1 μF
R_L	10–200 KΩ

Figure 10 shows the measured result of the rectifier using LDDE. It shows the input voltage V_{PN}, bootstrap pulse signals V_{SW1} and V_{SW2}, and the output V_{RECT}. The transient during self-startup is shown in the inset. When V_{PN} is increased, the BPG starts generating V_{SW1} and V_{SW2}. Then, V_{RECT} starts increasing and the steady-state condition is reached at about 20 s. After this time, V_{SW1} and V_{SW2} reach a value about twice that of the multiplier output and fully turn on the bias-flip circuit.
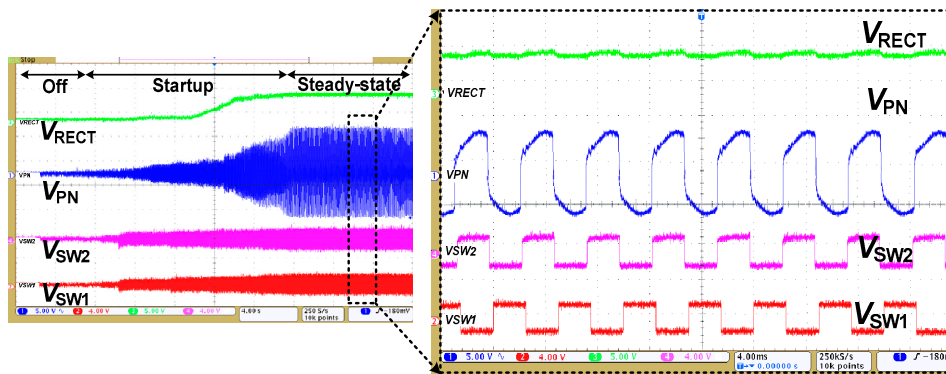

Figure 10. Measured waveforms of the resonant rectifier using LDDE.

Figure 11 shows the measured and calculated P_{OUT} and efficiency versus V_{RECT}. We characterize the rectifier under external and self-power conditions. When it is externally powered, the VM provides power only to the BPG and the internal oscillator is turned off. The CLK frequency is supplied externally to match the f_p of the PE transducer. By receiving the CLK, the BPG generates V_{SW1} and V_{SW2}. The V_{RECT} is measured with I_P = 600 μA. Since V_{RECT} depends on R_L, it is varied from 10 to 200 kΩ, searching for an optimum value. When V_{RECT} reaches 3.36 V, the measured peak P_{OUT} of 564 μW is achieved with an R_L of 20 kΩ. The $P_{OUT,calc}$ obtained using Equation (12) is 626 μW, which indicates that the power consumed by the control circuit is 62 μW. The maximum input power which can be delivered by the PE transducer is obtained as P_{IN} = 2 $C_p f_p (V_p)^2$ = 828 μW. Using the definition for power transfer efficiency = P_{OUT}/P_{IN}, we obtain 68.1%. Using the measured V_f of 1.53 V in Equation (1), a flipping efficiency η_f of 72.8% is achieved. Under the same PE input condition and with V_D = 0.7 V, the maximum power that can be obtained using the FBR [2] is 190 μW. The results show that the rectifier using LDDE delivers three times higher P_{OUT} than that of the FBR.
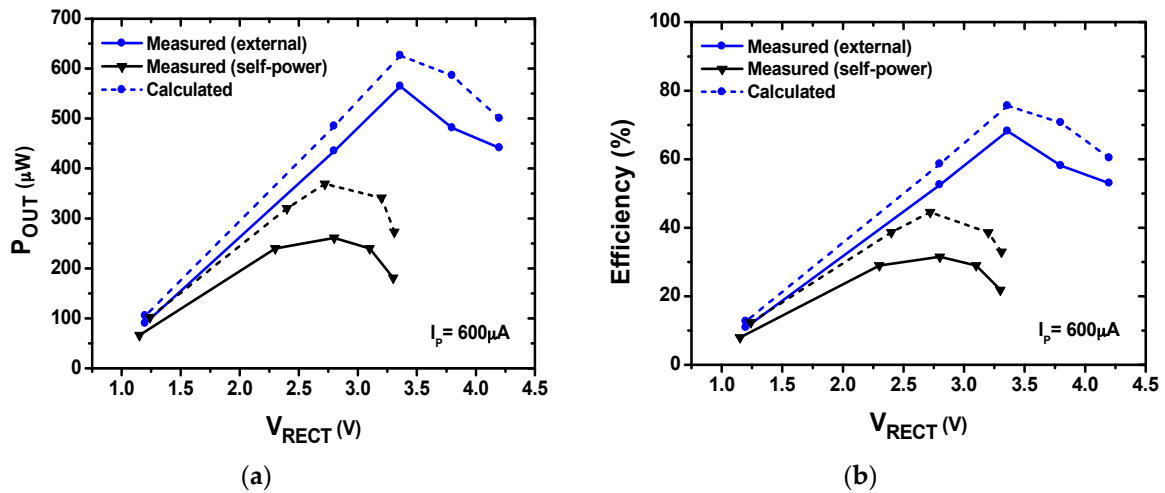
Figure 11. Performance of the rectifier using LDDE: (**a**) output power versus output voltage; and (**b**) power transfer efficiency versus output voltage.

Under the self-power condition, a resistive voltage divider is placed at the output of the VM. The role of the divider is controlling the supply voltage of OSC, which determines the CLK. The voltage divider is tuned so that the CLK frequency is closely matched to the f_p of PE transducer. The results show a P_{OUT} of 261 μW with a V_{RECT} of 2.8 V.

Figure 12 shows the measured waveform of the rectifier using MDDE. The result shows the initial transient waveform during self-startup. When V_{PN} starts increasing, the SBPG generates pulses for the bias-flip. After the steady-state condition is reached at about 2 s, V_{PN} flips abruptly. Figure 13 shows the measured and calculated P_{OUT} and efficiency versus V_{RECT} for two cases: I_P = 600 μA and 400 μA. The rectifier is characterized by varying R_L from 10 to 200 kΩ to find an optimum condition. Using I_P = 400 μA, a peak P_{OUT} of 288 μW and a V_{RECT} of 2.4 V are extracted with an R_L of 20 kΩ, which corresponds to an efficiency of 78.4%. The $P_{OUT,calc}$ obtained using Equation (12) is 386 μW, which indicates that the additional loss and control power is 98 μW. Since P_{OUT} depends on the PE transducer characteristics and the mechanical vibration [18,19], it is difficult to directly compare P_{OUT} performance (See Table 3). However, the conventional FBR can be used as a common reference. Under the same conditions, the maximum power that can be obtained using the FBR is 48.8 μW. The results show that the rectifier using MDDE delivers 5.9 times higher P_{OUT} than that of the FBR. Using I_P = 600 μA, a P_{OUT} of 441 μW is extracted with a V_{RECT} of 2.1 V using an R_L of 10 kΩ. The result shows that efficiency is reduced when I_P is increased from 400 to 600 μA. This is related to the narrow working window where V_D is increased with I_P (See Figure 6).
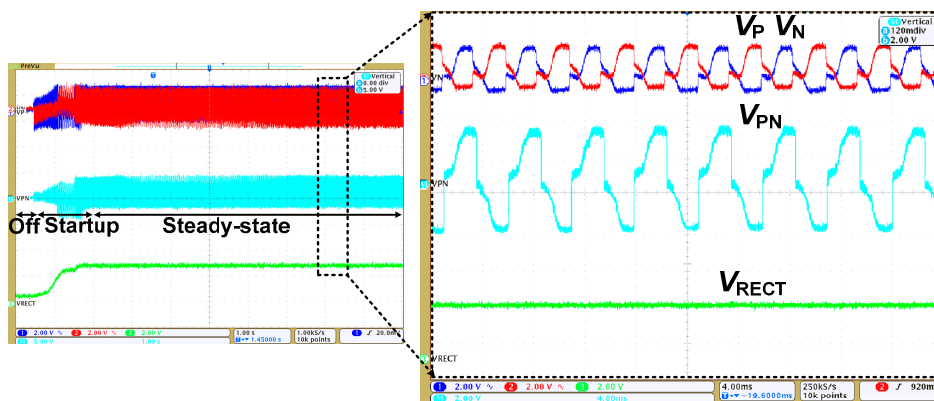

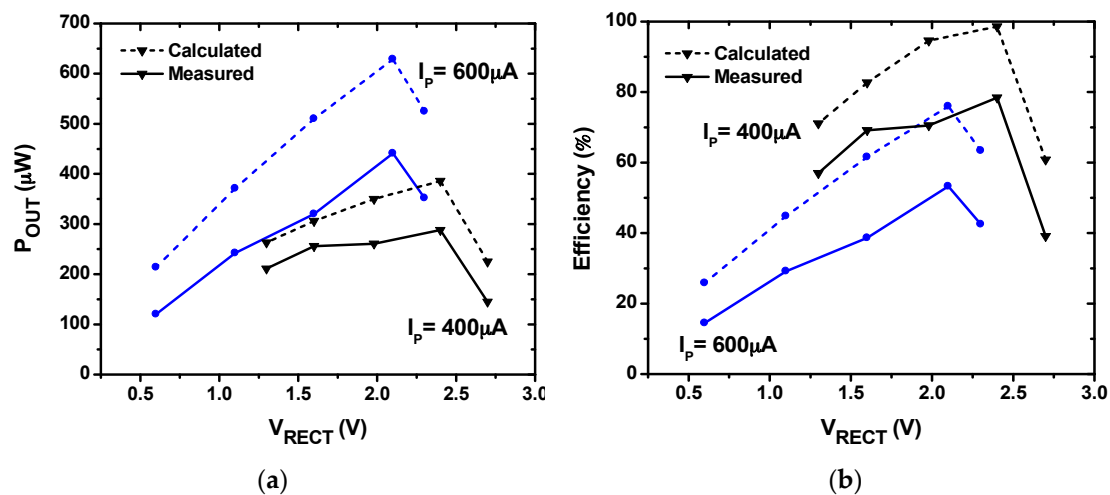**Figure 12.** Measured waveforms of the resonant rectifier using MDDE.

Figure 13. Performance of the rectifier using MDDE for two I_P values: (**a**) output power versus output voltage; and (**b**) power transfer efficiency versus output voltage.

Table 3 shows a performance comparison with previous works realized using IC technology. The work in [2] presents a resonant rectifier using the bias-flip technique. The bias-flip timing is controlled by a digital inverter delay line that can be programmed externally. Although the adjustable delay control provides flexibility to accommodate various PE transducers, self-startup is not supported. Further, the efficiency of 58% is rather low, which can be attributed to the voltage drop in bias-flip switches and rectifying stages. In [4], a passive differentiator is used to detect the I_P polarity change. In this work, two separate paths are used to reduce the voltage drop for bias-flip. A relatively high P_{OUT} of 1230 μW is achieved under externally-powered conditions. The work in [6] proposes a parallel synchronized switch harvesting on inductor (P-SSHI) technique which extracts 48 μW. The result in [20] shows a high efficiency of 91%. Including [20], however, the results in [4,6] are based on discrete realization and not included for comparison.

Table 3. Performance comparison with previous works.

	This Work		[2]	[3]	[21]	[22]	[23]	[24]
	Rectifier (MDDE)	Rectifier (LDDE)						
Tech.	0.18 μm		0.35 μm	0.18 μm	0.18 μm	0.35 μm	0.35 μm	0.25 μm
Type	Bias-flip/diode equivalent		Bias-flip	Active FBR	S-SSHI	Energy Invest	Inductor-less	SSHI
V_P (V)	2.89	4.34	2.8	2.8	2.2	2.6	2.5	4.9
f_0 (Hz)	200		225	200	200	143	82	144
PE transducer	Thrive K7520BP2		V22B Mide	Circuit model	Circuit model	V22B Mide	V22W Mide	V22B Mide
Self-power	Y	N	N	N	Y	N	N	Y
V_{RECT} (V)	2.4	3.36	3.2	2.78	3.6	3.7	1.0	3.9
P_{OUT} (μW)	288	564	53	81	74	52	35	136
Efficiency (%)	78.4	68.1	58	90	89.5	69	77	85

The work in [21] presents a series synchronized switch harvesting on inductor (S-SSHI) technique, which is applied to the conventional FBR. It shows a good efficiency of 89.5%. However, the results in [3,21] are obtained using an equivalent model of the PE transducer, therefore, its performance in a real environment is unknown. The work in [22] increases power extraction by investing energy from the battery to enhance the electromechanical coupling factor. The work in [23] presents a fully-integrated interface to a PE transducer which does not employ an inductor. By dynamically switching between parallel and series configurations of two PE transducers, this work achieves a peak efficiency of

77%. The work in [24] inserts an active diode in the resonant loop of the SSHI circuit which allows bias-flipping to occur at an optimal time without the need for complicated delay-tuning circuits. In the proposed rectifier using LDDE, we achieve an efficiency of 68.1% under the external-power condition. Under the self-power condition, the rectifier using MDDE delivers a P_{OUT} of 288 μW and a V_{RECT} of 2.4 V. This corresponds to an efficiency of 78.4%. Although this efficiency number is lower than the results of [24], a P_{OUT} of 441 μW is extracted using I_P = 600 μA, demonstrating the high power extraction capability of the proposed work. The results indicate the improvement is achieved using efficient bias-flipping with a low V_D of the MDDE.

4. Conclusions

In this work, we presented an efficient rectifier design technique for PE energy harvesting. To reduce the voltage drop in the rectifier, two diode equivalents are proposed. The diode equivalents are successfully embedded in two resonant rectifiers using the symmetric bias-flip technique. In addition, time synchronization of the bias-flip with the PE transducer is studied. Further, we propose a self-power boosted pulse generator that synchronously detects the zero crossing transition of the PE transducer. The measured results show that the proposed rectifiers significantly increase the extracted power and efficiency. The rectifier using LDDE delivers a P_{OUT} of 564 μW with a corresponding efficiency of 68.2%. The rectifier using MDDE delivers a P_{OUT} of 288 μW with a peak efficiency of 78.4%. Compared to the conventional FBR, these results show that the rectifier using MDDE and LDDE achieves a power extraction capability enhanced by factors of 5.9 and three times, respectively. The results indicate that an improvement is achieved with the proposed diode equivalents. This result can play a valuable role in various sensing applications that demand energy harvesting to obtain auxiliary power for extended battery lifetime.

Author Contributions: Amad Ud Din designed the resonant rectifiers and setup, performed the experimental work, and wrote the manuscript. Seneke Chamith Chandrathna supplied input to the rectifier operation and performed simulations. Jong-Wook Lee conceived the project, organized the paper content, and edited the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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