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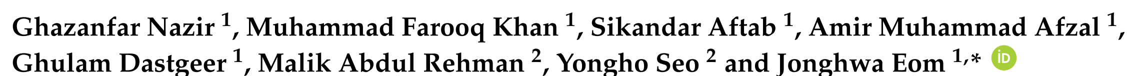
Gate Tunable Transport in Graphene/MoS_2/(Cr/Au) Vertical Field-Effect Transistors



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Received: 11 November 2017; Accepted: 22 December 2017; Published: 28 December 2017

Abstract: Two-dimensional materials based vertical field-effect transistors have been widely studied due to their useful applications in industry. In the present study, we fabricate graphene/MoS_2/(Cr/Au) vertical transistor based on the mechanical exfoliation and dry transfer method. Since the bottom electrode was made of monolayer graphene (Gr), the electrical transport in our Gr/MoS_2/(Cr/Au) vertical transistors can be significantly modified by using back-gate voltage. Schottky barrier height at the interface between Gr and MoS_2 can be modified by back-gate voltage and the current bias. Vertical resistance (R_{vert}) of a Gr/MoS_2/(Cr/Au) transistor is compared with planar resistance (R_{planar}) of a conventional lateral MoS_2 field-effect transistor. We have also studied electrical properties for various thicknesses of MoS_2 channels in both vertical and lateral transistors. As the thickness of MoS_2 increases, R_{vert} increases, but R_{planar} decreases. The increase of R_{vert} in the thicker MoS_2 film is attributed to the interlayer resistance in the vertical direction. However, R_{planar} shows a lower value for a thicker MoS_2 film because of an excess of charge carriers available in upper layers connected directly to source/drain contacts that limits the conduction through layers closed to source/drain electrodes. Hence, interlayer resistance associated with these layers contributes to planer resistance in contrast to vertical devices in which all layers contribute interlayer resistance.

Keywords: vertical transport; transition metal dichalcogenides; MoS_2; graphene

1. Introduction

Heterostructures [1–3] composed of graphene and other two-dimensional (2D) crystals, such as transition metal dichalcogenides (TMDs), are of a great interest due to their fundamental and applied aspects. Extensive research has been carried out in both lateral [4–6] and vertical [3,7–11] hetero-stacks of graphene with other two-dimensional materials. The vertical devices of two-dimensional materials open particularly promising new horizons in material research. For example, graphene vertical field-effect transistors (G-VFETs) are charming candidates for future research, as they have ultimately thin bodies of a few atomic layers, which provide ultrafast transport nearly in a few femtoseconds [12] and higher switching (on/off) ratio as compared to their lateral counterparts.

Thus far, several vertical heterostructures of graphene with other 2D materials have been proposed. For example, Britnell et al. introduced a VFET heterostructure [13] composed of two graphene electrodes and a thin hexagonal boron nitride (h-BN) layer sandwiched between them showing the on/off ratio ~50. When h-BN was replaced by MoS_2, on/off ratio was enhanced to ~10^4 due to the low bandgap of MoS_2 as compared to h-BN. It was reported that tunneling transport was dominant in off-state, whereas thermionic transport played a major role in on-state in other previous studies on

Gr/TMDs/Gr vertical devices [3]. Another configuration of VFETs has been investigated in which one side of TMDs was contacted with a graphene electrode, while the other was contacted with a metal electrode [7,14–21]. In this kind of devices (Gr/TMDs/Metal), Schottky barriers at the interface between graphene and TMDs play an important role in the electrical transport. Electric field from the back-gate can modify the Schottky barrier height. These devices are superior to tunneling devices due to a large current density through the semiconducting TMDs channel [22–24]. Gr/TMDs/Metal devices showed a high on/off ratio and low driving voltage; therefore, they are good to use in low power consumption applications.

In previous reports, most VFETs were studied by employing the two-probe measurement configuration, which included contact electrodes as a part of the devices. This configuration always possesses contact resistance due to which intrinsic characteristics of the device were impossible to achieve. In the present paper, we have fabricated Gr/MoS_2/(Cr/Au) VFET with various MoS_2 thickness. However, we use four-probe cross-bar geometry in this experiment to exclude contribution of electrode to the measurement. Monolayer Gr used as a bottom electrode allows back-gate electric field to tune the energy states of MoS_2 in VFET. Therefore, we could investigate the gate-dependent electrical transport in our MoS_2 VFET. Moreover, graphene contacts [25–28] can effectively decrease contact resistance because of small work function mismatch between graphene and MoS_2. We have also measured planar transport properties of lateral MoS_2 field-effect transistors for comparison. Electronic transports in the vertical and lateral direction were discussed by analyzing the resistance components.

2. Experimental Section

2.1. Device Fabrication

Our Gr/MoS_2/(Cr/Au) VFETs were fabricated on SiO_2/P^+-Si substrate. The thickness of dielectric (SiO_2) was 300 nm, whereas P^+-Si was used to apply back-gate voltage. In the first process, chemical vapor deposition (CVD) grown graphene was transferred on SiO_2/Si substrate using wet transfer method [29], and a graphene Hall bar pattern was defined by using photo-lithography. Then oxygen plasma (power ~50 W) was used for several minutes to etch extraneous graphene. The Raman spectrum for Gr is shown in Supplementary Materials Figure S1 (see Supplementary Materials). In Raman spectrum, 2D to G peak intensity ratio is larger than 3:1, indicating monolayer characteristics of Gr [30]. We used the scotch-tape method for mechanical exfoliation of MoS_2 [17,31–45]. The suitable MoS_2 flake was selected under an optical microscope and then transferred on graphene Hall bar by using micromanipulator. Subsequently, 15-nm-thick HfO_2 films was grown by atomic layer deposition on the e-beam lithography defined area. In the last process, e-beam lithography was done to define the top electrode of Cr/Au (8/120 nm).

2.2. Measurements

Electrical measurements were performed by using Keithley 2400 source meter, Keithley 6485K picoammeter, and Keithley 2182A nanovoltmeter. All measurements were performed in vacuum at room temperature. Structural investigation and material identification were performed using Raman spectroscopy and atomic force microscopy (AFM). In Raman spectroscopy, laser wavelength of 514 nm with power below 1 mW was selected to avoid structural degradation caused by the heating effects of the laser. The nominal diameter of laser spot was 0.7 μm.

3. Results and Discussion

3.1. Gr/MoS_2/(Cr/Au) Vertical Field-Effect Transistor

A schematic representation of Gr/MoS_2/(Cr/Au) VFET is shown in Figure 1a, where the back-gate voltage is applied to control the vertical transport in MoS_2 channel. The optical micrograph of device is shown in Figure 1b. Graphene is represented by the purple color, MoS_2 by the sky blue, and HfO_2

(~15 nm thick) window by the dark blue color. We choose CVD-grown monolayer graphene despite multilayer graphene. We believe that, in case of multilayer graphene, the gate effect would be small as compared to monolayer graphene due to back-gate electric field screening, and modulation in Schottky barrier height will be more difficult as compared to monolayer graphene.

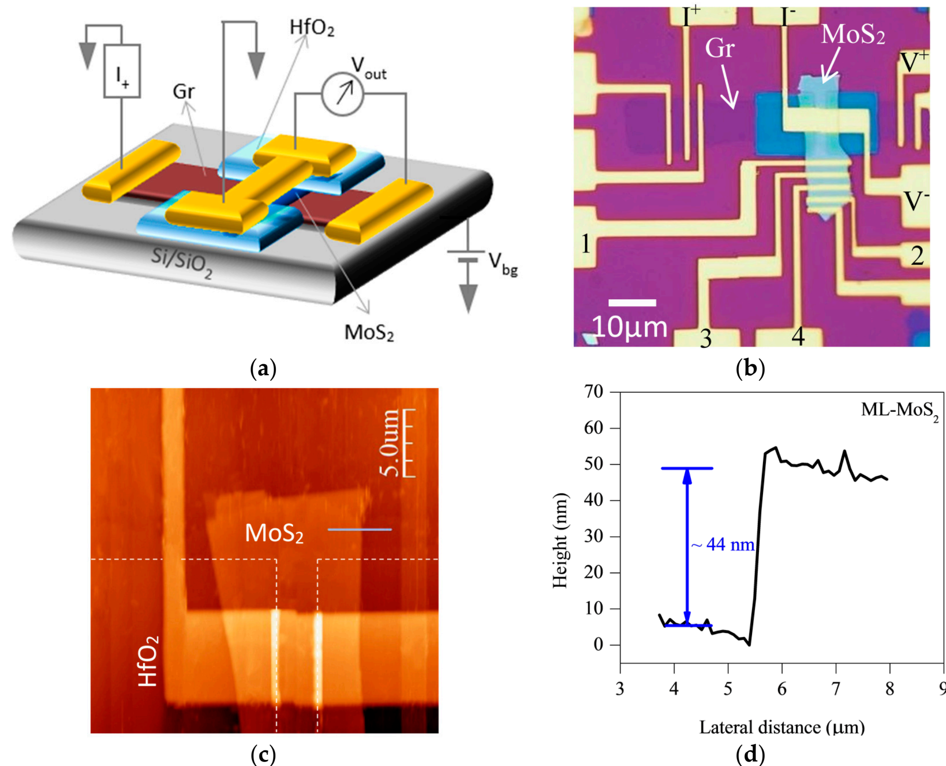

Figure 1. (**a**) Schematic representation of Gr/MoS_2/(Cr/Au) vertical field-effect transistor (VFET) (**b**) Optical image of Gr/MoS_2/(Cr/Au) VFET. Two HfO_2 windows on top of Gr/MoS_2 layer define the junction region. Different contacts with alphabetic and numeric letters were used to measure R_{vert} and R_{planer}, respectively (**c**) Atomic force microscope image that clearly reveals multilayer MoS_2 (ML-MoS_2) flake with top Cr/Au contact. HfO_2 windows are highlighted by dashed lines. (**d**) Height profile of ML-MoS_2 shows the thickness of nearly 44 nm.

The alphabetic and numeric symbols indicate different contacts used for the planar and vertical transport measurement. Figure 1c shows AFM of MoS_2 film, which reveals uniform surface morphology. Height profile taken by AFM shows the thickness of MoS_2 to be ~44 nm in Figure 1d.

Raman spectroscopy of MoS_2 on monolayer Gr was studied in comparison with MoS_2 on Si/SiO_2 substrate shown in Supplementary Materials Figure S2. Raman spectrum for MoS_2 on Si/SiO_2 substrate was represented by the black color, whereas the red color shows Raman spectrum of MoS_2 on Gr. Two prominent peaks of MoS_2 appeared in the wavenumber range from 380 to 420 cm^{-1}. These two Raman peaks belongs to in-plane (E^1_{2g}) and out of plane (A_{1g}) vibrations of "Mo" and "S" atoms [46]. The difference between E^1_{2g} and A_{1g} Raman peaks for MoS_2 on Si/SiO_2 substrate amounted to $\Delta \approx 24$ cm^{-1}, indicating a multilayer nature [22]. There was a slight change in peak positions of MoS_2 when stacked on Gr. This slight change was due to the relaxation of atoms on different substrate.

We assume that vertical resistance (R_{vert}) is a cumulative effect of all the resistances including contact resistance and MoS_2 channel resistance. We made a cross-junction geometry to investigate the vertical transport in Gr/MoS_2/(Cr/Au). The measurements consisted of four-probe technique where two contacts were used as source and drain, while the other two for voltage measurement across VFET. Figure 1b shows the measurement configuration (I^+, I^-, V^+, V^-) for the vertical resistance R_{vert}.

We also measured planar resistance R_{planar} of the same MoS_2 film using Cr/Au contacts as illustrated by numeric symbols 1, 2, 3, 4 in Figure 1b.

3.2. Vertical Resistance of Gr/MoS_2/(Cr/Au) VFET

Figure 2a shows a schematic diagram of Gr/MoS_2/(Cr/Au) VFET, where R_{int} and R_c represent interlayer resistance between stacked layer of MoS_2 and contact resistance, respectively. Figure 2b represents vertical resistance (R_{vert}) of Gr/MoS_2/(Cr/Au) VFET as a function of the back-gate voltage (V_{bg}). In this experiment, the current flows from Gr to the top Cr/Au contact through semiconducting MoS_2 channel. The electrical characteristics are strongly modified by V_{bg}. To understand the physics of the transport mechanism, there are lot of factors that should be keep in mind e.g., Schottky barrier height, barrier width etc. It is a well-known concept that electrical transport in TMD's based field effect transistors (FET) is governed by either tunneling or thermionic emission. Tunneling is due to passing of carriers through barrier height and is a temperature-independent quantity. However, thermionic emission is highly reliant on temperature. Tunneling current depends upon barrier width, and if the barrier width is too large, we cannot observe tunneling current. Here, our average MoS_2 thickness is 50 nm (barrier width ~50 nm). Usually, to observe tunneling mechanism, the barrier width should be $\leq$5 nm [47]. So, we can firmly say that in our experiment, electrical transport is not caused by tunneling. However, the low value of current observed at $V_{bg} < 0$ in our Gr/MoS_2 heterostructure's transport property (shown in Supplementary Materials Figure S3c) is due to gate leakage current and not by the tunneling that is a very well-known phenomenon in Si-based field effect transistors. The Gr/MoS_2 junction is completely in off state at low V_{bg} due to the presence of large Schottky barrier height (SBH), which is why we observed large resistance at that point.

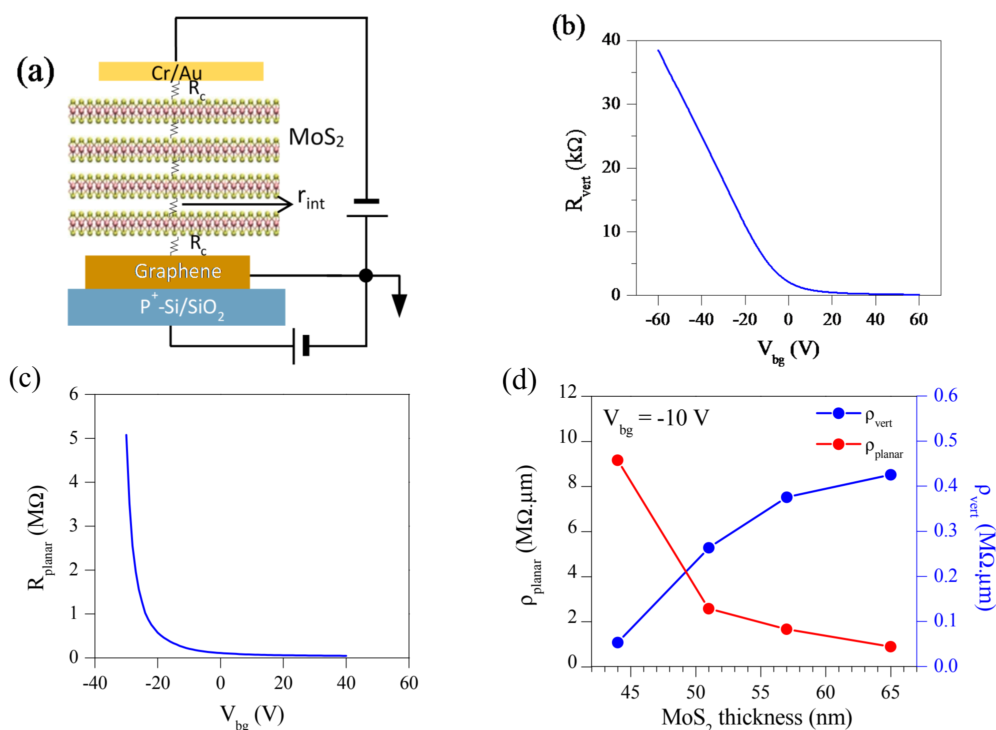

Figure 2. (**a**) Schematic diagram for resistances to compose Gr/MoS_2/(Cr/Au) vertical field-effect transistor (VFET) with 50 nm-thick MoS_2. (**b**) Vertical Resistance (R_{vert}) as a function of the back-gate voltage (V_{bg}) for Gr/MoS_2/(Cr/Au) VFET with 50 nm-thick MoS_2. (**c**) Planar resistance (R_{planar}) as a function of V_{bg} for the lateral MoS_2 field-effect transistor with 48 nm-thick MoS_2. (**d**) Dependence of ρ_{planar} and ρ_{vert} on the thickness of MoS_2 channels at $V_{bg} = -10$ V.

On the other hand, Deshun Qu et al. reported that "S" vacancies in MoS_2 play an important role in r_{int} [48]. The importance of "S" atoms was further elaborated for the vertical carrier transport by orbital overlapping between "S" atoms in adjacent layers [49,50].

3.3. Resistance Analysis of Gr/MoS_2/(Cr/Au) VFET

R_{vert} in the measurement configuration of Figure 2a can be considered as the sum of interface resistance between Gr and MoS_2 (R_{Gr/MoS_2}), total channel resistance of individual layers of MoS_2 ($R_{TCR\text{-}V}$), interlayer resistance (R_{int}) of MoS_2, and interface resistance (R_{SBH}) between Cr/Au electrode and MoS_2. So, the vertical resistance (R_{vert}) is given by Equation (1).

$$R_{vert} = R_{TCR\text{-}V} + R_{int} + R_{GR/MoS_2} + R_{SBH} \quad (1)$$

where total interlayer resistance (R_{int}) is given by $R_{int} = Nr_{int}$, where N is the total number of layers in MoS_2 and r_{int} is the interlayer resistance between two consecutive layers of MoS_2. As the thickness of MoS_2 increases, R_{int} increases, and then R_{vert} increases as well. In the vertical transport, r_{int} is a non-negligible quantity in the thick MoS_2 channel. Another important factor that should be elaborated here is the channel resistance itself. In the vertical transport, $R_{TCR\text{-}V}$ increases with an increase of the thickness of MoS_2 channel. Since both R_{int} and $R_{TCR\text{-}V}$ increase with increasing MoS_2 thickness, R_{vert} shows the dependence of MoS_2 thickness. However, the resistance of planar or vertical device depends on cross-sectional area, so it is better to examine resistivity instead of resistance. Figure 2d shows ρ_{planar} and ρ_{vert} as a function of MoS_2 thickness.

As another important component of R_{vert}, we discuss R_{Gr/MoS_2} which is the interface resistance between Gr and MoS_2. We analyze R_{Gr/MoS_2} within 2D thermionic emission theory, where the Schottky barrier height is given by Equation (2).

$$\Phi_B = \frac{k_B T}{e} \ln\left(\frac{A^* T^2}{J_{rev}}\right) \quad (2)$$

where k_B is the Boltzmann's constant, A^* is effective Richardson constant and we choose $A^* = 54$ Acm^{-2} K^{-2} for MoS_2 [51]. We extracted Schottky barrier height at T = 300 K from I_{ds}-V_{ds} curves shown in Supplementary Materials Figure S3. J_{rev} (=I_{ds}/A_{junc}) is the reverse saturation current density at $V_{ds} = -0.5$ V, where we see a beginning of saturation of I_{ds}. A_{junc} (=200 μm^2) is the junction area of Gr/MoS_2. Barrier height decreases with an increase of V_{ds} or V_{bg} (see Figure 3a,b). Φ_B ranges from 1.10 to 0.78 eV for the interface between monolayer Gr and 53-nm-thick ML-MoS_2.

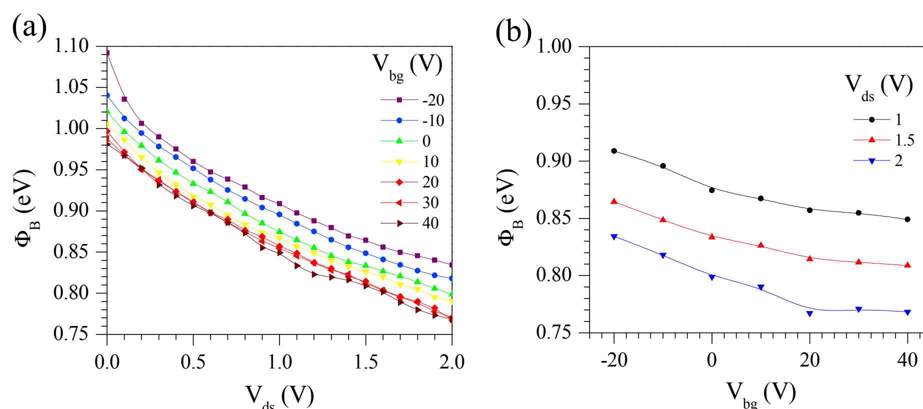

Figure 3. (**a**) Schottky barrier height (φ_B) at T = 300 K between monolayer Gr and 53-nm-thick ML-MoS_2 as a function of V_{ds} at different V_{bg}'s from −20 to 40 V with equal step of 10 V. (**b**) φ_B at T = 300 K as a function of V_{bg} at V_{ds} = 1, 1.5, and 2 V.

Moreover, planar resistance (R_{planar}) of the MoS_2 channel was measured by using the electrodes labelled as numeric letters in Figure 1b. While current was applied between 1 and 2, voltage was measured between 3 and 4. Figure 2c shows R_{planar} as a function of V_{bg}. As V_{bg} increases from −30 to 40 V, R_{planar} rapidly decreases, indicating MoS_2 is a *n*-type semiconductor. The MoS_2 channel thickness dependence of R_{planar} at V_{bg} = −10 V is shown in Figure 2d. As MoS_2 flake thickness increases, R_{planar} decreases in contrast to $R_{vert.}$ We can analyze R_{planar} as $R_{TCR\text{-}P}$ in 4-probe measurement configuration. Here, $R_{TCR\text{-}P}$ represents the in-plane resistance of MoS_2. As the thickness of MoS_2 channel increases, more layers can contribute to the planar electrical transport, so that total planer channel resistance, $R_{TCR\text{-}P}$ decreases. To have an estimate of contact resistivity, we employed transmission line method (TLM) on 51 nm-thick MoS_2 flake and extracted contact resistivity to be 0.14 MΩ µm at V_{bg} = −10 V as shown in Supplementary Materials Figure S4b. The contact resistivity is smaller than the planar resistivity of MoS_2 channel itself. So, it is obvious that there are other factors contributing to the total in-plane resistance other than contacts. The back-gate voltage-dependent contact resistivity was also estimated using TLM method as shown in Supplementary Materials Figure S4d. The contact resistivity decreases with V_{bg} and has a low value in the positive region of V_{bg} due to the increasing carrier channels.

In lateral devices, the source and drain contacts are directly attached to top surface of MoS_2. Therefore, the charge carriers will flow from source to drain mainly through a few top layers of MoS_2 due to the interlayer resistance [52,53]. Moreover, since the thickness of MoS_2 flake in the lateral device is ~50 nm (about 76 layers), the back-gate electric field will not affect much on the charge carrier transport. This could be the reason of a low R_{planer} for thick MoS_2 channel in the lateral devices.

3.4. Vertical Transport of (Cr/Au)/Mos_2/(Cr/Au) Vertical Field-Effect Transistor

We have studied vertical transport in (Cr/Au)/MoS_2/(Cr/Au) VFET, the schematic representation of which is shown in Figure 4a, and inset of Figure 4b shows the scanning electron microscope image. The thickness of MoS_2 is about 48 nm. While current bias is applied between 4 and 3, voltage is measured between 2 and 1. Figure 4b shows R_{vert} as a function of V_{bg} at room temperature. It shows similar characteristics as Gr/MoS_2/(Cr/Au) VFET, but with a low R_{vert}, which may be due to the low interface resistance between Cr/Au and MoS_2. The strong screening of electric field by the bottom Cr/Au electrode creates a weaker dependence on V_{bg}. The I-V characteristics show almost ohmic behavior at different back-gate voltages (see Figure 4c).

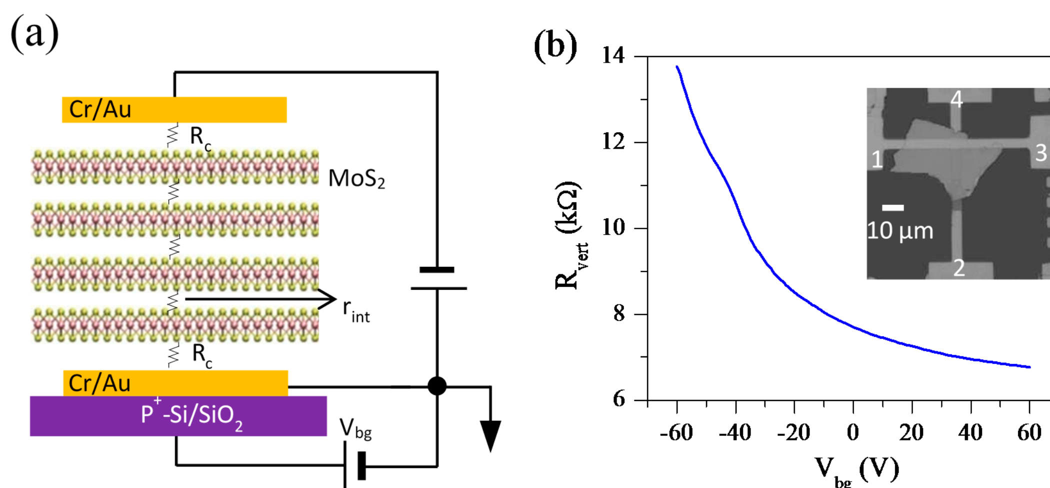

Figure 4. *Cont.*

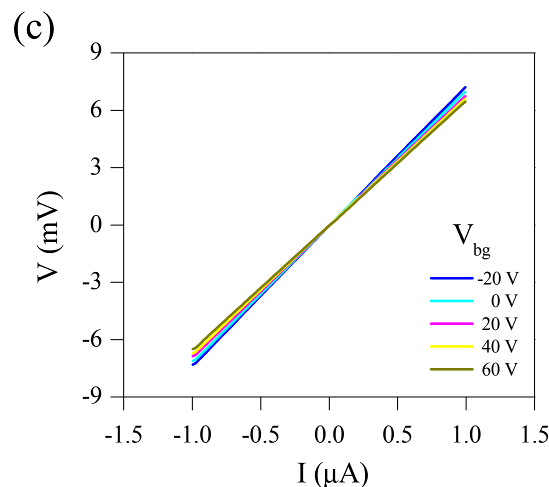

Figure 4. (**a**) Schematic diagram of the resistances to compose (Cr/Au)/MoS_2/(Cr/Au) vertical field-effect transistor (VFET). The thickness of MoS_2 is 48 nm. (**b**) R_{vert} as a function of V_{bg} for (Cr/Au)/MoS_2/(Cr/Au) VEFT. Inset: A scanning electron microscope image of the device. While the constant current of 1 μA is applied between 1 and 4, voltage is measured between 2 and 3. (**c**) I-V characteristics at different V_{bg}'s.

Although R_{vert} of (Cr/Au)/MoS_2/(Cr/Au) VFET in Figure 4b decreases as V_{bg} is increased, the relative change of R_{vert} is rather small. To compare the relative change of R_{vert} we obtain R_{vert}/R_0 as a function of V_{bg}, where R_0 at $V_{bg} = -10$ V is taken as a reference resistance. Figure 5a shows R_{vert}/R_0 as a function of V_{bg} for Gr/MoS_2/(Cr/Au) and (Cr/Au)/MoS_2/(Cr/Au) VFETs. The thickness of MoS_2 is 50 nm and 48 nm for Gr/MoS_2/(Cr/Au) and (Cr/Au)/MoS_2/(Cr/Au) VFETs, respectively. Of note, V_{bg} does not significantly affect transport characteristics in (Cr/Au)/MoS_2/(Cr/Au) VFET, because the bottom Cr/Au electrode effectively screens the electric field from the V_{bg} application. However, R_{vert}/R_0 has a strong dependence on V_{bg} in Gr/MoS_2/(Cr/Au) devices, due to the weak screening of the electric field by bottom monolayer Gr. For comparison, we also present R_{planar}/R_0 as a function of V_{bg} in Figure 5b. A rapid increase of R_{planar}/R_0 below $V_{bg} = -30$ V indicates the threshold voltage of *n*-type MoS_2 channel in our devices. The dependence of R_{planar}/R_0 on V_{bg} is much larger than VFETs, asMoS_2 channel is directly affected by V_{bg} application in ordinary planar geometry.

In the positive region of V_{bg}, both resistances in planar (in-plane) and vertical configuration show a similar dependence of V_{bg}. However, at negative V_{bg}, we find different dependences of V_{bg} as seen in Figure 5a,b. In Figure 5a R_{vert}/R_0 shows an exponential dependence of V_{bg} for Gr/MoS_2/(Cr/Au) VFET with 50 nm-thick MoS_2 flake. This might be due to the gate-voltage dependent density of states in graphene, which affects the interface resistance between graphene and MoS_2. In case of (Cr/Au)/MoS_2/(Cr/Au) VFET with 50 nm-thick MoS_2, there exists large screening effect by the bottom Cr/Au electrode that does not allow the back-gate electric field to influence on the electronic transport. On the other hand, in case of planar 48 nm-thick MoS_2 FET of Figure 5b, we have source/drain (Cr/Au) electrodes directly on the lateral channel of MoS_2. At a particular negative V_{bg}, the channel transport is in off-state, so resistance increases rapidly at V_{bg} below the threshold voltage.

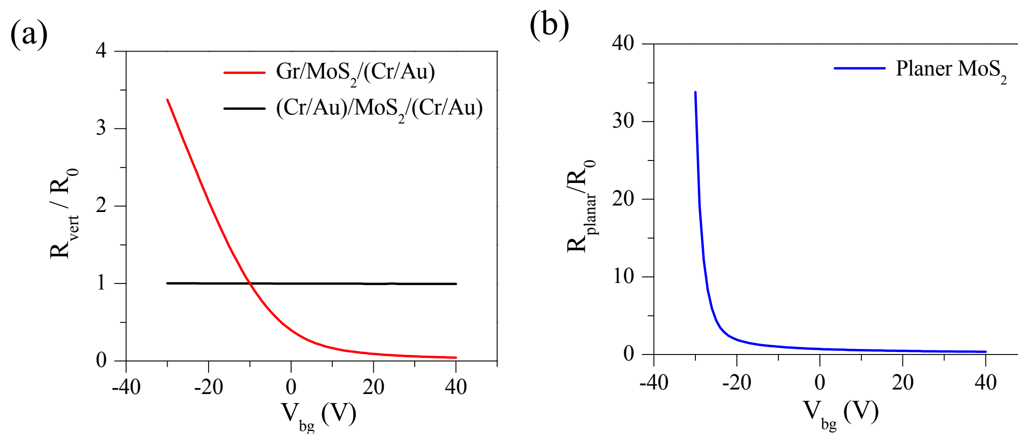

Figure 5. (**a**) R_{vert}/R_0 as a function of V_{bg}. While the thickness of MoS_2 is 50 nm for Gr/MoS_2/(Cr/Au) VEFT, the thickness of MoS_2 is 48 nm for (Cr/Au)/MoS_2/(Cr/Au) VEFT. (**b**) R_{planar}/R_0 as a function of V_{bg} for 48 nm-thick MoS_2 in planar geometry. Reference resistances (R_0) were taken at V_{bg} = −10 V. All measurements were done at T = 300 K.

4. Conclusions

In the present study, we performed four probe measurements using cross-junction geometry of Gr/MoS_2/(Cr/Au) VFETs. We were able to achieve gate-tunable transport characteristics in VFETs. Since the bottom Gr allows the electric field to reach MoS_2 channel, the vertical resistance (R_{vert}) of Gr/MoS_2/(Cr/Au) VFET can be effectively modified by V_{bg}. The vertical transport characteristics are examined as compared to those of the ordinary lateral MoS_2 field-effect transistor. R_{vert} increases as the thickness of MoS_2 increases, whereas R_{planar} decreases. The increase of R_{vert} in the thicker MoS_2 film can be attributed to the interlayer resistance in the vertical direction. However, R_{planar} shows a lower value for a thicker MoS_2 film because of excess of charge carriers available in upper layers connected directly to source/drain contacts and cumulative contribution of low R_{int} from the lower layers. In planer geometry only, layers attached near to channel layer (on which source/drain electrodes are constructed) are the main source of the conduction mechanism. Schottky barrier height at Gr/MoS_2 interface can be analyzed from the I_{ds}-V_{ds} curve. The Schottky barrier height decreases as V_{bg} or V_{ds} increases. V_{bg} does not affect transport characteristics much in (Cr/Au)/MoS_2/(Cr/Au) VFET, because the bottom Cr/Au electrode effectively screens the electric field from the V_{bg} application. However, a strong dependence on V_{bg} in Gr/MoS_2/(Cr/Au) devices was observed due to the weak screening of electric field by bottom Gr. We believe that gate tunable VFET will serve as one of important components for future 2D materials electronics.

Supplementary Materials: The following are available online at www.mdpi.com/2079-4991/8/1/14/s1.

Acknowledgments: This research was supported by Priority Research Center Program (2010-0020207) and Basic Science Research Program (2016R1D1A1A09917762) through the National Research Foundation of Korea funded by the Ministry of Education.

Author Contributions: J.E. and G.N. conceived and designed the experiment; M.F.K., S.A., G.D. and A.M.A. contributed to device fabrication and measurement. M.A.R. carried out ALD process to grow HfO_2. Y.S. and J.E. contributed to discussion of the manuscript. G.N. and J.E. wrote the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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