Supply-Doubled Pulse-Shaping High Voltage Pulser for CMUT Arrays

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Abstract

A supply-doubled pulse-shaping high voltage (HV) pulser is presented for medical ultrasound imaging applications, particularly those that use capacitive micromachined ultrasonic transducers (CMUT). The pulser employs a bootstrap circuit combined with dynamically-biased stacked transistors, which allow HV operation above process limit without lowering device reliability. The new pulser overcomes supply voltage limitation of conventional unipolar pulsers by generating output signals that are almost twice the supply level. It also can generate three-level pulses to further optimize the transmit pressure signals. A proof-of-concept prototype has been implemented in 0.18-μm HV CMOS/DMOS technology with 60 V devices. Measurement results show that the HV pulser can safely generate controllable three-level pulses with up to 85 V_{pp} from 45 V supply. Acoustic measurements are conducted connecting the pulser to a CMUT with 2 pF capacitance and 8.3 MHz center frequency. The pulse shape has been adjusted for the CMUT under test to generate maximum pressure output and the results are in good agreement with a large signal CMUT model.

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Index Terms

High voltage pulser; capacitive micromachined ultrasound transducer (CMUT); medical ultrasound imaging

I. Introduction

Medical ultrasound imaging has had a significant impact on clinical practice by providing real-time images of different organs with high spatiotemporal resolution non-invasively at low cost [1]. In recent years, the capacitive micromachined ultrasound transducers (CMUT) have shown several advantages over the conventional bulk piezoelectric transducers, due to smaller size, wider bandwidth, and ease of integration with interfacing circuitry [2]. Compared to piezoelectric transducers, CMUTs typically have larger electrical impedances for the same transducer area. Although integration with reduced parasitics lead to low noise CMUT receivers [3], larger voltages are required to generate the required pressure output by CMUT transmitters as compared to piezoelectric transducers. Therefore, CMUT based ultrasound systems would benefit from high voltage (HV) ultrasound pulse generators that utilize the maximum available voltage level given the integrated circuit process constraints.

Ultrasound pulse generator, *aka* pulser, is one of the key building blocks of medical ultrasound imaging systems, which drives the ultrasound transducers, including CMUTs with high voltage (HV) output swing to create an ultrasonic pressure pulse towards the target tissue. HV digital pulsers are commonly used in current commercial systems for their simplicity [4], while recent publications shows that linear amplifiers are also becoming attractive in driving piezoelectric transducers, capable of generating low harmonic content signals by adopting apodization profiles [5]. To drive a CMUT load, however, its nonlinear distortion could refute good linearity performance of the linear amplifier's output signal. Moreover, amplifiers have higher power consumption and considerable power loss when charging and discharging the CMUT parasitic capacitance, which reduce the pulser power efficiency [6]. A three-level pulser with pulse shaping and charge recycling capabilities has also been reported in [7], saving power in the pulser at the cost of requiring multiple supply voltages, which need HV DC-DC converters and extra capacitors, which increase the overall system complexity and power consumption. Furthermore, there is demand for pulsers capable of generating versatile HV output waveforms efficiently within a compact chip area especially for applications such as intracardiac echocardiography (ICE) and intravascular ultrasound (IVUS) imaging, which are implemented on catheters that are only 1 mm to 3.3 mm in diameter (3–10 F) [8].

The main challenges in designing interface electronics in these applications are limited space, temperature rise, supply voltage drop across long interconnects, and number of control lines in the catheter. These applications clearly benefit from interface electronics integration, such as CMUT-on-CMOS or flip-chip bonding [9], [10]. To further reduce the catheter electrical interconnect complexity, the ultrasonic transmitter (US-Tx) beam-forming, driver electronics and HV pulser can be integrated directly under the CMUT array. In addition, the CMUT fabrication processes allow for fabricating HV capacitors within its

MEMS structure, which can be used in the pulser bootstrap circuit to further reduce the size and voltage drop across the long catheter wires by using a lower external supply voltage.

In this brief, we present an integrated HV pulser for CMUT arrays, that provides pulse-shaping and an output swing close to twice its supply voltage above the device breakdown, which is often limited by the CMOS process. The following section describes the new pulser circuit topology, including its voltage doubler. Experimental setup with CMUT and measurement results are presented in section III, followed by conclusions.

II. High Voltage Pulser Design

A. Circuit topology

The primary objective of this circuit is to generate sharp pulses with amplitudes close to twice the supply voltage without violating safe operating range of its circuit elements. A simplified schematic diagram of the proposed pulser is depicted in Fig. 1a. The external control logic generates low voltage control signals and level shifters convert the dc voltage levels to drive double-diffused metal oxide semiconductor (DMOS) transistors of the pulser. Fig. 1b shows operation of the voltage doubling stage. A capacitor, C, which can be on-chip or integrated with the CMUT array, is charged to V_{DD} during charging mode through S_1 and S_4. Then, a HV switch, S_2, drives the negative terminal of C to V_{DD} during doubling mode, while all other switches are open for V_{out} to reach $2V_{DD}$. S_3 is used to discharge C by connecting it to ground. The CMUT can be modeled mainly as a capacitive load, resulting in a capacitive voltage divider between C and CMUT, which indicates the actual output pulse voltage. The voltage doubling stage requires careful design because it goes beyond the process operating voltage. To ensure safe operation, we employed dynamically gate-biased transistor stack and Schottky diodes to protect all the transistors from out of range operating conditions.

B. Design and operation of voltage-doubling pulser

Fig. 2 shows detailed schematic of the proposed pulser, which is driven by three input control signals (I_1, I_2, and I_3). Two N-type DMOS transistors, M_1 and M_3, are driven by 0 – 5 V control signals. Two P-type DMOS transistors, M_2 and M_5, are driven by 40 – 45 V level-shifted control signals. Note that in this case, V_{DD} = 45 V. To achieve a compact design, simple level shifters are used in Fig. 2b, while ensuring that IN_{P1} and IN_{P2} generate 40–45 V sharp pulses with low current consumption, compared to the CMUT driving stage [11].

The circuit operation is similar to the bootstrapping circuits in [12]. During charging mode, the external capacitor, C, is charged up to $V_{DD} - (V_{D2} + V_{D3})$ by turning on M_1 and M_5 transistors, where ($V_{D2} + V_{D3}$) is the forward voltage drop across D_2 and D_3. When C is charged, we turn on M_2 and turn off all the other transistors so that V_{out} is bootstrapped to $2V_{DD} - (V_{D2} + V_{D3})$. During this doubling mode, it is crucial to ensure that all devices in the circuit are operated in their safe operating conditions, considering the fact that in this process, the drain-source junction breakdown and gate-oxide breakdown voltages are 60 V and 5 V, respectively. To prevent excessive V_{DS} on M_5 and its parasitic N-well substrate

diodes from turning on, two HV Schottky diodes are added in series with M$_5$. Each diode has a maximum reverse voltage of 36 V, and when the output is doubled, the two diodes should handle 45 V of total reverse voltage between them, resulting in each diode having reverse voltage well below its limit.

Between V_{out} terminal and GND, stacked N-type DMOS transistors, M$_3$ and M$_4$, are used to ensure safe operation when V_{out} is doubled. The gate of M$_4$ is dynamically biased to V_{DD} during doubling mode, while M$_3$ is turned off. The Zener diode, D$_1$, keeps V_{GS} of M$_4$ below 5 V, so that M$_3$ and M$_4$ can divide the doubled output voltage across their designated drain-source voltage limit.

The value of external capacitor, C, is key to determine the pulser V_{out} and slew rate according to,

$$V_{out1} = V_{DD} - (V_{D2} + V_{D3}), \quad (1)$$

$$V_{out} = V_{DD} + V_{out1} \times \frac{C}{C + C_{CMUT}}, \quad (2)$$

where C_{CMUT} is the equivalent capacitance of the CMUT. Therefore, C should be large to obtain higher V_{out}. However, larger C would increase the output RC time constant, limiting the operating frequency range and slew rate of output pulses,

$$SR = \max\left(\frac{dV}{dt}\right) = \frac{I_{max}}{C + C_{CMUT}}, \quad (3)$$

where I_{max} is the maximum current sourced to capacitance. By decreasing slew rate, V_{out} will suffer from slow charging problem. Moreover, if C is integrated in the CMUT, its value may be limited by the size of the CMUT. Thus deciding the optimal value of C is critical in the pulser design.

In this study, we consider a particular application of 2-D CMUT array for intracardiac echography (ICE), where the center frequency is about 8.3 MHz and CMUT array element size is limited to approximately 100×100 μm^2, resulting in $C_{CMUT} = 2$ pF. We also investigated the case for an 8 pF device capacitance, realized by an oscilloscope probe (P6139A, Tektronix) in electrical characterization.

A realistic design target for the pulser would be to achieve peak HV level of at least $1.8 \times V_{DD}$ while having a rise time less than a quarter period of the CMUT center frequency, i.e. 30 ns for the 8.3 MHz CMUT. (1) and (2) suggest that the minimum required C would be > $4 \times C_{CMUT}$. Considering the forward voltage drop across the diodes and parasitic

capacitances of the large DMOS transistors, we chose $C = 30$ pF for 2 pF of C_{CMUT}. Also to obtain $SR > 3$ V/ns during the charging mode, we designed M_5 to have $I_{max} > 100$ mA, based on (3). Since the size of large DMOS transistors mainly define the layout size, we chose I_{max} for driving a 2 pF CMUT load at 8.3 MHz center operating frequency.

To verify the pulser design and compare with measurements we simulated the voltage-doubled output pulse for 2 pF of CMUT load and 8 pF of passive probe loading, for which C was changed within $10 - 40$ pF and $30 - 150$ pF, respectively. For ensuring the initial condition of $V_{out} = 0$ V, a 100 kΩ resistor was added in parallel with C, which adds a slight slope on doubled output pulse with minimal effect on output voltage division. With 2 pF load, $C = 30$ pF shows 85 V_{pp} of output pulse, rise time of 11.5 ns, and $SR = 3.2$ V/ns in the charging mode, which is suitable for driving a CMUT array with 8.3 MHz center frequency. With 8 pF load, $C = 100$ pF shows 85 V_{pp} of output pulse, rising time of 34.8 ns, and $SR = 1.0$ V/ns during charging mode. The slew rate of the doubling stage does not depend on the value of C, as evident in Fig. 3, because the charged C is simply connected in series with V_{DD}.

C. Three level pulse shaping above the process limit

Multi-level pulsing circuits have been adopted in the past for driving CMUTs and piezoelectric transducers due to better power efficiency, requiring several supply voltages or DC-DC converters with large off-chip capacitors [7]. Since the capacitors required for DC-DC converters are often quite large, using off-chip components would be inevitable. A potential advantage of the proposed pulser is that it requires a capacitor 10 to 15 times larger than C_{CMUT}, which can be implemented together with the CMUT microfabrication. For example, using a high-K dielectric like hafnium dioxide with $e_r = 16$, one can fabricate a capacitor with $C > 10 \times C_{CMUT}$ underneath the CMUT using the same area by replacing the vacuum gap with the high-K dielectric [12]. This approach would enable fabrication of a high voltage capacitor in the CMUT layer for compact ultrasound analog front end design.

It is worth noting that this pulser surpasses the maximum operating voltage level imposed by the process to generate three different output levels. As shown in Fig. 4, with three control signals, I_1, I_2, and I_3, the measurement results show that the pulser can generate up to 85 V_{pp} from 45 V supply. Different pulse shapes can be obtained with the three control signals. Changing durations of T_1, T_2, and T_3 will affect the width of middle (45 V) and high (85 V) levels. Different pulse shapes affect the acoustic power and frequency content of the US-Tx, and there is an optimal pulse shape for maximizing the Tx acoustic power for any particular CMUT load.

III. Experimental Results

The proposed pulser was designed and fabricated in a 0.18-μm 60 V power management 4M1P HV-CMOS process, and occupied a core area of 0.2 mm^2, as shown in Fig. 5. The chip was mounted on a PCB inside a QFN package along with an off-chip surface mount capacitor, C. Fig. 6 shows the measured output voltage with two different C and more than 8 pF loading, including the input capacitance of a passive probe and parasitic capacitance of wire-bonding and PCB routing in parallel with 100 kΩ resistor. The measured waveform

with $C = 100$ pF, shows peak $V_{out} = 85$ V and slew rates of 0.88 V/ns, 3.2 V/ns, and 2.44 V/ns during charging, doubling, and falling modes, respectively. Similarly, with $C = 30$ pF, peak $V_{out} = 78.6$ V was achieved with slew rates of 2.1 V/ns, 2.9 V/ns, and 4.7 V/ns, respectively. Fig. 4 shows a sample measurement with non-zero T_1, T_2, and T_3 values overlapped for comparison with the simulations.

An acoustic pressure measurement setup was used to measure the US-Tx pressure with an actual CMUT load, as shown in Fig. 7. The CMUT used in this experiment occupied 100×100 μm^2 area on silicon and consisted of a 2×2 array of four 45 μm wide square membranes. It created a 2 pF element, ~1.8 pF of which was due to bond pads parasitic capacitance, with 8.33 MHz center frequency and −3 dB bandwidth of 5 MHz. It was part of a larger 2-D ICE imaging array, which was fabricated using a low temperature CMOS-compatible process [9]. The CMUT array, mounted on a separate PCB, was connected to the larger pulser board via header pins. The off-chip capacitor, $C = 30$ pF, was selected to obtain maximum output swing and fast slew rate as discussed in section II. The CMUT array was submerged in a water tank, while a hydrophone (HGL-0085, Onda Corp) was placed above the CMUT array, 4.5 mm from its surface, to measure the US-Tx acoustic pressure. The pulser generates a single pulse with 60 ns pulse width and 8.3 MHz center frequency. We generated different pulse shapes to evaluate their impact on the US-Tx output pressure.

The pulse shape is defined by $\{T_1, T_2, T_3\}$, as shown in the Fig. 4. When $\{T_1, 0\ ns, 0\ ns\}$ is applied, a two-level pulse is generated, which is not doubled. When only T_3 is 0 ns, a three-level voltage doubled pulse, shown in Fig. 6, is generated. The measured peak-to-peak US-Tx pressure results are summarized in Fig. 8a. V_{DD} in these experiments was reduced to 30 V because the CMUT breakdown voltage was 60 V. The maximum peak-to-peak pressure of 2467 Pa was recorded with $\{30, 30, 0\}$, as shown in Fig. 8b. This is a desired pulse shape because it generates more than twice the pressure level obtained from the conventional two-level pulse (1100 Pa) using the same 30 V supply. The optimal pulse shape varies with supply voltage because slew rate limitation can lower the maximum voltage level, reducing the acoustic output pressure. Pulses with T_1 lower than the output RC settling time cannot fully double the supply voltage. Measured RC settling time showed 25 ns, hence 20 ns of T_1 pulses might not efficiently generate supply doubled pulse with 30 V supply voltage, as shown in Fig. 8a. Measurements show that every doubled pulse shape generates higher pressure than the conventional two-level pulse. To test the validity of experimental results, we used a large signal nonlinear CMUT model to predict the pressure signal variations with similar pulse shapes [15]. Normalized pressure variations simulated by the model follow the measurements closely in Fig. 8a, indicating that this pulser structure along with the large signal model can offer higher performance. Table I summarizes the pulser specs for the $\{30, 30, 0\}$ pulse shape and benchmarks its performance against prior work. Measurements from over 20 chips have shown consistent results with the maximum V_{out} (mean±std) = 84.24 ± 1.52 V, indicating reliability of this HV pulser circuit.

IV. Conclusions

This brief presents an integrated voltage-doubling and pulse-shaping HV pulser circuit to interface CMUT ultrasound systems in a 0.18-μm 60 V 4M1P CMOS/DMOS process. The

presented circuit overcomes process limitation by adopting HV protection techniques that generate 85 V_{pp} of output pulse with 45 V supply voltage. A three level pulsing scheme is successfully applied to a CMUT array element and optimized for maximum acoustic pressure, as predicted by a large signal CMUT model, paving the way for simulation-based CMUT pulser optimization. The prototype pulser ASIC measurements were conducted with an off-chip capacitor, which can be integrated with the CMUT using high-K dielectric layers during CMUT fabrication. Our ongoing research involves co-optimization of the pulser and CMUT arrays using CMUT-on-CMOS technology for very compact catheter-based ultrasound imaging systems.

Acknowledgments

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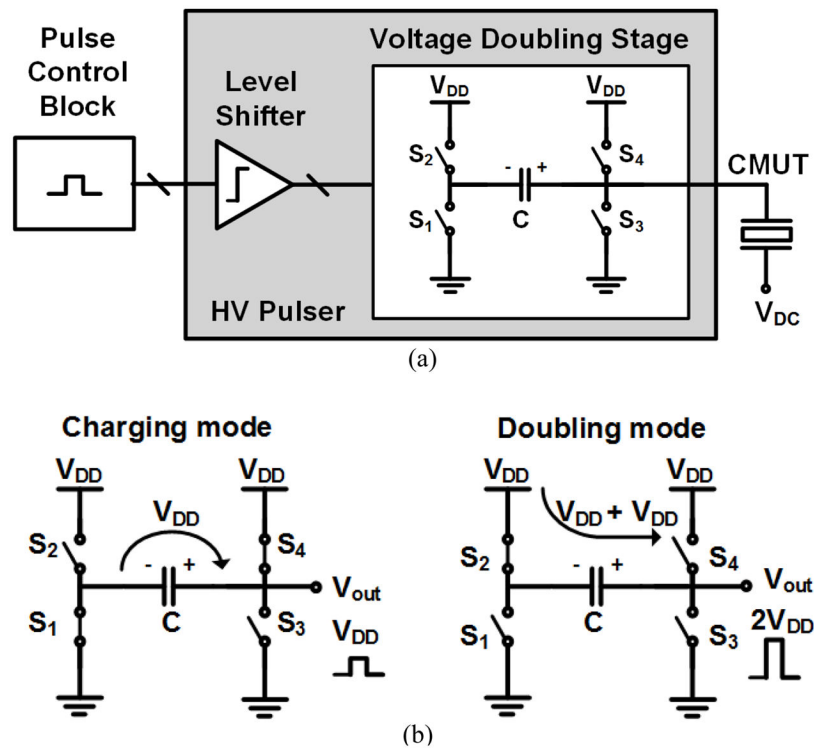
Fig. 1.
(a) Simplified schematic diagram of the supply-doubled pulse-shaping high voltage pulser, and (b) the operation of voltage doubling stage.
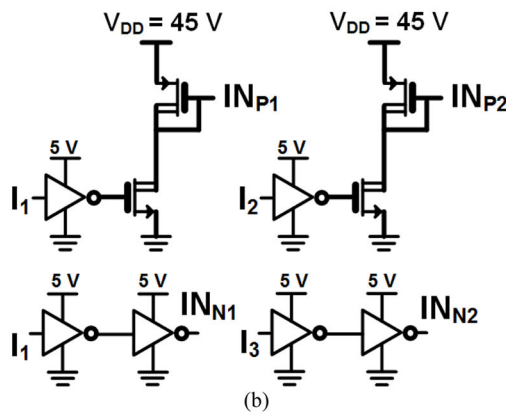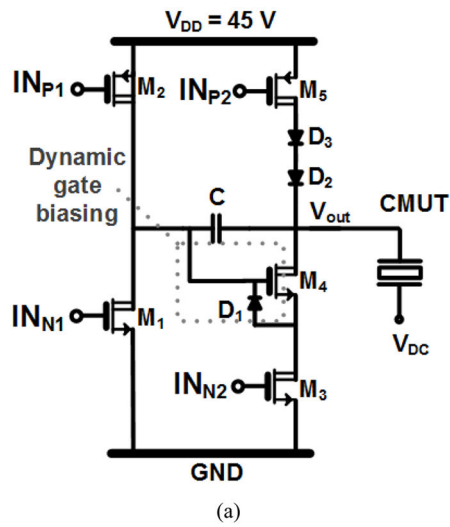
Fig. 2.
(a) Schematic of the proposed voltage doubled pulser. (b) Schematic of the input driving buffers and level shifters for high voltage PMOS input signals.
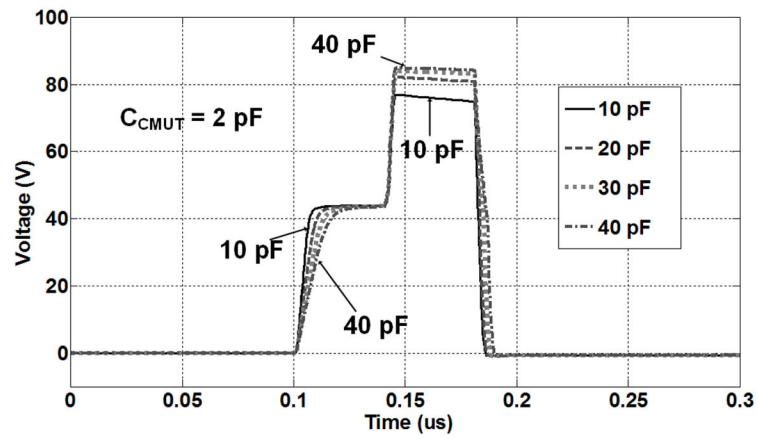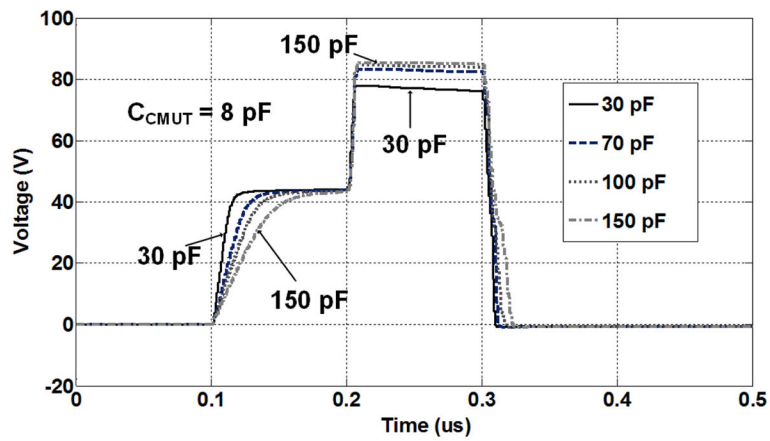
Fig. 3.
Simulation of the output pulse with different C values, (a) when CMUT loading is considered 2 pF, (b) C_{CMUT} = 8 pF.
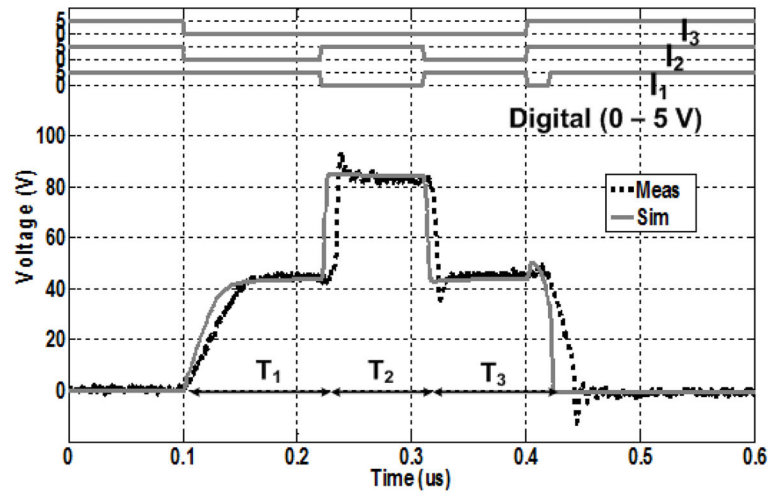
Fig. 4.
Simulated and measured three-level output pulse along with three input control signals. $C =$ 100 pF, $C_{CMUT} = 8$ pF.
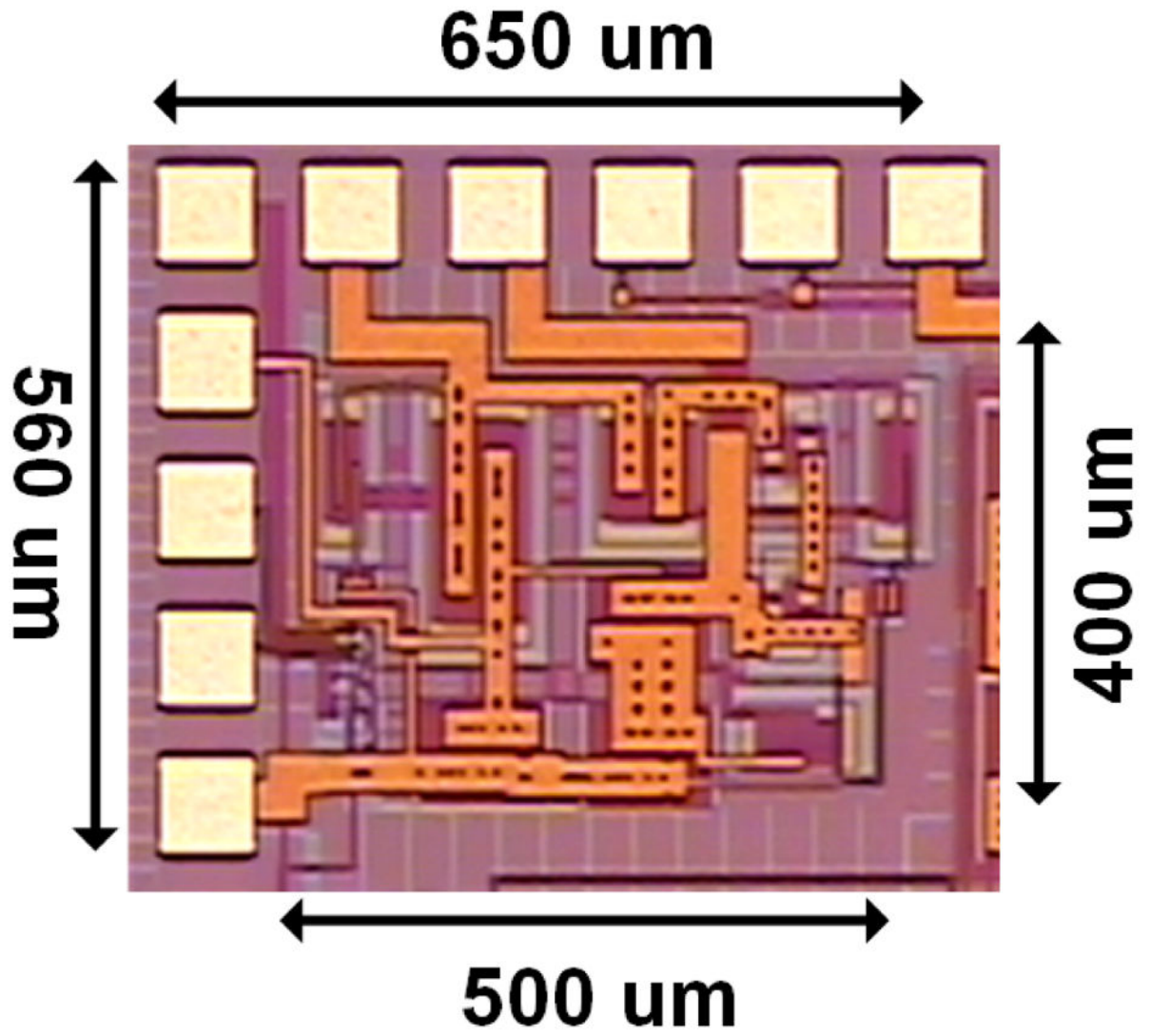
Fig. 5.
Microphotograph of the proposed pulser chip.
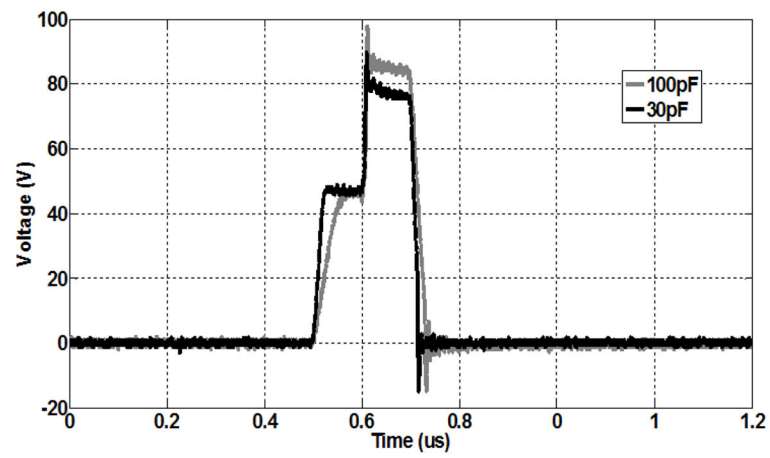
Fig. 6.
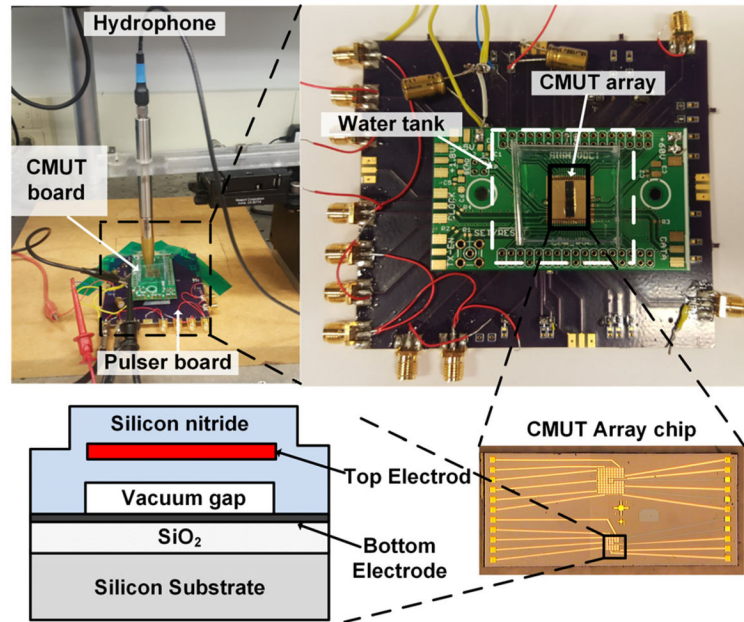Measured output pulse with $C = 30$ pF and 100 pF when CMUT loading is 8 pF.

Fig. 7.
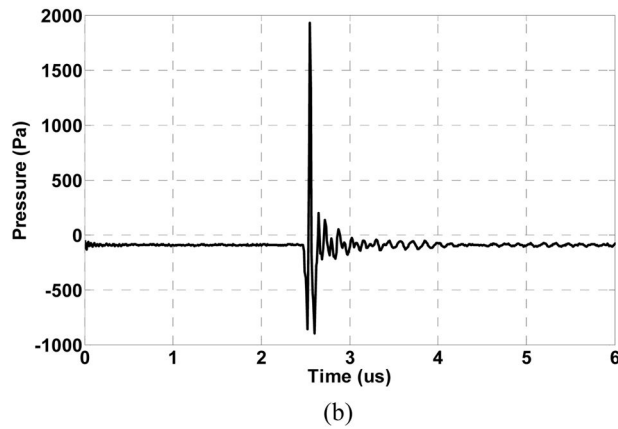Acoustic pressure experimental setup with CMUT array board and pulser board.
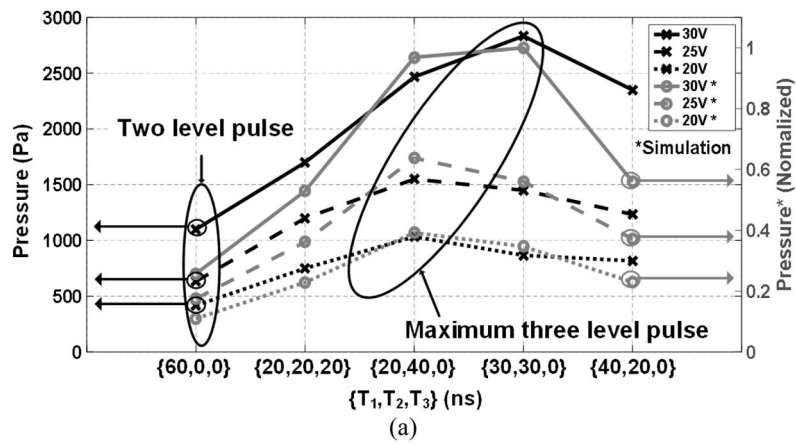
Fig. 8.
(a) Transmitted peak-to-peak acoustic pressure measurement and simulation with different pulse shapes and supply voltages. (b) Measured transmitted pressure with $T_1 = 30$ ns, $T_2 = 30$ ns, $T_3 = 0$ ns, and $V_{DD} = 30$ V.

Table I

Benchmarking of the Proposed Pulser Performance

Parameter	This work	[7]	[11]	[14]
Input voltage (V)	5	3.3	3.3	1.8
Output voltage (V)	85	30	60	12.8
V_{DD} (V)	45	30	60	12.8
Frequency (MHz)	8.33	2.5 to 5	1.38	1.25
Rise/fall time (ns)	26,16/18	30	68/68	40/50
Power (mW)	48.6	52.4	98.1	
Power (mA)	150 Dynamic *	-	-	19.9 Dynamic *
Chip area (mm^2)	0.2	-	0.08	0.022
Output load (pF)	2	40	18	15
Pulse shaping	Y	Y	N	N
Technology (μm)	0.18	0.18	0.35	0.18

*
Simulation results