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A Bidirectional-Current CMOS Potentiostat for Fast-Scan Cyclic Voltammetry Detector Arrays

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Abstract

A potentiostat circuit for the application of bipolar electrode voltages and detection of bidirectional currents using a microelectrode array is presented. The potentiostat operates as a regulated-cascode amplifier for positive input currents, and as an active-input regulated-cascode mirror for negative input currents. This topology enables constant-potential amperometry and fast-scan cyclic voltammetry (FSCV) at microelectrode arrays for parallel recording of quantal release events, electrode impedance characterization, and high-throughput drug screening. A 64-channel FSCV detector array, fabricated in a 0.5-μm, 5-V CMOS process, is also demonstrated. Each detector occupies an area of 45 μm × 30 μm and consists of only 14 transistors and a 50-fF integrating capacitor. The system was validated using prerecorded input stimuli from actual FSCV measurements at a carbon-fiber microelectrode.

Keywords

CMOS potentiostat; bidirectional current; VLSI detector array; fast-scan cyclic voltammetry (FSCV); quantal release; microelectrode arrays; high-throughput drug screening; electrode impedance characterization; dopamine detection

I. INTRODUCTION

NEURONS, the fundamental units of the nervous system, communicate with each other via a chemical signaling process mediated by the storage and release of neurotransmitters, a set of biomolecules that act as chemical messengers to regulate neuronal function and behavior [1]. Neurons store high concentrations of these biomolecules in small membranebound secretory vesicles attached to the inside of the presynaptic plasma membrane. When the presynaptic terminal is electrically stimulated, the vesicles fuse with the plasma membrane through a process called exocytosis, releasing the vesicle contents into extracellular space [2]. Neurotransmitter release from a single vesicle is termed quantal release. The number of biomolecules expelled in a quantal release event is the quantal size [3]. Quantal release has been the subject of extensive medical research because some of the underlying molecular mechanisms mediating exocytosis are still not fully understood. A better understanding of properties such as the quantal size and the frequency and time course of quantal release events is necessary for the discovery and development of new therapeutic drugs that modulate these properties.

Several recording techniques have been used to investigate the properties of quantal release events and their modulation. Constant-potential amperometry (CPA) [4], [5] at a polarizable working electrode is one of the prevalent techniques. Typically, a carbon-fiber microelectrode (CFM) is used as the working electrode due its chemically inert properties, small dimensions (5–20 μm diameter), and thus low noise, allowing high bandwidth recording [6].

In CPA at a CFM, the electrode is held at a positive potential (0.6–0.7 V) with respect to a silver/silver-chloride (Ag|AgCl) reference electrode. Neurotransmitters and hormones from the catecholamine family, such as dopamine and its conversion products adrenaline and noradrenaline, easily oxidize when they come in contact with the surface of the CFM, releasing two electrons each in the process [7]. The resulting electron transfer is then measured as a transient current. Thus, a single exocytotic event such as catecholamine release from chromaffin cells or dopamine release from dopaminergic neurons can be measured as an amperometric current spike, with high precision and high temporal resolution using amperometry. Integration of the transient current spike yields the total charge, from which quantal size can be calculated.

However, CFM recording techniques have their limitations being only capable of measuring quantal release events from a single cell at a time. Each experiment is time-consuming and laborious, requiring precise manual positioning of the CFM adjacent to an individual cell that releases neurotransmitters. Thus, CFM recordings are not suitable for drug screening, an

application that requires a statistically significant set of measurements from a large number of cells to obtain conclusive evidence on the effect of a drug on quantal release.

Microelectrode arrays (MEAs) have recently emerged as a viable candidate to replace CFMs as the working electrode mainly because the microfabrication and surface modification techniques involved in the production of MEAs not only provide better reproducibility than traditional CFM fabrication methods but also facilitate batch fabrication of the electrodes [8], [9]. Surface-patterned planar MEAs using noble metals such as gold and platinum and other materials have recently been applied to measure quantal release events from single cells [10]. Scalable arrays incorporate CMOS potentiostats with on-chip electrodes for parallel recordings from large numbers of cells [11]–[14].

Proper functionality of electrochemical electrodes is generally assessed by cyclic voltammetry (CV), in which the voltage applied to the microelectrode is not held constant but instead is ramped from −0.5 V to +1.0 V and back from +1.0 V to −0.5 V (vs. Ag|AgCl). The resulting current reflects the electrode impedance and thus the basic functionality of the electrode. In addition, test analytes such as ferricyanide, which is reduced to ferrocyanide, forming a well-behaved redox pair [10], as well as other compounds [15], have been used in conjunction with cyclic voltammetry for characterization of the performance of electrochemical electrodes. Such measurements cannot easily be performed with unipolar CMOS chips because they require not only the application of bipolar voltages but also the measurement of bidirectional currents.

Cyclic voltammetry can also be used to distinguish between different electroactive species. Fast-scan cyclic voltammetry (FSCV) has been used to perform such measurements on release events from different cell types [7], [16]. In FSCV at a CFM [17], [18], the electrode potential is typically ramped up and down within 10 ms, and these sweeps, or scans, are repeated every 100 ms. The fast rate at which the voltage changes, or the high scan rate, gives rise to a large background current on which the small *faradaic* current from the reduction and oxidation (*redox*) of an electroactive compound is superimposed [19]. To recover the *faradaic* current, the background current elicited during the absence of the compound is subtracted from the total current (sum of background and *faradaic* currents) elicited during the presence of the compound through a procedure known as background subtraction [20]. This *faradaic* component is then plotted versus the applied voltage to yield a background-subtracted voltammogram from which the *redox* voltages can be extracted to identify the detected compound.

This paper reports a precision bidirectional-current CMOS potentiostat circuit along with a prototype 64-channel VLSI FSCV detector array to accelerate the development and testing of new treatments that modulate the size and the kinetics of quantal release. The detector array provides a five-fold increase in temporal resolution over the unidirectional-current detector array we reported previously in [11], [13].

The remainder of this paper is organized as follows: Section II introduces the architecture of the detector array. Section III details the implementation of the core potentiostat unit along

with on-chip timing and read-out blocks. Section IV reports measurement results, Section V provides a discussion, and Section VI concludes this paper.

II. SYSTEM ARCHITECTURE

Fig. 1 illustrates a system-level diagram of the 64-channel VLSI FSCV detector array. As shown in Fig. 1a, the array consists of a read-out column with on-chip biasing and timing blocks. As depicted in Fig. 1b, the read-out column consists of a set of 64 detectors that share a common output stage, which in turn consists of a voltage follower, correlated double sampling (CDS) circuit and unity-gain output buffer similar to the one described in [14]. The CDS circuit provides $1/f$ noise and offset cancellation. The output buffer provides a low output impedance to ensure reliable read-out at a sampling rate of 640 kS/s. The detectors in the read-out column are switched sequentially through a set of select signals from the timing block using a time-division multiplexing technique described in detail in Section III. The output of the read-out column is then fed to an external A/D converter for acquisition.

III. CIRCUIT IMPLEMENTATION

A. Bidirectional-Current CMOS Potentiostat

Traditional unidirectional-current potentiostat circuits such as the one described in [21] use a DC offset current to measure bidirectional currents, which not only adds noise (but does not provide gain) to the signal path but also disturbs the charge balance of the electrode-electrolyte interface [22]. The main contribution of this work is a novel potentiostat circuit that enables bidirectional-current measurements from *redox* processes without use of a DC offset current. The bidirectional-current detection feature doubles the total input current range and enables not only amperometry but also cyclic voltammetry at MEAs.

Fig. 2a shows a schematic diagram of the core potentiostat unit, which consists of integration capacitor C_{INT}, switch M_0, cascode transistors M_1 and M_4, mirror transistors M_2 and M_3, and inverting half amplifiers A_1 and A_2, that take advantage of the shared amplifier scheme from [14] to minimize the transistor count per detector. Each detector also includes built-in current mirrors B_P and B_N for calibration currents I_P and I_N, respectively. The reference half of the calibration mirrors and the shared non-inverting half amplifier A_0 (*dashed lines*) are not part of the detector unit. The core unit was implemented at the cost of only seven additional transistors compared to the one reported in [14]. Fig. 2b shows a schematic diagram of the non-inverting shared half amplifier A_0 and the inverting half amplifiers A_1 and A_2 acting as a folded-cascode amplifier. The amplifier consists of current source M_5, input differential pair M_6–M_{6a}, load devices M_7–M_{7a} and M_8–M_{8a}, and cascode devices M_9–M_{9a}. Table I lists all device dimensions, bias voltages and capacitor values. Note that M_5 in the shared half amplifier carries $(N+1)I_B$ where I_B is the bias current, and N is the total number of inverting half circuits that share a single non-inverting half amplifier, to minimize the transistor count per detector. In this work, $N = 4$ because two detector units, and thus two pairs of inverting half amplifiers, share a single non-inverting half amplifier.

The circuit operates as follows: Assuming the Ag|AgCl reference electrode is held at 1.5 V (*virtual* ground), a voltage ramp (or constant voltage or arbitrary time-varying waveform) is

applied to the working electrode at node V_{IN} in the range of 1.0 V to 2.5 V to yield an equivalent range of −0.5 V to +1.0 V vs. Ag|AgCl. A reset signal RST is initially asserted to precharge node V_{INT} to V_{DD} via M_0. After the reset signal is de-asserted, node V_{INT} is discharged with the input current through either M_1 or M_4 for a period of 100 μs. The 100-μs integration time was chosen to provide a 10-kHz sampling rate, which is appropriate to resolve amperometric spikes from chromaffin cells and FSCV data. For positive input current ($I_{IN} > 0$), which is generally present during the positive slope of the voltage ramp, the circuit operates as the regulatedcascode amplifier from [14], depicted in Fig. 2c. In this case, negative feedback forces $V_X = V_{IN}$ and $V_A > V_X$, which turns on cascode transistor M_1 and allows I_{IN} to flow directly out of C_{INT} into the electrolyte, producing an integration voltage given by

$$V_{INT} = V_{DD} - \frac{1}{C_{INT}} \int_0^{T_0} I_{IN}(t)dt, \quad (1)$$

where T_0 is the period of the integration phase. For negative input current ($I_{IN} < 0$), which is generally present during the negative slope of the voltage ramp, the circuit operates as the source-driven active-input regulated-cascode mirror from [23], shown in Fig. 2e. In this case, negative feedback forces the following conditions: $V_A < V_X$, which shuts off M_1 and turns on M_2–M_3; $V_B > V_Y$, which turns on M_4; and $V_X = V_Y = V_{IN}$, which allows all of the input current to flow through M_2 and to be mirrored onto M_3 with high accuracy, producing an integration voltage identical to (Equation 1) across a wide range of applied voltages. This configuration provides very low systematic transfer error by ensuring the drain-to-source voltages of M_2–M_3 are identical. Mismatch between M_2–M_3 certainly results in a random gain error. For this process, the current mismatch varies inversely with the square root of the gate area (Pelgrom's rule), and NMOS transistors have 2×–3× better current matching for a given size. M_2–M_3 are NMOS transistors, which is advantageous from a matching viewpoint for a given amount of area. With a drawn area of 9 μm^2, the coefficient of variation for M_2–M_3 is ~10%. In addition, B_P and B_N can be used to calibrate the gains of both the positive and negative current measurements, which can further minimize the gain errors.

A detailed noise analysis of the circuit has been previously presented in [14] for the regulated-cascode amplifier mode of operation shown in Fig. 2c, where the input current flows through M_1 into the solution ($I_{IN} > 0$). In this case, the dominant noise sources will be M_6–M_{6a}, M_7–M_{7a}, and M_8–M_{8a} in A_0–A_1. Similar analysis for the active-input regulatedcascode mirror mode of operation shown in Figs. 2d–2e, where the input current flows through M_2 from the solution ($I_{IN} < 0$), suggests that the relative contributions of the noise sources depends on the electrode impedance, which is difficult to predict with certainty, but the dominant noise sources are likely to be M_2–M_3, besides M_6–M_{6a}, M_7–M_{7a}, and M_8–M_{8a} in A_0–A_2. For zero input current ($I_{IN} = 0$), all amplifiers are shut down and no DC path exists, except for negligible leakage. In this case, the dominant noise source is the sampled kT/C noise from the reset transistor.

Which mode the circuit works in depends on the direction of the input current. The switchover is automatic and, provided that the bandwidth and slew rate of amplifier A_1 is high enough compared to the rate of change of the input current, the switchover is smooth. Note that in actual CV or FSCV measurements, when the voltage ramp reaches its maximum value at the end of the positive ramp and starts to decrease at the onset of the negative ramp, the input current also changes rapidly from large positive values to large negative values. The current level at this polarity inversion is strong enough to support the change of V_A from a few hundred millivolt above V_{IN} to a few hundred millivolt below V_{IN}. For most cases, the oxidation peaks and reduction peaks will remain unaffected by the switchover as both peaks occur far from the switching point. Also note that the input resistances of the regulatedcascode amplifier and source-driven active-input regulatedcascode mirror are ~1/($g_{m1}A_1$) and ~1/($g_{m2}A_1$), respectively, where g_{m1}–g_{m2} are the transconductances of M_1–M_2, respectively. Because transconductance is proportional to input current, the input resistance of the potentiostat decreases as input current increases in each direction. Simulation results indicate input resistances of 290 kΩ and 588 kΩ at maximum positive and negative input current (±1.5 nA), respectively.

The source-driven topology shown in Fig. 2e was chosen for this work because it does not need compensation, unlike the conventional topology illustrated in Fig. 2d, which requires a compensation scheme that depends on the value of the input current and that becomes impractical for low input current values. Since the output of A_1 drives the low-impedance source of M_2, and since diode-connected M_2 acts as a noninverting passive device, the source-driven topology behaves as a stable single-dominant-pole system that is linear over a wide range of input currents regardless whether the transistors operate in either strong or weak inversion [24]. The activeinput regulated-cascode mirror shown in Fig. 2e was also chosen because it offers orders-of-magnitude higher output resistance (~$A_2g_{m4}r_{o4}r_{o3}$) compared to the finite output resistance (~r_{o3}) of the active-input mirror from [24], shown in Fig. 2f. In addition, the active-input regulated-cascode mirror in this work uses differential-input regulation amplifiers that are less sensitive to process and circuit parameters versus the single-input regulation amplifiers used in the regulatedcascode mirrors described in [22], [25]. The potentiostat in this work also avoids use of two separate integration stages [26], which increase the detector's real estate.

B. Timing Block

Given the large number of detectors in the array, timedivision multiplexing was implemented to reduce the number of outputs to be sampled off-chip. We limited the number of multiplexed outputs for the read-out column to 64 to avoid the use of a high-frequency on-chip clock, which would add excessive switching noise. Fig. 3 shows the timing scheme used to implement time-division multiplexing of the 64 detectors in the read-out column. Fig. 3a shows a schematic diagram of the timing block, which consists of a 64-stage shift register along with minimal combinational logic. Fig. 3b shows the corresponding timing signals produced by the timing block. The shift register is driven by two external clocks: a 640-kHz main clock, *CLK*, with 50% duty cycle and a 10-kHz shift clock, *SCLK*, with ~1% duty cycle. *SCLK* is pulsed high briefly every 100 μs. At the positive edge of the main clock, the output of the first *D* flip flop, *SEL[0]*, goes high to select the output of one of the 64

detectors in the read-out column for one period of the main clock. Consecutive positive edges of the clock activate select signals *SEL[1]* through *SEL[63]* in a sequential manner, as seen in Fig. 3b. The process is repeated with each consecutive *SCLK* pulse. A set of NAND gates is used to derive reset signals $\overline{RST}[0]$ through $\overline{RST}[63]$ to reset one detector at a time for half of a main clock period. A buffer is used to derive the clamping signal, *CLAMP*, which is fed to the CDS block in the read-out column.

C. Correlated Double Sampling Circuit

The CDS circuit depicted in the *dotted* frame in Fig. 1b operates as follows. At the end of the integration period for a particular detector, e.g., Detector 0, select signals *SEL[0]* and *CLAMP* are asserted, as shown in Fig. 3b. *SEL[0]* connects the output of Detector 0, i.e., V_{INT}, to the left plate of a 2-pF capacitor C_{CDS} via a voltage follower, while *CLAMP* grounds the right plate. Thus, the voltage across C_{CDS} at the end of the integration period is equal to V_{INT}, as described by (Equation 1). At the onset of reset, *CLAMP* is de-asserted first and $\overline{RST}[0]$ is subsequently asserted (pulsed low). During this time, the left plate of the C_{CDS} is pulled to V_{DD} while the right plate is left floating. Subtracting V_{INT}, i.e., the voltage previously stored across C_{CDS}, from V_{DD} yields

$$V_{OUT} = V_{CDS} = \frac{1}{C_{INT}} \int_0^{T_0} I_{IN}(t)dt \equiv \Delta V, \quad 2$$

where V_{OUT} and V_{CDS} are the outputs of the read-out column's common output buffer and shared CDS block, respectively, as seen in Fig. 1b, and ΔV represents the voltage step in the signal V_{OUT} shown in Fig. 3b, proportional to the input current.

IV. MEASUREMENT RESULTS

Fig. 4 illustrates a micrograph of the prototype CMOS IC that was fabricated in ON Semiconductor's 0.5-μm technology. Each potentiostat unit includes a 10 μm × 10 μm glass cut for post-CMOS surface-patterning of the polarizable electrode material, and operates within the typical electrode voltage range of −0.5 V to +1.5 V (vs. Ag|AgCl) for FSCV, at a maximum scan rate of 30 V/s. The area of each potentiostat is 45 μm × 30 μm. The entire system occupies an active area of 276 μm × 1110 μm (excluding pads), and draws 970 μA from a 5-V supply, yielding a total power consumption of 4.85 mW. The heat generated by the chip could be a potential problem for neuron activities [27] and therefore the power budget of the circuit should be carefully examined. The duration of a typical on-chip recording is <10 min. During this time there was no detectable change of temperature in the sample. The sample temperature increased by 0.4 °C within 1 hr of chip operation (measured with a type K thermocouple thermometer, *Test Products International Inc., OR*). The power is thus low enough to avoid significant heating of the sample even over extended recording times. At zero input current, the RMS noise is 443 fA at 10-kHz bandwidth, which is comparable with the RMS noise of 580 fA at 10-kHz bandwidth for a *HEKA EPC10* patch clamp amplifier in medium gain range. For larger positive and negative input currents the maximum RMS noise increases somewhat up to <1 pA and <2 pA, respectively. Fig. 5

shows the measurement setup used for the device characterization and validation experiments, which were carried out inside a grounded Faraday cage to minimize electrical interference. The sampling rate was limited to 10 kHz by the external A/D converter's input capacitance (100 pF) and the connecting cable's load capacitance (37.5 pF).

Table II summarizes the measured performance of the fabricated chip. Table III compares the performance of the chip against that of recently published voltammetric detector arrays. Notably the chip presented here features orders of magnitude smaller detector footprint compared to previous work. The small area of the working electrode enables a reduced double layer capacitance at the electrode-solution interface, and therefore a decreased background current. The advantage is that with a small background current, the maximum input range required is much smaller compared to previous work with large detector area, and the RMS noise is also reduced by orders of magnitude. In a real CV or FSCV measurement from live cells, the amounts of neurotransmitters released from individual vesicles are very small (10^4–10^7 molecules) [32], and therefore minimal noise is critical for identifying activity from the cells. The small RMS noise enables on-chip amperometry measurements which typically have peak currents of 1–100 pA [32]. The chip presented in this work also has the potential of performing simultaneous amperometry and FSCV measurements, which can provide more detailed and precise information about cell exocytosis events.

A. Device Characterization

To test the static linearity of the potentiostat, the input current was linearly swept in the range of ±1.5 nA in steps of 10 pA using a *Keithley 236* DC current source. Fig. 6 shows the measured output current for positive and negative input currents ranging from 10 pA to 1.5 nA.

B. Device Validation

The chip is intended for cyclic voltammetry measurements with on-chip electrodes. Since it was not possible to connect external electrodes to the on-chip contacts, a separate 30-V/s FSCV recording with a CFM was performed to generate a realistic voltammetry current waveform that was used to validate bidirectional current detection with a fabricated chip. CFMs were fabricated from 5-μm diameter carbon fibers as described in [33]. The tip of the carbon fiber was entirely coated with wax and then cut such that only the circular area at the end of the cut fiber was exposed as the working electrode. The area of such a CFM is similar to that of onchip electrodes after post-fabrication [11], [13], which also will be fabricated in the future on the FSCV chip described here. The CFM was immersed into a petri dish filled with a buffer solution containing 140 mM NaCl, 5 mM KCl, 5 mM $CaCl_2$, 1 mM $MgCl_2$, and 10 mM HEPES/NaOH pH 7.3. The electrode potential was swept linearly from −0.45 V to +1.0 V over 50 ms, and back to −0.45 V over the next 50 ms. At the start of the recording, buffer solution supplemented with 1-μM dopamine (DA) was flowed through the dish to replace the DA-free buffer. After two minutes of recording, DA-free buffer was flowed into the dish to replace the DAcontaining buffer. The CFM currents recorded during flow of the DA-free and DA-containing buffer are depicted by the *solid gray* traces in Figs. 7a–7b, respectively. The slower scan rate, compared to the standard 300-V/s FSCV, was chosen to

limit the current amplitude to <1.5 nA, the input range of the on-chip detectors. However, the 30-V/s scan rate is sufficient for on-chip electrode characterization. The main component of the recorded currents is the capacitive background current (Fig. 7a), which changes only slightly due to the additional *faradaic* DA current (Fig. 7b). This background is due to the ionic double layer capacitance between the electrode surface and the buffer solution, and is roughly proportional to the scan rate [34].

The prerecorded input current was fed to the on-chip detectors through B_P and B_N in Fig. 2a as follows. To avoid excessive capacitive loading from the long cables connecting the *Keithley 236* DC current source to the chip, a voltage waveform was applied directly to the diode-connected transistors in each current mirror using discrete components on a custom board with negligible stray capacitance. The applied voltage waveform was calculated from the desired input current waveform based on *I-V* curves that were obtained for the diode-connected transistors. Positive and negative prerecorded CFM data were applied via B_P and B_N, respectively. The voltage ramp applied to V_{IN} in Fig. 2a was set to the same voltage ramp used in the 30-V/s FSCV CFM recording. Although a capacitance will form at the electrode-air interface, the resulting current can be safely neglected as the capacitance is extremely small (in contrast to the large capacitance between the electrode and buffer solution). The output of the detector was directly connected to a *NI PXIe-6368* external A/D converter.

The *solid black* traces depicted in Figs. 7a–7b represent the measured output current of a single detector during flow of the DA-free and DA-containing buffer, respectively. It is evident from these traces that the potentiostat in Fig. 2a does not provide the input current directly but rather provides the absolute value of the current due to the use of the same integration capacitor for both positive and negative input currents. To recover the original input current, sign inversion of the negative values of the current was performed offline as follows. First, the zero-crossings of the measured output currents were identified at around t = 53 ms as evidenced by the V-shaped sharp turn of the traces at around this time. Second, *a priori* knowledge of the shape of the current expected for FSCV was used to confirm that only the values to the right of the zero crossings were the ones that needed sign inversion. The *dashed black* traces in Figs. 7a–7b represent the corrected output current during flow of the DA-free and DA-containing buffer, respectively. In both cases, the output current after offline sign-inversion of the negative data matches accurately the prerecorded input current. Plotting output current as a function of applied voltage yields the voltammograms shown in Fig. 7c, obtained during flow of the DA-free (*gray* background trace) and DA-containing (*black* trace) buffer. The *black* trace in Fig. 7d represents the corresponding background-subtracted difference voltammogram. The peaks near +0.25 V and −0.15 V (vs. Ag|AgCl) correspond to dopamine oxidation and reduction, respectively. In these test measurements, voltage and current were applied simultaneously to all of the 64 detectors, and the outputs from all 64 detectors were recorded simultaneously. The *gray* traces in Fig. 7d show the superimposed difference voltammograms from all 64 detectors.

One potential application of cyclic voltammetry would be in the identification of specific transmitters released from individual cells. To resolve cyclic voltammograms during rapidly changing concentrations, as occurs during stimulated release from cells that will be cultured

on the chip, a 30-V/s scan rate may be insufficient and should be increased to at least 300 V/s. Due to the 10× higher voltage scan rate, and thus ~10× larger background current, an electrode capacitance of ~20 pF is estimated assuming an electrode area of 64 μm^2, yielding a background current of ±6 nA for a 300-V/s scan rate. Using ADCs with ultra-small input capacitance for data acquisition, it should possible to increase the sampling rate to 40 kS/s with a reliable output, decreasing the integration time to 25 μs and thus increasing the input current range to ±6 nA. One possibility would be to integrate on-chip ADCs as has been demonstrated for an amperometric front-end chip [35]. For a further reduction in gain, the integration capacitor C_{INT} could be increased to hold more charge during measurement, leading to a lower gain and allowing higher scan rates.

V. DISCUSSION

As mentioned previously in Section IV, the bidirectionalcurrent detector does not measure input currents directly but provides the absolute value instead due to the use of the same integration stage for both negative and positive currents. In the present design, the negative currents were recovered via offline sign inversion. The process was effective given that an identical input current was applied to all of the detectors in the read-out column during measurement. In reality, the input current will vary considerably from detector to detector during actual *in vitro* measurements. Thus, offline sign inversion becomes impractical for analyzing measurements from all of the 64 detectors in this array. In this case, implementing a zero-crossing detection algorithm using the rules described in Section IV becomes necessary, although not sufficient because the algorithm could miss, in principle, some crossings in the presence of noise. A more robust approach to solve this issue involves generating a binary output signal that reflects the sign of the input current in each detector.

One such implementation, which requires only a minor modification to the existing circuitry, leverages the fact that the output of the regulation amplifier A_1 in Fig. 2a, i.e., node V_A, is pulled several hundred millivolts higher and lower than the applied voltage V_{IN} for positive and negative input currents, respectively, as illustrated in Fig. 8a. Fig. 9a shows the proposed modification for generating the binary output signal *SIGN* depicted in Fig. 8b. The technique takes advantage of the same time-division multiplexing and sharedamplifier schemes described in Section II. When the select signal for a particular detector, e.g., Detector 0, goes high for one period of the main clock, a comparator shared by all detectors in a read-out column, compares V_{IN} versus the V_A node of that particular detector. Fig. 9b shows a simplified schematic diagram of the shared comparator, which operates as follows. For negative input currents, V_A becomes lower than V_{IN} and all of the bias current flows into the detector through M_{10} and M_{12}. Thus, the drain voltage of M_{14} is pulled to V_{DD}, which forces the digital output signal *SIGN* to go low (Fig. 8b). Similarly, for positive input currents, V_A becomes higher than V_{IN} and all of the bias current flows instead through M_{11} into the common current mirror formed by M_{13}–M_{14}. Thus, the drain voltage of M_9 is pulled to ground instead, which forces the *SIGN* to go high (Fig. 8b). The proposed scheme only requires two additional transistors, i.e., M_{10} and M_{12}, and an extra read-out line per detector, yielding a negligible increase in detector area.

VI. CONCLUSION

In this work, we presented a new CMOS potentiostat circuit topology for application of bipolar voltages and high precision measurements of bidirectional currents. We also introduced a scalable CMOS VLSI potentiostat array for high-throughput drug screening applications. The proposed circuit enables not only amperometry but also FSCV at a MEA for massivelyparallel detection of quantal release events and characterization of electrode impedance, respectively. We demonstrated system functionality through device validation using prerecorded input stimuli. We discussed the potentiostat's inability to detect the sign of the current, established a methodology for recovering the negative values of the current via a sign inversion procedure, and suggested a minor circuit modification to capture the sign of the current via a binary output signal with minimal area overhead. Ongoing work includes the design and validation of a 16 × 64 FSCV detector array, composed of 16 parallel readout columns, with post-CMOS surface-patterned electrodes for on-chip cell recordings.

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Biography

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In 2003, Dr. Lindau was elected as a Member of the Asian Institute of NanoBioScience and Technology. That same year, he received a Research Award from the Alexander von Humboldt Foundation, Germany, in recognition of his scientific achievements. In 2018, he received the Sir Bernard Katz Award from the Biophysical Society Exocytosis and Endocytosis Subgroup, in recognition of his outstanding contributions as a leader and scientist in the areas of exocytosis and endocytosis. He is a member of the Biophysical Society and the Society for Neuroscience.

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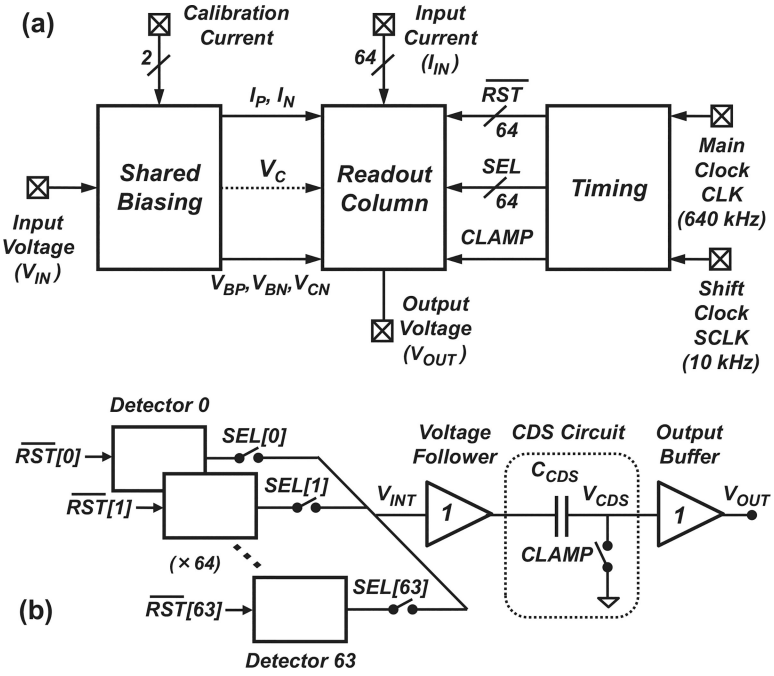

Fig. 1.

System-level diagram of the FSCV detector array. (a) The system consists of a read-out column along with on-chip biasing and timing blocks. (b) The read-out column contains 64 detectors that share a common output stage consisting of a correlated double sampling (CDS) circuit and an output buffer. Detectors are switched sequentially using time-division multiplexing.

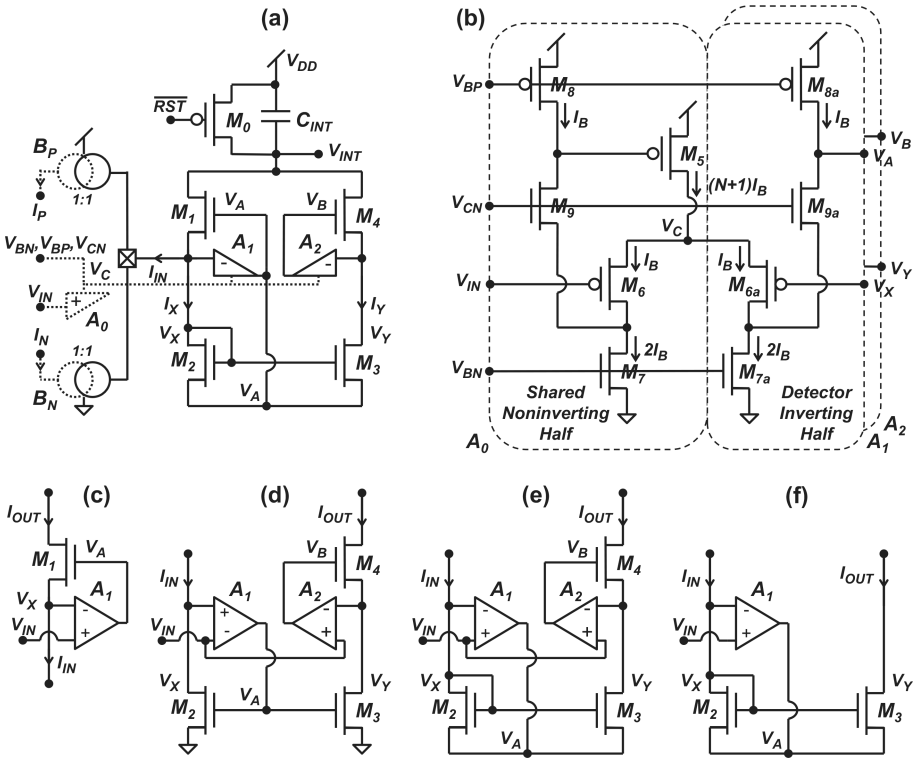

Fig. 2.

Schematic diagrams of the (a) bidirectional-current potentiostat unit implemented in this work, (b) shared half amplifier scheme from [14], (c) regulatedcascode amplifier from [14], (d) conventional active-input regulated-cascode mirror from [23], (e) source-driven active-input regulated-cascode mirror from [23], and (f) source-driven active-input current mirror from [24].

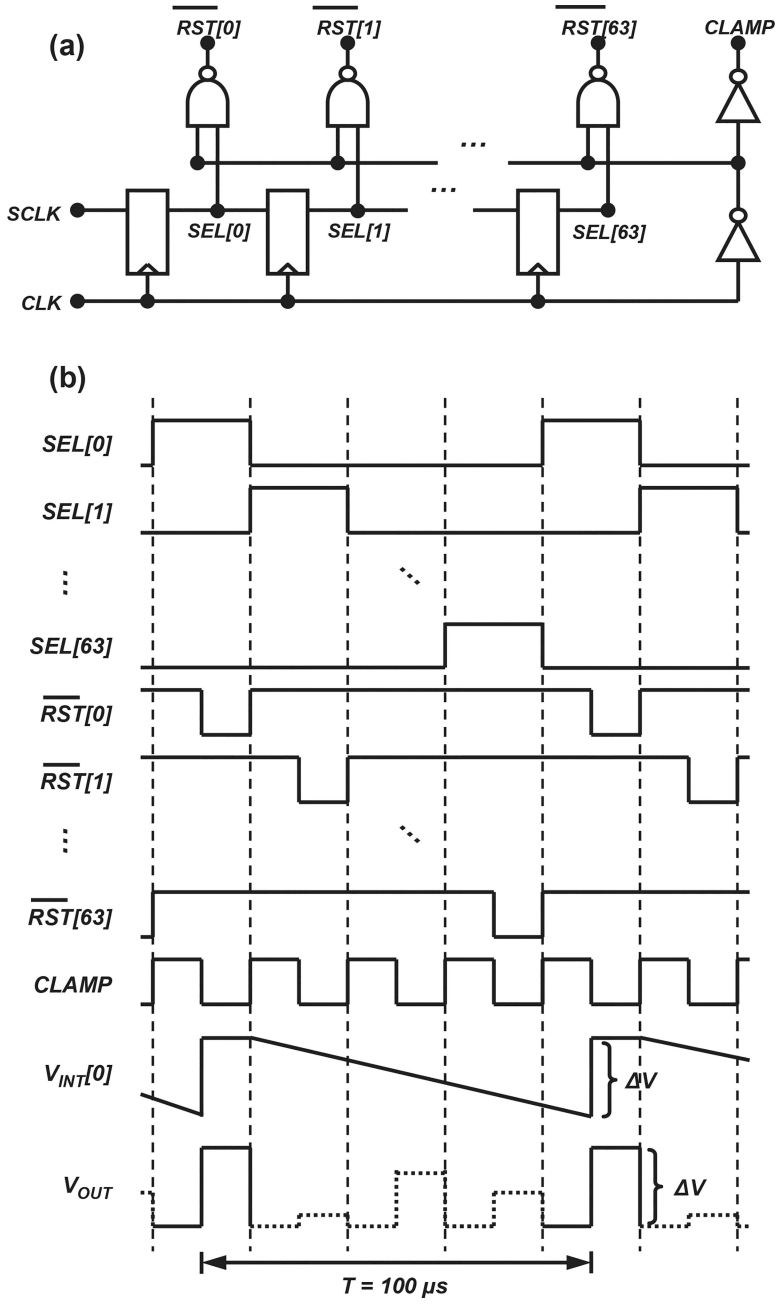

Fig. 3.

Timing scheme used to implement time-division multiplexing in the read-out column: (a) timing circuit and (b) timing signals.

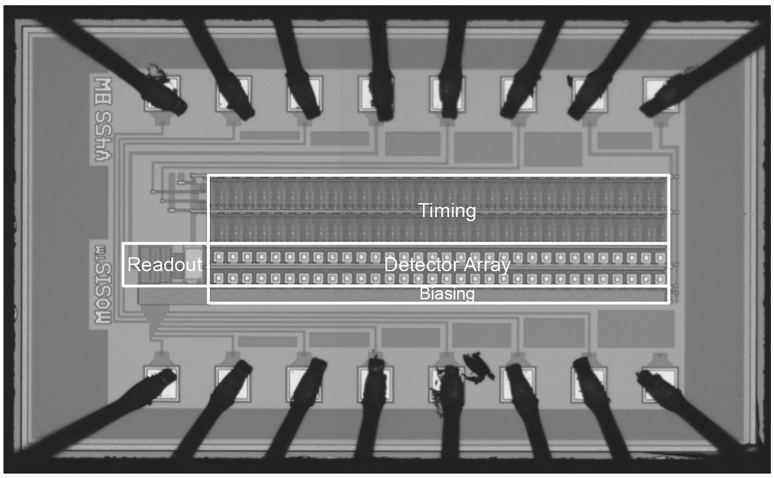

Fig. 4.
Micrograph of the fabricated prototype FSCV detector array IC.

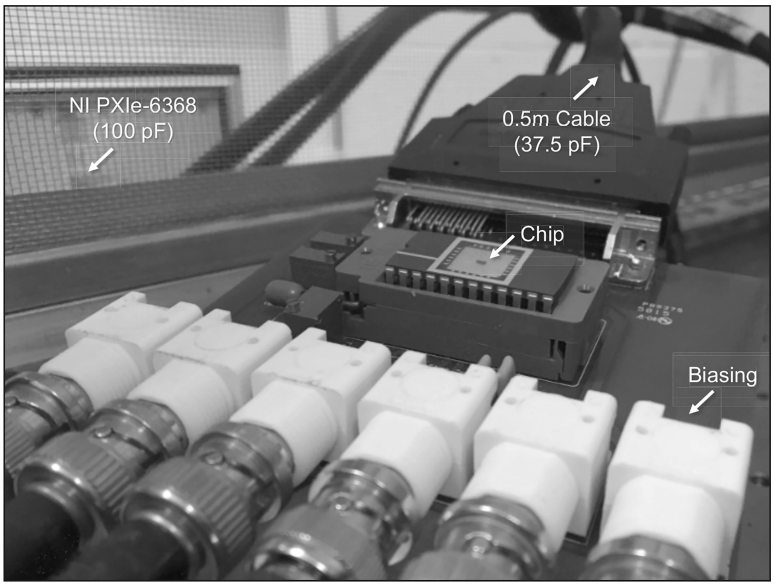

Fig. 5.
Measurement setup used for device characterization and validation.

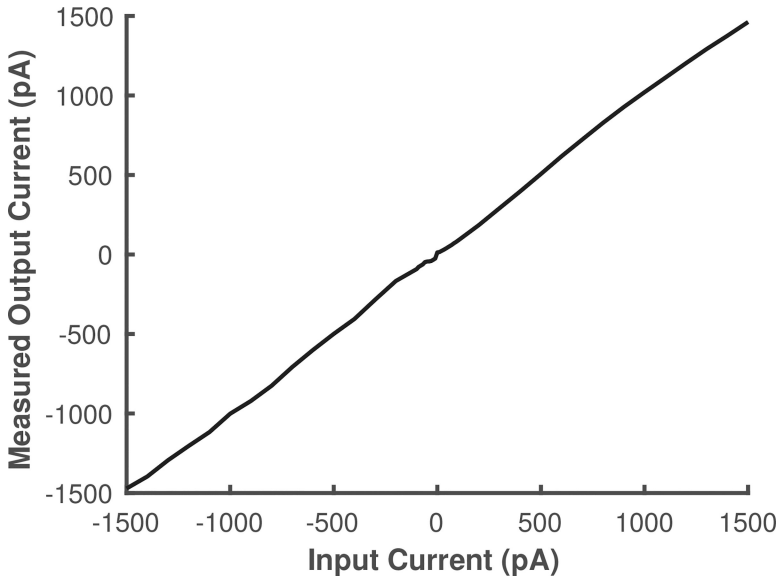

Fig. 6.

Measured static linearity of the potentiostat circuit for negative and positive input currents in the range of 10 pA to 1.5 nA.

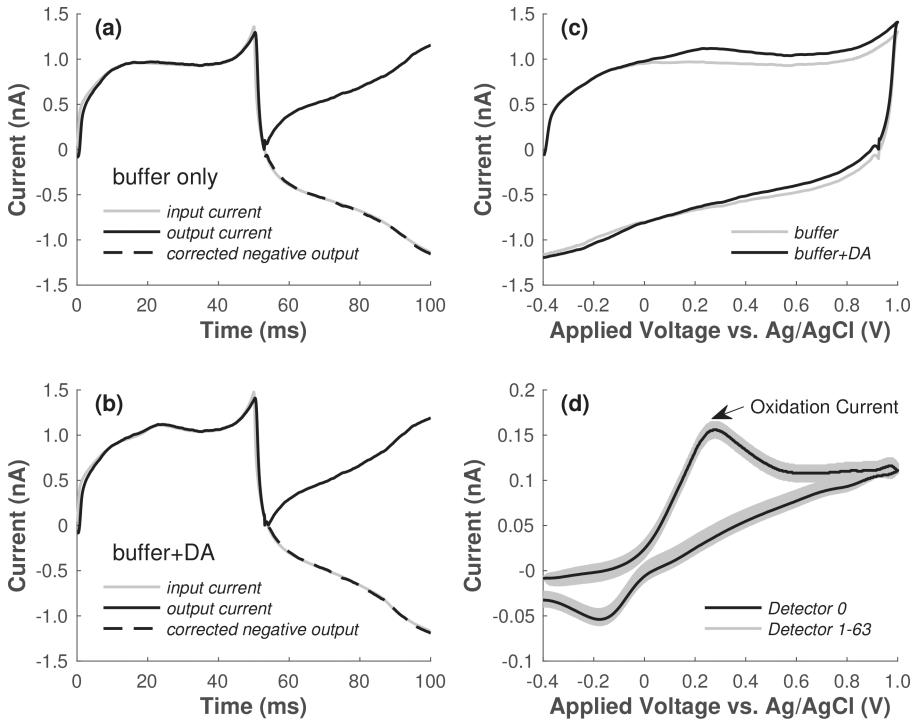

Fig. 7.

(a) Prerecorded input current (*solid gray* trace) during flow of the dopamine-free buffer, and measured output current before (*solid black* trace) and after (*dashed black* trace) offline sign-inversion of the negative data. (b) Prerecorded input current (*solid gray* trace) during flow of the dopamine-containing buffer, and measured output current before (*solid black* trace) and after (*dashed black* trace) offline sign-inversion of the negative data. (c) Measured background voltammograms during flow of the dopamine-free (*gray* trace) and dopamine-containing buffer (*black* trace). (d) Measured superimposed background-subtracted cyclic voltammograms for all of the 64 detectors.

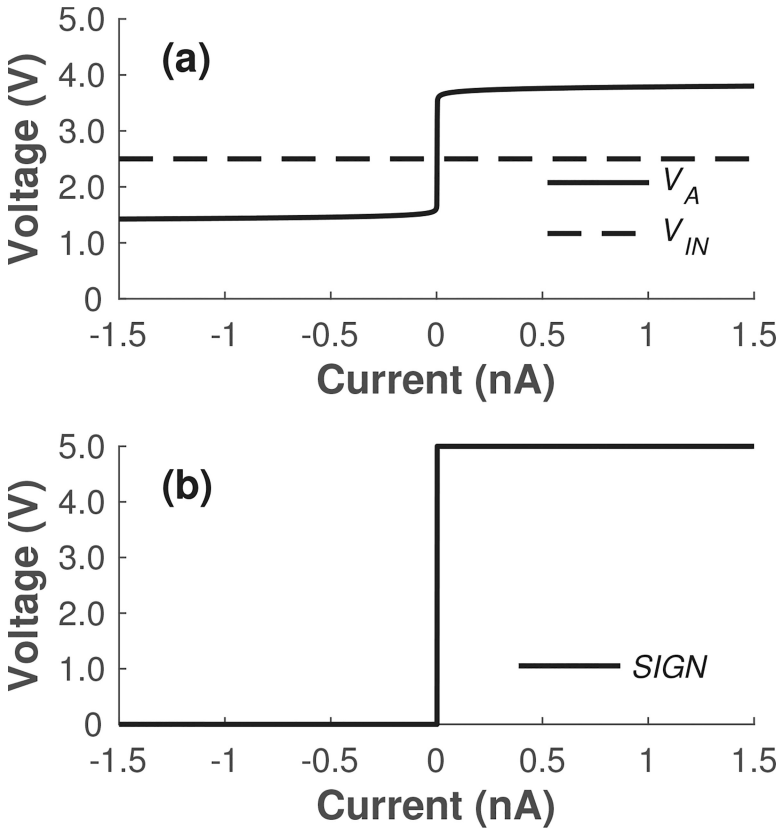

Fig. 8.

Simulation results illustrating the signals used to generate a binary output signal corresponding to the sign of the current. (a) The output of the regulation amplifier A_1 in Fig. 2a, i.e., node V_A, is pulled several hundred millivolts higher and lower than the applied voltage V_{IN} for positive and negative input currents, respectively. (b) The two signals in (a) can be fed to the comparator in Fig. 9 to generate the desired binary output signal *SIGN*.

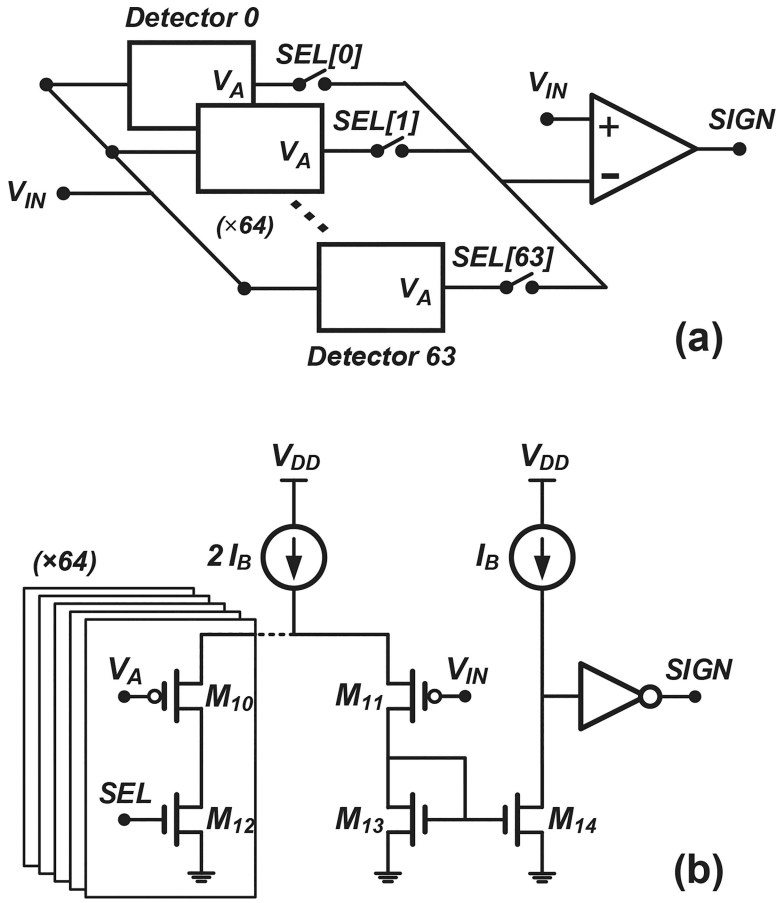

Fig. 9.

(a) Proposed modification to each read-out column in the array to generate a binary output signal corresponding to the sign of the input current. (b) Proposed implementation of the shared comparator shown in (a). The proposed solution only adds two additional transistors and a read-out line per detector for a negligible increase in detector area.

Table I

DETECTOR DESIGN VALUES

Device	Type	W (μm)	L (μm)	Voltage	Value (V)
M_0	PMOS	1.2	0.6	V_{BN}	1.0
M_1–M_4	NMOS	3	3	V_{BP}	3.7
M_5	PMOS	6·(N+1)	3	V_{CN}	1.3
M_6, M_{6a}	PMOS	6	3	V_{CN}	1.0–2.5
M_7, M_{7a}	NMOS	6	3	**Capacitor**	**Value**
M_8, M_{8a}	PMOS	3	3	C_{INT}	50 fF
M_9, M_{9a}	NMOS	3	3	C_{CDS}	2 pF

Table II

SUMMARY OF MEASURED PERFORMANCE

Conversion Rate	10 kS/s
Input Current Range	±1.5 nA
Input RMS Noise	443 fA (10-kHz BW)
Detector Pixel Power	13.5 μW
Detector Array Power	0.97 mW
Readout Stage Power	1.80 mW
Timing Block Power	0.95 mW
Shared Biasing Power	1.13 mW
Total Chip Power	4.85 mW
Detector Pixel Area	45 μm × 30 μm
Total Chip Area*	276 μm × 1110 μm
Supply Voltage	5.0 V
Process	0.5-μm CMOS

* includes 64-detector array plus readout, timing, and biasing overhead

Table III

PERFORMANCE COMPARISON OF VOLTAMMETRIC DETECTOR ARRAYS

	This work	**[27]**	**[28]**	**[29]**	**[30]**	**[31]**
Process (μm)	**0.5**	0.5	0.35	0.35	0.18	0.065
Supply Voltage (V)	**5.0**	5.0	3.3	3.3	1.8	1.8
Pixel Count	**64**	100	1,024	1	200	4
Pixel Power (μW)	**13.5**	21	–	9,300	12.1	36
Pixel Area (mm^2)	**0.001**	0.06	0.01	0.6	0.03	0.045
RMS Noise (pA)	**0.443**†	7.2	0.540	120‡	0.480	50
Bandwidth (kHz)	**10**	11.5	0.13	7	0.110	10
Input Range (nA)	**±1.5**	±110	±1	±300	±0.2	±2,560
Sweep Rate (V/s)	**30**	0.04	0.1	0.095	2.8	400
Cyclic Voltammetry	**Yes**	Yes	Yes	Yes	Yes	Yes
Amperometry	**Yes**	–	–	Yes	Yes	–

†open-input measurement

‡calculated from given information