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High electrical conductivity and carrier mobility in oCVD PEDOT thin films by engineered crystallization and acid treatment

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Air-stable, lightweight, and electrically conductive polymers are highly desired as the electrodes for next-generation electronic devices. However, the low electrical conductivity and low carrier mobility of polymers are the key bottle-necks that limit their adoption. We demonstrate that the key to addressing these limitations is to molecularly engineer the crystallization and morphology of polymers. We use oxidative chemical vapor deposition (oCVD) and hydrobromic acid treatment as an effective tool to achieve such engineering for conducting polymer poly(3,4-ethylenedioxythiophene) (PEDOT). We demonstrate PEDOT thin films with a record-high electrical conductivity of 6259 S/cm and a remarkably high carrier mobility of 18.45 cm² V⁻¹ s⁻¹ by inducing a crystallite-configuration transition using oCVD. Subsequent theoretical modeling reveals a metallic nature and an effective reduction of the carrier transport energy barrier between crystallized domains in these thin films. To validate this metallic nature, we successfully fabricate PEDOT-Si Schottky diode arrays operating at 13.56 MHz for radio frequency identification (RFID) readers, demonstrating wafer-scale fabrication compatible with conventional complementary metal-oxide semiconductor (CMOS) technology. The oCVD PEDOT thin films with ultrahigh electrical conductivity and high carrier mobility show great promise for novel high-speed organic electronics with low energy consumption and better charge carrier transport.

INTRODUCTION

The rapid development of electronics and optoelectronics induces enormous demand for scalable and transparent electrodes, which are crucial for better human-device interface (1, 2) and better lightmatter interaction (3). Air-stable conducting polymers, especially poly(3,4-ethylenedioxythiophene) (PEDOT), are among the most promising candidates in this field, providing key advantages over their inorganic counterparts, such as low cost, lightweight, material abundance, and excellent biocompatibility. As a result, PEDOT holds great prospect for various applications, such as solar cells (4), optical displays (5), organic light-emitting diodes (6), and sensors (7). However, the electrical conductivity and carrier mobility of PEDOT are still far below conventional inorganic conductors, resulting in higher power consumption and lower operational speed. To address this limitation, improvements in the electrical conductivity and carrier mobility are highly desired.

On the basis of the Drude model (8, 9), the strategy to achieve high electrical conductivity requires realization of high carrier mobility and high carrier density. However, it is very difficult to maintain high carrier mobility simultaneously with high carrier density in PEDOT because of the ionized impurity scattering induced by the increased dopant counteranions, which occurs at high doping levels (5). Research efforts to improve the electrical conductivity of PEDOT have been mainly divided into two categories: enhancing carrier mobility and enhancing carrier

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density. Typically, the carrier mobility for organic semiconductors and conductors is on the order of $\sim 10^{-5}$ to 10 cm² V⁻¹ s⁻¹ and is highly dependent on crystallinity (10, 11). The carrier mobility of PEDOT can be increased by annealing at elevated temperature (5), sulfuric acid treatment (12), cosolvent engineering (13), doping anion engineering (14, 15), and other methods, mainly to enhance the alignment and crystallization of PEDOT films. For example, Lee et al. (5) reported mobility as high as 33.6 cm² V⁻¹ s⁻¹ using elevated temperature annealing. However, using this method, carrier density was significantly sacrificed, and therefore, overall conductivity was only 592 S/cm. On the other hand, researchers have also investigated the enhancement of charge carrier density through oxidation-level engineering (16-18). However, impurity scattering induced by the dopant counter-anions will decrease carrier mobility (5, 19) and result in a limited enhancement in electrical conductivity. Therefore, it is important to find a balance between obtaining high carrier density and high carrier mobility to optimize the conductivity. The key is to molecularly engineer the crystallization at high doping level to maintain high mobility. For example, single-crystal PEDOT nanowires have achieved electrical conductivity up to 8797 S/cm (8); however, this level of conductivity has not been achieved in the thinfilm geometries desired for most electronic devices.

Here, we successfully synthesize highly conductive and wafer-scale PEDOT thin films through an oxidative chemical vapor deposition (oCVD) approach and postdeposition hydrobromic acid (HBr) treatment. The oCVD method provides control over crystallization and morphology, which leads to enhancement of carrier mobility at high carrier density. Unlike the solution-based processes with concerns of substrate compatibility, oCVD is a vapor-phase and substrate-independent technology enabling large-scale synthesis of high-quality conjugated polymer thin films (20). By introducing monomer [for example, 3,4-ethylenedioxythiophene (EDOT)] and oxidant (here, FeCl₃) simultaneously, the oxidant not only initiates the step-growth polymerization but also heavily dopes the polymer chains in an in situ manner (with a typical carrier density of ~ 10^{21} cm⁻³) (20). Here, we introduce a temperature-controlling method to finely tune

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Fig. 1. The crystallization-orientation transition induced by engineered deposition temperature and film thickness. (**A**) Schematic representation of the face-on stacking in the ultrathin films (left) and the edge-on stacking in the thick films (right). (**B**) Schematic showing high crystallinity is induced by high deposition temperature in the face-on regime. The chemical structure of PEDOT is shown on the right. (**C**) Room temperature XRD maps (θ -2 θ) of 10-nm PEDOT thin film deposited at 300°C (left) [the inset is the schematic of the face-on stacking (0k0)], 248-nm PEDOT thin film deposited at 190°C (middle) [the inset is the schematic of the edge-on stacking (0k0)], and 23-nm PEDOT thin film deposited at 300°C (right). a.u., arbitrary units. (**D**) Room temperature XRD pattern for face-on samples deposited at different substrate temperatures. Note that the peak intensity is increasing as the deposition temperature increases. The deposition temperature and the film thickness are included in the figure. (**E**) Bar chart summarizing the room temperature XRD results. The length of each bar is the normalized integrated intensity of the edge-on (red) or face-on (blue) stacking peak. Here, to visualize the intensity of both kinds of peaks together, we normalize the peak intensity by converting the edge-on intensity (at 2 θ ~ 6.5°) to equivalent face-on intensity (at 2 θ ~ 26°) using the Lorentz-polarization factor. In the face-on regime, the crystallinity (closely related to the normalized intensity) increases markedly with increasing deposition temperature.

the crystallization orientation of PEDOT polymer chains in the oCVD polymerization process. Combined with film thickness engineering, our technique can effectively induce crystallization transition from "edge-on" (Fig. 1A, right) to "face-on" orientation (Fig. 1A, left) and significantly reduces the energy barrier of intercrystallite carrier transport in a confined layer, which is the key to enhance the carrier mobility. In the face-on regime, it is also observed that increasing the growth temperature increases the crystallinity (Fig. 1B) and therefore further enhances carrier mobility. We successfully achieved a record-high electrical conductivity of 6259 S/cm and a remarkably high carrier mobility of 18.45 cm² V⁻¹ s⁻¹ in this manner. Subsequent thermoelectric measurements and temperature-

dependent charge carrier transport measurements, together with the Kang-Snyder (K-S) model, reveal the metallic nature of face-on oCVD PEDOT and validate an effective reduction of transport energy barrier between crystallized domains.

RESULTS AND DISCUSSION

The PEDOT samples are synthesized using the oCVD method at substrate temperatures ranging from 150° to 300°C, followed by HBr treatment. Experimental details can be found in section S1 and fig. S1. Using x-ray diffraction (XRD), we observe that the crystallization-orientation transition from edge-on to face-on is induced by decreased film thickness and increased deposition temperature. Figure 1C shows the XRD results of PEDOT thin films deposited at 300°C (left, 10 nm thick), 190°C (middle, 248 nm thick), and 300°C (right, 23 nm thick). The XRD peak (21, 22) at $2\theta \sim 6.5^{\circ}$ corresponds to an edge-on stacking orientation (h00) with the lattice spacing d = 1.36 nm in Fig. 1C (middle), while the peak at $2\theta \sim 26^{\circ}$ corresponds to the face-on stacking orientation (0k0) with d = 0.34 nm in Fig. 1C (left) (21, 22). The schematics of both stacking orientations can be found in Fig. 1C (12, 22). Compared with the 10-nm sample deposited at 300°C, the 23-nm sample deposited at the same temperature shows an emerging edge-on peak in addition to the dominating face-on peak as shown in Fig. 1C (right). Figure 1D shows the XRD results for face-on samples deposited at different temperatures, demonstrating an increasing peak intensity as deposition temperature increases. Furthermore, a summary of the crystallization orientation and integrated XRD peak intensity of oCVD PEDOT thin films is shown in Fig. 1E (the original XRD patterns can be found in fig. S5, and the peak data can be found in table S1), with the length of the bars denoting the integrated XRD peak intensity, which is closely related to the crystallinity (23, 24). The face-on stacking is shown in blue, and the edge-on stacking is shown in red. Here, to visualize the intensity of both kinds of peaks together, we convert the edge-on intensity (at $2\theta \sim$ 6.5°) to equivalent face-on intensity (at $2\theta \sim 26^{\circ}$) using the Lorentzpolarization factor (23) (a detailed discussion can be found in section S2). Figure 1E can be divided into the edge-on region (red) and the face-on region (blue), showing that the formation of face-on stacking strongly favors the synthesis conditions of (i) low film thickness and (ii) high deposition temperature. For example, with the same deposition temperature of 250°C, the 222-nm-thick film has preferential edge-on stacking, while the 11-nm-thick film is purely face-on (Fig. 1E and fig. S5). This thickness dependence phenomenon can be explained by the confinement effect in the ultrathin films. The crystallite size of the PEDOT film is calculated on the basis of the Scherrer equation (22, 25) (detailed crystalline domain sizes can be found in table S2): The stacking length along the stacking direction is ~6.8 nm for edge-on stacking and ~3.2 nm for face-on stacking. For a film thickness of ~10 nm, the large edge-on stacking with a dimension of ~6.8 nm is more difficult to accommodate than the more compact face-on stacking with a dimension of ~3.2 nm. Furthermore, high deposition temperature is also essential for the formation of face-on stacking. The 34-nm film deposited at 150°C still has dominating edge-on stacking, while the 23-nm film grown at 300°C (Fig. 1C, right) shows minor edge-on stacking with dominating face-on stacking. The mechanism for the crystallization-orientation transition associated with thickness and growth temperature may be related to the energy minimization in confined layers during the crystallization process. A detailed discussion can be found in sections S2 and S9. In addition, the integrated XRD peak intensity monotonically increases with the deposition temperature increasing in the face-on regime, as shown in Fig. 1E, indicating a larger crystallinity (23, 24), or a larger portion of crystallized region, which is beneficial for improved electrical conductivity.

The room temperature in-plane electrical conductivity of PEDOT samples with different crystallization orientations and different deposition temperatures is shown in Fig. 2A. The room temperature conductivity increases as the deposition temperature increases over the range of 150° to 300°C. The face-on films (as shown in Fig. 1, D and E) exhibit much higher electrical conductivity than the edge-on films. The highest electrical conductivity is 6259 ± 1468 S/cm, achieved in the face-on PEDOT thin films deposited at 300°C. We also benchmark our result with previous record values reported in the literature (Fig. 2B) (*12, 14, 26, 27*) and demonstrate a new record for the electrical conductivity of PEDOT thin films. This high electrical conductivity is accompanied with a marked surface morphology change induced by the crystallization-orientation



Fig. 2. In-plane electrical conductivity of oCVD PEDOT thin films. (A) Room temperature electrical conductivity of oCVD PEDOT thin films with face-on and edge-on stacking. The error bar is the 95% confidence interval by seven independent measurements among one typical batch. (B) Comparison between the results from this work with benchmarks. (C) Temperature-dependent electrical conductivity for oCVD PEDOT samples. (D) Zabrodskii plot showing a metallic nature of the PEDOT samples.

transition and crystallinity increase. The morphology change of the oCVD PEDOT thin films can be found in the atomic force microscopy (AFM) images in fig. S6. A detailed discussion can be found in section S2. In addition, the thermal stability study, Raman and attenuated total reflection (ATR) Fourier transform infrared (FTIR) spectra, and x-ray photoelectron spectroscopy (XPS) results of the oCVD PEDOT samples can be found in sections S3 and S4. The influence of film thickness on electrical conductivity and batch reproducibility are studied in section S5.

To further understand the charge carrier transport, we conducted cryogenic electrical conductivity measurement, as shown in Fig. 2C and section S1. The temperature-activated conductivity shown in Fig. 2C is a result of the disorder region between crystallites (9, 10, 28). On the basis of the extent of disorder and the doping level (18) in conducting polymers, there are three transport regimes: metal, insulator, and the critical regime. To identify the transport regime of conducting polymers, the Zabrodskii plot (18) is generated by defining the quantity W

$$W = -T \left[\frac{d \ln \rho(T)}{dT} \right] = \frac{d \ln \sigma(T)}{d \ln T}$$
(1)

where σ is the electrical conductivity, ρ is the electrical resistivity, and *T* is the temperature. The log-log plot of *W* versus *T* (Zabrodskii plot) is very sensitive to the metal-insulator transition. With a positive slope at the low-temperature region (*18*), the Zabrodskii plot of the oCVD PEDOT thin films shown in Fig. 2D reveals a metallic nature.

Induced by the crystallization-orientation transition and elevated deposition temperature, the enhancement in the electrical conductivity can be explained by improved carrier mobility or improved carrier density. Seebeck coefficient and work function measurements indicate that the carrier density does not vary significantly among PEDOT thin films of different crystallization orientations and crystallinities. It is well known that the Seebeck coefficient of a material is highly related to its carrier density: Usually, Seebeck coefficients decay with increasing carrier density (9, 16) in the same material. Figure 3A shows the Seebeck coefficient measured on edge-on and face-on oCVD PEDOT thin films deposited at different temperatures (measurement method in section S1). The Seebeck coefficients all lie at ~11 ± 1 μ V/K, with little variance within the measurement error. Therefore, it is indicated that the carrier density does not change significantly among the samples. Consistent with the result of the Seebeck coefficients, the work functions of the samples also lie at ~5.33 ± 0.04 eV (Fig. 3A) with little variance, indicating that the carrier density does not vary significantly among the samples (29). Therefore, we hypothesize that the much enhanced carrier mobility is the key to the enhanced electrical conductivity.

We use the K-S model (9) to obtain a more profound understanding of the charge carrier transport process. The key equations from the K-S model are

$$\sigma = \sigma_{\rm E0}(T) \times sF_{s-1}(\eta) \tag{2}$$

$$S = \frac{k_{\rm B}}{e} \left[\frac{(s+1)F_s(\eta)}{sF_{s-1}(\eta)} - \eta \right]$$
(3)

with the nonnormalized complete Fermi-Dirac integral

$$F_{i}(\eta) = \int_{0}^{\infty} \frac{\varepsilon^{i}}{1 + e^{\varepsilon \cdot \eta}} d\varepsilon$$
(4)



Fig. 3. Theoretical modeling to study the charge carrier transport process in oCVD PEDOT. (**A**) Left *y* axis: Work function of oCVD PEDOT samples deposited at different temperatures. Right *y* axis: Room temperature Seebeck coefficient of the PEDOT samples. (**B**) Calculated transport coefficient σ_{E0} at 300 K. (**C**) Calculated room temperature carrier mobility of face-on samples deposited at different temperatures and Hall effect–measured carrier mobility. The error bar is based on three samples. (**D**) Calculated carrier mobility as a function of measurement temperature and fitted energy barrier W_{γ} of intercrystallite charge carrier transport.

where σ denotes the electrical conductivity and *S* denotes the Seebeck coefficient. Transport coefficient $\sigma_{E0}(T)$ is a temperature-dependent but energy-independent parameter, which is related to the transport function (9). *s* is an integer characterizing the polymeric system. For PEDOT (9), *s* = 1 (discussions can be found in section S1). The reduced chemical potential $\eta = (E_F - E_t)/k_BT$, where E_F is the Fermi level and E_t is the transport edge with the unit of energy (for details, see section S1). k_B is the Boltzmann constant, and *T* is the temperature. *e* in Eq. 3 is the elementary charge, and *e* in Eq. 4 is the mathematical constant (Euler's number). ε in Eq. 4 is the variable of the integration used to define the mathematical form of $F_i(\eta)$. ε does not have a physical meaning.

High transport coefficient σ_{E0} indicates a much enhanced carrier mobility in the face-on oCVD PEDOT thin films. From the K-S model, $\sigma_{\rm E0}(T)$ is a temperature-dependent parameter characterizing the carrier mobility (9). Figure 3B shows room temperature σ_{E0} calculated using Seebeck coefficient and electrical conductivity with Eqs. 2 and 3 (details can be found in sections S1 and S10). As observed in Fig. 3B, room temperature σ_{E0} increases with increasing deposition temperature. In addition, face-on samples exhibit higher room temperature σ_{E0} than the edge-on samples deposited at the same temperature. This phenomenon indicates higher carrier mobility in the face-on samples than in their edge-on counterparts. In addition, the highest room temperature σ_{E0} , achieved in the face-on samples deposited at 300°C, is much higher than the reported σ_{E0} for PEDOT (~20 S/cm) (9), indicating a much improved carrier mobility in this work compared to the conventional PEDOT thin films. Here, we note that the room temperature σ_{E0} for edge-on samples deposited from 150° to 250°C lies in the range of 16 to 40 S/cm, which is in agreement with the literature value for PEDOT (9). This consistency also validates the reliability of our analysis method.

To compare with experimental results and literature values, carrier mobility is calculated (9) using eq. S1. The calculated room temperature carrier mobility of the face-on films is shown in Fig. 3C. With the deposition temperature varying from 190° to 300°C, the mobility increases from 2.81 to 18.45 cm² V^{-1} s⁻¹. Hall effect measurement validates the calculated carrier mobility for the sample deposited at 300°C (details can be found in section S1). As plotted in Fig. 3C, the measured mobility is $26.6 \pm 9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, whose error range includes the theoretical analysis result. This carrier mobility is among the highest values for conjugated polymers (5, 8). With $\mu = 18.45$ cm² V⁻¹ s⁻¹, the charge carrier density can be calculated as 2.12×10^{21} cm⁻³ using the Drude model. This result is confirmed by the Hall effect measurement [2.73 (± 0.9) × 10^{21} cm⁻³]. The carrier density is in the range of metallic polymers (2 × 10^{21} to 5×10^{21} cm⁻³) (18). The room temperature electrical properties of the oCVD PEDOT thin films are summarized in table S3 in section S6.

Using the temperature-dependent electrical conductivity (Eq. 2 and eq. S1), we also extract the temperature-dependent $\sigma_{E0}(T)$ (fig. S16A) and carrier mobility (Fig. 3D) for face-on samples deposited at both 190° and 300°C, as well as for edge-on samples deposited at 190°C (a detailed discussion can be found in section S12). The key difference of face-on and edge-on films deposited at 190°C is that the carrier mobility of the face-on film markedly increases from 0.7 to 3.2 cm² V⁻¹ s⁻¹ over the experimental temperature range, while the mobility of the edge-on film starts at ~0.77 and increases slowly to 1.1 cm² V⁻¹ s⁻¹. Although the mobility of both edge-on and face-on films deposited at 190°C is almost identical in the low-temperature region, the face-on film shows a much higher increasing rate compared to the edge-on film.

We can now examine the effect of deposition temperature and crystallization-orientation transition on charge carrier transport in PEDOT thin films. With the physical picture of inhomogeneous disorder model (21, 28), $\sigma_{E0}(T)$ is positively correlated to $\exp\left[-\left(\frac{W_{\gamma}}{k_B T}\right)^{1/2}\right]$, where

 W_{γ} is the energy barrier for the intercrystallite carrier transport (9, 25). With an improved morphology and charge transport path, the barrier W_{γ} should decrease (9, 25). We extract the energy barrier W_{γ} (details can be found in section S12) and find that $W_{\gamma} = 175.4$ meV for the 190°C edge-on sample, 0.6 meV for the 190°C face-on sample, and 0.2 meV for the 300°C face-on sample. Here, the W_{γ} of the 190°C edge-on sample is in agreement with the literature report of edge-on dominated regioregular poly(3-hexylthiophene) (~100 meV) (10). Compared to the edge-on films, the energy barrier of the intercrystallite carrier transport is much lower in the face-on films, indicating an intrinsically different physical picture of intercrystallite connection. In addition, higher deposition temperature decreases the energy barrier W_{γ} in the face-on regime, potentially because of improved crystallinity. The much reduced energy barrier W_{γ} in the face-on samples grown at high temperature is the key to the much enhanced carrier mobility.

The low energy barrier of face-on samples may originate from the improved interdomain connection between face-on crystallites. As depicted in Fig. 1A, the connection between crystallites in the face-on samples is largely confined in a thin layer. The connecting polymer chains between two face-on crystallites through a confined space (about three times of the stacking length) are much likely to be more straight [or "rod-like" (28)] and ordered, because the out-of-plane dimension of the thin films may be smaller than the dimension of the random coil. In contrast, in the thick edge-on films (248 nm grown at 190°C; schematic shown in Fig. 1A), the possibility of the formation of the "coil-like" (28), highly disordered intercrystallite polymer chains, or even disconnected chains, is much higher because of the larger film thickness that allows random coil formation. This will result in a much higher intercrystallite energy barrier. Further discussions can be found in section S12.

Previous discussions are all based on the in-plane electrical conductivity of the PEDOT thin films. To further understand the relationship between crystallization orientations and the electrical conductivity, we measured the out-of-plane electrical conductivity (σ_{\perp}). The experimental methods can be found in section S1. The results are summarized in Fig. 4 and Table 1.

As shown in Fig. 4, if we compare the edge-on 190°C-grown PEDOT thin films with the face-on 190°C-grown PEDOT thin films, σ_{\perp} decreases as the crystallization orientation transits from edge-on to face-on. Here, σ_{\perp} values of the edge-on 190°C-grown samples are in agreement with the reported values for PEDOT:PSS (polystyrene sulfonate) measured with relatively large electrodes (*30*, *31*), which validates our results.

In addition, by comparing the σ_{\perp} values of 300°C-grown face-on samples with those of 190°C-grown face-on samples, we observe that σ_{\perp} increases with the increasing deposition temperature in the face-on regime, probably because of increased crystallinity induced by the increasing deposition temperature.

We further calculated anisotropy $(\sigma_{//}/\sigma_{\perp})$ in Table 1. The drop in σ_{\perp} and the increase in anisotropy in the face-on samples compared to the edge-on samples can be explained as follows. As shown in Fig. 1A, in the face-on samples, the interconnecting chains may have a more regular structure extending in the in-plane direction. While this regular interconnecting chain structure enhances the in-plane conductivity $\sigma_{//}$ significantly as we analyzed before, it hinders the delocalization of charge carriers in the out-of-plane direction. At the same time, the more randomized structure of the



Fig. 4. Out-of-plane electrical conductivity of a series of oCVD-grown PEDOT samples. The conductivity in the out-of-plane direction decreases with the crystallizationorientation transition from edge-on to face-on but increases as deposition temperature increases in the face-on regime. The error bar is the SD based on three samples deposited in different batches. The average thickness of the edge-on and face-on samples can be found in Table 1. interconnecting chains in the edge-on samples may provide pathways for charge carrier delocalization in the out-of-plane direction. Therefore, σ_{\perp} in the face-on samples is much lower than in the edge-on samples deposited at the same temperature. In addition, although the π - π stacking of the face-on crystallites in the out-of-plane direction helps delocalize the charge carriers in this direction in the top few nanometers, any shift, tilt, or rotation of the crystallite through the overall thickness will hinder the π - π overlap between two adjacent crystallites, therefore decreasing the overall σ_{\perp} through the whole thickness (32).

In the 300°C-grown face-on samples, the crystallinity of face-on domains is higher than that in the 190°C-grown face-on samples (Fig. 1E). Therefore, the benefit of π - π stacking in the out-of-plane direction of face-on crystallization orientation might begin overcoming the drawbacks of shift, tilt, or rotation, resulting in an enhanced σ_{\perp} in the 300°Cgrown face-on samples compared to the 190°C-grown face-on samples.

The highly conductive oCVD PEDOT film is very attractive for the application of high-frequency (HF) rectifiers because of the reduced resistor-capacitor time constant by its high electrical conductivity. We demonstrate for the first time a Schottky-type radio frequency (RF)

Table 1. Summary of the σ_{\perp} measurement.						
Deposition temperature (°C)	Average thickness (nm)	Crystallization orientation	Average σ_{\perp} (S/cm)	SD of $\sigma_{\scriptscriptstyle \perp}$ (S/cm)	Relative vertical resistance through same area*	Anisotropy (σ _{//} /σ⊥)
190	387.4	Edge-on	0.00645	0.00304	1	7.33×10^4
190	25.7	Face-on	0.000372	0.000131	1.15	2.88 × 10 ⁶
300	28.3	Face-on	0.00135	0.000688	0.350	2.05 × 10 ⁶

 R_{\perp}/R_{\perp} (190°C-grown edge-on PEDOT) given the same contact area S.



Fig. 5. The device performance of RF rectifiers fabricated using PEDOT-Si Schottky diode. (**A**) HF Schottky diode structure composed of high work function metallic oCVD PEDOT thin film and n-type Si. The PEDOT-Si Schottky diode converts the input HF AC signals to DC bias to power a load at its output. (**B**) Optical image of one representative PEDOT-Si RF diode. The zoom-in figure shows the details. The left terminal is the Schottky junction formed between the PEDOT thin film and Si (Au/Ti/PEDOT/Si); the right terminal is the ohmic electrode on top of Si (Au/Ti/Si). The dashed line indicates the mesa isolation region, where the PEDOT thin film is etched away to isolate each electrode. Scale bar, 10 µm. (**C**) Equivalent circuit of PEDOT-Si rectifying diode for measurement at 13.56 MHz. The capacitance in the circuit is 0.02 µF. Inductance is 8 mH. The load resistance is adjusted for impedance matching. (**D**) DC *I-V* characteristics of the PEDOT-Si diode in the log scale. (**E**) Rectifying performance of the rectifier. The red line denotes the input AC voltage at the frequency of 13.56 MHz, while the blue line is the output DC voltage rectified by the PEDOT-Si diode. The load resistance used here is 55 kilohms.

rectifier array working at 13.56 MHz using PEDOT as a high work function metal (33). As a wafer-scale demonstration, we directly synthesize the oCVD PEDOT film on a 10.16-cm Si wafer and pattern it into PEDOT-Si Schottky diode arrays. Figure 5A shows the structure of the Schottky diode formed between the high work function PEDOT and n-type Si. The optical image of a representative PEDOT-Si rectifier is shown in Fig. 5B (see section S1 for the fabrication process). The equivalent circuit of the rectifier is shown in Fig. 5C. The DC I-V characteristics of the PEDOT-Si diode show clear rectification behavior (Fig. 5D). This rectification behavior allows its application in converting incoming AC signal into DC voltage, which is the key in many applications such as RF energy harvesting (that is, rectenna) and RF identification (RFID). Our PEDOT-Si diodes can successfully operate at 13.56 MHz, which is one of the most widely used operation frequencies of RFID. As shown in Fig. 5E, an RF signal at 13.56 MHz ($V_{pp} = 2.5$ V) was generated through a function generator and fed into the PEDOT-Si diode. The PEDOT-Si diode is connected with a load resistance in a series configuration (Fig. 5C). As shown in Fig. 5E, the PEDOT-Si diode can successfully rectify the input RF signals and obtain the DC voltage at the output, which is measured to be ~0.75 V using an oscilloscope. The performance of this rectifier satisfies the standard frequency of 13.56 MHz for the HF system (33). It is also among the best-performing organic rectifiers (33, 34) in terms of working frequency and outperforms many other organic rectifiers with similar structures (33).

In summary, this study demonstrates record-high electrical conductivity of PEDOT with engineered crystallization and morphology. The high in-plane conductivity is a result of enhanced carrier mobility at high carrier density. XRD shows the crystallization-orientation transition induced by increasing the deposition temperature and decreasing the film thickness, which enhances the carrier mobility. Hall effect measurements validate the high carrier mobility and high carrier density calculated from theoretical modeling. Our results suggest that the high mobility could be due to a decrease of the energy barrier of the intercrystallite carrier transport. To fully understand the relationship between crystallization orientation and electrical properties, out-of-plane conductivity is also studied. Finally, the wafer-scale fabrication of a 13.56-MHz rectifier is demonstrated with PEDOT as the high work function metal to validate the metallic nature of the PEDOT thin films. This is also the first RF rectifier using PEDOT as the high work function metal in a Schottky diode.

MATERIALS AND METHODS

oCVD synthesis: The oCVD process introduced the monomer and the oxidant simultaneously. The detailed description and the reactor configuration of the oCVD process can be found in previous literature (20, 35). Figure S1 shows the oCVD process: The monomer EDOT (purchased from Sigma-Aldrich) and the oxidant iron (III) chloride (anhydrous FeCl₃, purchased from Sigma-Aldrich) were introduced in a vacuum chamber in the vapor phase simultaneously, and the deposition took place on the substrate mounted on a temperature-controlled heating stage. The PEDOT films were deposited on (100) Si wafers, Si wafers with 1-µm SiO₂ layer, and glass slides. The samples were prepared with oCVD using a custom-built reactor. With a newly installed heating stage, the substrate temperature can be heated up to 400°C, which is significantly higher than the previous temperature limit (200°C) achieved by other oCVD reactors. The monomer, EDOT, was heated to 140°C in a monomer jar outside of the reactor and was introduced into the vacuum reactor in the vapor phase. The flow rate of EDOT was ~5 standard cubic centimeters per minute (sccm). The oxidant, FeCl₃, was heated to ~200°C

inside the reactor and was also introduced into vacuum in the vapor phase. The pressure of the reactor is maintained at ~1 mtorr. The deposition temperature was controlled at 150° to 300°C, as stated in the main text. The deposition time varied from 20 min to 2 hours to modulate the resulting film thickness. After cooling down to room temperature under vacuum, the samples were taken out and rinsed with methanol to remove the excess oxidant. During the postdeposition HBr treatment, the samples were immersed in 8 M HBr water solution for 5 min and then rinsed with pure methanol to remove residual acid. The samples were stored in airtight desiccators at room temperature. The following measurements were done within 2 weeks of fabrication. More detailed methods can be found in the Supplementary Materials.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at http://advances.sciencemag.org/cgi/ content/full/4/9/eaat5780/DC1

Section S1. Methods

Section S2. Additional information about the XRD results and the surface morphology change reflecting the transition of crystallization orientation and crystallinity

Section S3. Thermal stability of oCVD-grown PEDOT thin films

Section S4. Raman/FTIR/XPS of oCVD PEDOT thin films

Section S5. The influence of film thickness on electrical conductivity and batch reproducibility Section S6. Summarizing the room temperature electrical properties of the oCVD PEDOT samples

Section S7. The effect of HBr rinsing on work function and optical properties

Section S8. The effect of HBr rinsing on crystallization and surface morphology

Section S9. The mechanism of crystallization-orientation transition

Section S10. The discussion about Seebeck coefficient measurement

Section S11. Sensitivity analysis of the Seebeck coefficient measurement

Section S12. The energy barrier W_{γ}

Section S13. The wafer-scale fabrication of RF rectifier arrays and their performance at other frequencies

Table S1. The XRD peak intensity for oCVD PEDOT samples in Fig. 1E.

Table S2. Crystalline domain size estimated from Scherrer equation.

Table S3. Summary of the growth conditions and the resulting PEDOT thin-film properties for the HBr-rinsed thin films.

Table S4. The fitting results for the parameters in $\sigma_{E0}(T)$.

Fig. S1. The schematic of the oCVD process.

- Fig. S2. The thermoelectric and electrical measurements.
- Fig. S3. Schematic representation of out-of-plane conductivity measurement.
- Fig. S4. The work function of PEDOT samples is determined using XPS.
- Fig. S5. The room temperature XRD patterns of oCVD PEDOT thin films rinsed with HBr.
 - Fig. S6. The surface morphology of PEDOT thin films deposited at different temperatures.
 - Fig. S7. The thermogravimetric analysis result.
 - Fig. S8. Room temperature Raman spectra of oCVD PEDOT samples.
 - Fig. S9. Room temperature ATR-FTIR results.

Fig. S10. XPS for oCVD PEDOT.

- Fig. S11. Supplementary data of the electrical conductivity (o) measured at room temperature.
- Fig. S12. The effect of HBr rinsing on work function and optical properties.
- Fig. S13. The effect of HBr rinsing on crystallization.
- Fig. S14. The effect of HBr rinsing on surface morphology of PEDOT thin films.

Fig. S15. Calculated $E_{\rm F} - E_{\rm t}$ and the sensitivity analysis of the Seebeck coefficient measurement error on the calculated carrier mobility.

Fig. S16. Extracting the energy barrier of intercrystallite charge carrier transport.

Fig. S17. Wafer-scale fabrication of the RF rectifier arrays.

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