HHS Public Access

Author manuscript

IEEE Biomed Circuits Syst Conf. Author manuscript; available in PMC 2018 September 28.

Published in final edited form as:

IEEE Biomed Circuits Syst Conf. 2017 October ; 2017: .

A CMOS Front-End Interface ASIC for SiPM-based Positron Emission Tomography Imaging Systems

Samrat Dey,
Department of Electrical Engineering University of Washington Seattle, USA

Jacques C. Rudell,
Department of Electrical Engineering University of Washington Seattle, USA

Thomas K. Lewellen, and
Department of Radiology University of Washington Seattle, USA

Robert S. Miyaoka
Department of Radiology University of Washington Seattle, USA

Abstract

A current-mode interface chip for Silicon Photomultiplier (SiPM) array based positron emission tomography (PET) imaging front-ends is described. The circuit uses a high-speed current amplifier with a low input impedance, to minimize signal loss at the SiPM amplifier interface. To reduce the impact of dark noise, a novel high-speed threshold detection/comparator circuit is used to remove unwanted noise events. A prototype chip interfaces an array of SiPMs to the digital backend of a Positron Emission Tomography (PET) system using 64 readout channels, each of which contain a current amplifier and a threshold detection component. To reduce the number of backend channels, a row-column pulse positioning architecture (RCA) has been implemented. The ASIC occupies an area of 14.04 mm^2 in 130nm STMicroelectronics HCMOS9GP process. The measured input impedance of the current amplifier is 20 ohms at 10 MHz, while the threshold detection circuit's propagation delay is 0.3-2ns.

Keywords

Photodetectors; Biomedical Imaging; current-mode circuits; current amplifier; dark current; current comparator; propagation delay; threshold detection

I. Introduction

Several applications in high-energy physics, bio-molecular imaging and medical imaging require high resolution image sensors. This includes fluorescence lifetime imaging microscopy (FLIM), Forster resonance energy transfer (FRET), optical range finding and Positron Emission Tomography (PET) imaging. Traditional image sensors, like photomultiplier tubes (PMTs), are replaced with solid-state detectors, known as Silicon Photomultipliers (SiPM). SiPM devices are silicon diodes biased above the breakdown voltage to create a high electric field, to detect a single photon, by triggering avalanche breakdown. This helps to achieve high quantum efficiency as well as high gain. Also, the ability to operate at low bias voltages, insensitivity to magnetic fields, and smaller form

factor make them favorable as compared to bulky PMTs. Recent research [1] shows that these diodes can be implemented in CMOS, thus enabling efficient CMOS imagers [2]. However, the high electric field makes SiPM diodes susceptible to various sources of noise. Additionally, increasing the array density of the detectors for improved resolution makes the readout channel more susceptible to optical crosstalk and dark current noise. Fig. 1 shows a typical implementation of a digital acquisition system for PET Imaging. The incident SiPM current is converted into a voltage-mode signal across the input impedance (R_{IN}) of a transimpedance amplifier (TIA), and the ADC at the backend digitizes the amplified signal. A SiPM diode has a finite impedance, thus the input impedance of the current mode front end becomes critical to avoid signal loss. Back-end digital signal processing extracts the pulse energy and the timing information from digitized data, to perform image reconstruction; Fig. 1. Thus, the described chip serves as the interface between the SiPM array and the digital processing. For a PET Imaging modality, the number of channels required varies depending on the application. For example, 400-600 channels are present for small animal PET, while that for a brain PET scanner is ~4500. In an effort to reduce the number of channels, multiplexing and channel combining techniques have been applied – both in the electrical and optical domain [3] [4]. However, these techniques can lead to SNR degradation due to optical crosstalk and dark noise. Dark noise is caused by the random generation of electrons and holes within the depletion region of the SiPM diode because of the high electric field, even in the absence of an incident photon. If the dark noise is strong enough, these noise events can trigger a false positive detection, thus the need to mitigate the impact of this noise source.

This paper presents a PET Imaging readout system with a low input impedance front-end interface current amplifier and a threshold detection circuit based on a high-speed current comparator architecture. The described approach helps reduce the contribution of dark noise produced by silicon photodiodes. This circuit is a component in Row-Column Architecture (RCA) chip [5]- details of this architecture go beyond the scope of this paper and are given in [5]. This paper begins in Section II with a description of the current amplifier architecture used to realize the front end interface with the SiPM diode. Next, Section III provides a discussion about dark noise and describes a current mode threshold detection circuit for dark noise mitigation. Section IV provides measurement results, followed by some concluding comments in Section V.

II. Front End Interface Electronics

The electric field developed in the depletion region of a SiPM device is higher than 3×10^5 V/cm, due to the bias voltage being higher than the breakdown voltage. This region of operation is known as Geiger-mode Avalanche (GM), differentiating it from normal avalanche mode, where the bias voltage is less than the breakdown voltage. In PET detection systems, the incident photon initiates the avalanche breakdown. A SiPM diode is segmented into thousands of tiny micro-cells (each working in GM) connected in parallel to a single output. When activated by an incident photon, the current response is similar for all the microcells, making the output signal proportional to the number of cells hit by a photon. The large number of microcells in parallel effectively reduces the complex impedance seen at the input of the front end interface, making it absolutely essential to have a low input impedance

front end. This prevents current sharing and extends the bandwidth at the SiPM-amplifier interface. Current-mode circuits have predominantly low impedance nodes, making them more favorable than their voltage-mode counterparts. Many of the existing current amplifier topologies have a direct tradeoff between the input impedance and bandwidth. A common-gate (CG) transistor with a large transconductance g_m can be used at the expense of either a large device or a large amount of current. Shunt feedback can be used to increase the effective g_m, as is done in regulated cascode buffers (RGC) [6]. The limited voltage gain from a common source (CS) stage implies lower loop-gain, and thus, a limited Z_{in} reduction.

This design includes an extra common gate stage in the feedback loop of the RGC buffer [7], Fig. 2. In addition to increasing the loop gain, the CG stage decreases capacitive loading at the input and increases the available DC headroom as compared to a CS stage. However, the presence of two poles within the feedback loop requires attention. R1 and C1 compensate the frequency response of the loop with a zero, maintaining loop stability. The CG stage introduces noise at higher frequencies, but a signal-to-noise ratio of 5 dB at the output of the interface electronics is enough to maintain the full width at half maximum (FWHM) energy resolution of the SiPM pulses [8]. As a result, relatively modest noise performance is required of the front-end interface electronics in a SiPM based PET Imaging System.

III. Dark Current Mitigation

The high electric field used to bias a SiPM device can lead to avalanche breakdown due to non-photo generated carriers. Known as dark noise, this results from carriers, trapped during the discharge and released after a pulse event, or carriers generated by photons emitted during the discharge of neighboring photodiodes (optical cross-talk). As more channels are multiplexed or combined, as with the RCA architecture, dark noise becomes a major design front-end challenge. In short, combining front-end channels will lead to the accumulation of dark noise generated by multiple SiPM devices throughout the array. This increases the possibility of producing a false triggering event as compared to a single-channel readout of individual SiPMs. This current-mode interface utilizes a threshold detection circuit embedded with the front-end current amplifier to reduce dark noise events. The input SiPM pulse is compared with a programmable threshold, Fig. 3. In its default state, the switch is open and the output of the amplifier is disconnected from either a row, or column output. If the input signal is more than the threshold, the switch is closed to connect the front-end amplifier with the output stage.

This considerably reduces the overall noise at the output, thus enhancing the SNR for backend processing. There are several design aspects of this particular threshold detection circuit. First, different SiPM operating conditions require an adjustment of the threshold level, thus the circuit must be made tunable. Second, it is critical that the threshold detection circuit is fast enough to capture as much energy as possible associated with a real photon detection event. As the threshold detection circuitry takes longer to enable the readout signal path, more energy is lost from a single SiPM pulse, as is evident in Fig. 3. In short, any mismatch between the delays T_{D1} and T_{D2} will clip the rising edge of the SiPM pulse, at the amplifier output. The SiPM pulses have a considerably shorter rise time as compared to the

fall time, and preserving the rising edge is critical to retain timing resolution in the overall PET system.

A current comparator is utilized to realize the threshold detection circuitry, shown in Fig. 4. Traditional high speed current comparators, [9] are composed of three parts- the input stage, the current positive feedback circuit and slew rate enhancement circuits. Shown in Fig. 4, the input stage is realized with current mirrors (M1-M2 and M3-M4), where the SiPM current is compared with a reference threshold current. The current fed to the second stage, I_{IN} is simply the difference between I_{SiPM} and I_{REF} ($I_{IN} = I_{SiPM} - I_{REF}$), see Fig. 4. The reference current is tunable from 100μA to 1.5mA, allowing for a variable threshold, tunable for various SiPM devices. The second stage is a current comparator used to amplify the current difference from the first stage. Normally this is done using a source follower stage [9] where a low input impedance allows detection and amplification of the current difference. In this work, a regulated cascode stage is used (M5-M9). The shunt feedback reduces the input impedance by a factor equal to the loop gain, resulting in a lower impedance than a source follower stage, making it more sensitive to changes in I_{IN} . In the third stage, an inverter chain is used which amplifies the threshold detection signal forcing it to run rail-to-rail. A replica bias circuit (RB in Fig. 4) is used to force the DC bias voltage at node Y to VDD/2. When there is no SiPM current, the threshold current mirrored by the transistors M3-M4 flows into the regulated cascode stage, thus bringing down the voltage of node Y from $V_{DD}/2$. This drives the output of the comparator low, which turns off the transistor switch (Fig.4). When there is a photon event, transistors M3-M4 mirror the SiPM current to node X, Fig. 4. If the SiPM current is lower than the threshold current, the comparator output retains the default operating condition as before, thus no signal pass through the current amplifier. However, when the SiPM delivers a current more than the threshold current, the voltage at node Y becomes higher than $V_{DD}/2$. As a result the output of the comparator is high, enabling the transistor switch (Fig. 3). The inverter with resistive feedback (M10-M11) allows the transistors to operate in the saturation region, thus having a very high voltage gain and less propagation delay. Also, biasing node Y at mid-rail reduces the propagation delay by holding the inverter input bias voltage near the comparator tripping point. The low input impedance of the regulated cascode, followed by the high gain of the inverter, ensures that any change in I_{IN} is propagated without delay to the output of the comparator, even at high frequencies.

IV. Measurement Results

The readout chip was fabricated in a 130nm 6-layer metal stack STMicroelectronics HCMOS9GP process, see Fig. 5. The chip dimensions are 3.9mm × 3.6mm. It has 64 channels in an 8×8 array. The RCA architecture is used to reduce the number of output channels to 16 (8 rows and 8 columns) and one timing channel. The board was mounted on a detector test bench with a SiPM array as well as with a BNC (Berkeley Nucleonics Corporation) Fast Tail Pulse Generator, Fig. 6. The inset shows the system response to both the pulse generator and the SiPM array. The data from the detector appears to be noisy, due to cross talk from neighboring detector elements.

Fig. 7 shows an S_{11} measurement using a N5247APNA-X Network Analyzer which obtained the front-end amplifier input impedance. The real part resistance is 20Ω at 10 MHz and increases to 50Ω at 500 MHz, as the loop-gain in the feedback loop decreases. Although the data below 10 MHz is not available, but higher loop gain at low frequencies will reduce the input impedance further.

Measurement data was acquired using the pulse generator to verify the threshold detection circuitry performance, shown in Fig. 8. When the threshold current is zero, the output of the channel maintains the energy as well as the timing information of the input pulse. However, as the threshold current level is increased to 1.2 mA and 1.5mA, the channel output becomes disabled, thus validating the functionality of the current comparator circuit. The negative spike for the 1.2 mA current threshold is due to the switching transients generated by the current comparator. The switching transients coupled with the propagation delay across the current comparator can lead to clipping on the rising edge of the pulse.

To investigate this, the clipping was noted at different threshold current levels, Fig. 9. The offset at a zero threshold level, 0.4ns is the propagation delay through the channel alone. The minimum propagation delay measured across the current comparator is (0.7 −0.4 =) 0.3ns for a threshold current of 100 μA. The lowest propagation delay for traditional current comparators known to the authors is reported to be 0.6 ns [10].

V. Conclusions And Future Work

This work describes an ASIC acting as the front-end readout electronics in SiPM-based PET Imaging systems. A low input impedance, high-bandwidth current amplifier interfaces the SiPM diode, followed by a threshold detection circuit to reduce dark noise at the output. At present, the described chip is being interfaced to data acquisition boards with ADCs and FPGAs which emulates the digital backend [11].

References

[1]. Rochas A, Gani M, Furrer B, Besse PA and Popovic RS., “Single photon detector fabricated in a complementary metal-oxide-semiconductor high-voltage technology,” Review of Scientific Instruments, vol. 74, no. 7, pp. 3263–3270, 7 2003.

[2]. Gersbach Marek and Charbon E , “ A Time-Resolved Low Noise Single-Photon Image Sensor Fabricated in Deep-Submicron CMOS Technology,” IEEE Journal of Solid State Circuits, Vol. 47, No. 6, 6 2012, pp. –1394–1407.

[3]. Miyaoka RS, Kohlmyer SG, and Lewellen TK, "Performance characteristics of micro crystal element (MiCE) detectors," Nuclear Science, IEEE Transactions on, vol. 48, pp. 1403–1407, 2001.

[4]. Olcott PD, Chinn G, and Levin CS, "Compressed Sensing for the multiplexing of PET detectors," 2011 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), pp. 3224–3226, 2011.

[5]. Dey S, Lewellen TK, Miyaoka RS, Rudell JC, “Highly-Integrated CMOS Interface Circuits for SiPM-based PET Imaging systems” IEEE Nuclear Science Symposium and Medical Imaging Conference(NSS/MIC), pp.- 3556–3559. 2012.

[6]. Rodriguez BA, Temes GC, Martin KW, Law SML, Handy R and Kadekodi N. “ An NMOS buffer amplifier,” IEEE Journal of Solid State Circuits, vol. SC-19, no.1, pp.69–71. 2 1984.

[7]. Kromer C, Sialm G, Morf T, Schmatz ML, Ellinger F, Erni D and Jackel H, " A Low-Pwer 20-GHz 52-dBΩ Transimpedance Amplifier in 80nm CMOS", IEEE Journal of Solid State Circuits,vol.39, no.6, pp.885–894, 6 2004.

[8]. Dey S, Lewellen TK, Miyaoka RS, Rudell JC, "Impact of Analog IC Impairments in SiPM Interface Electronics" IEEE Nuclear Science Symposium and Medical Imaging Conference(NSS/MIC), pp.-3572–3574., 2012

[9]. Traff H, "Novel approach to high speed CMOS current comparators," Electronic Letters, vol. 28,no.3,1 1992.

[10]. Tang X, Pun KP, " High-performance CMOS current comparator.", Electronic Letters vol.45, no. 20, pp.1007–1009, 2009.

[11]. Lewellen TK, Miyaoka RS, Macdonald LR, DeWitt D, Hauck S, "Evolution of the Design of a Second Generation Fire Wire Based Data Acquisition System", IEEE Nuclear Science Symposium and Medical Imaging Conference(NSS/MIC), pp. 2510–2514, 2010.

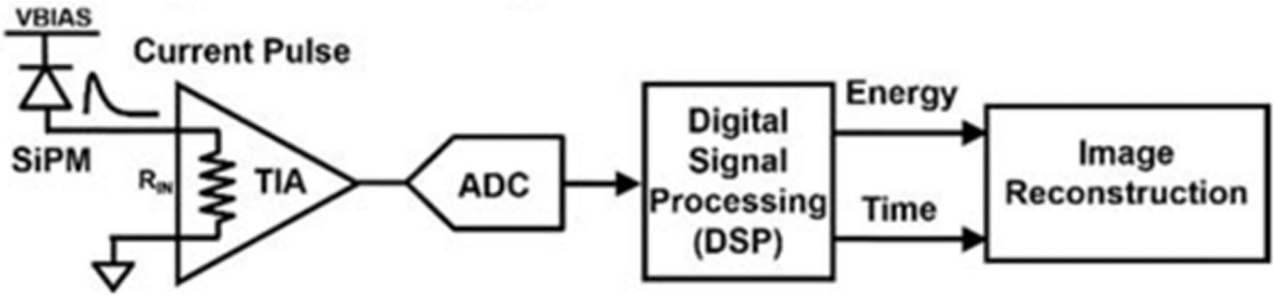

Fig. 1:
Generic PET imaging channel electronics

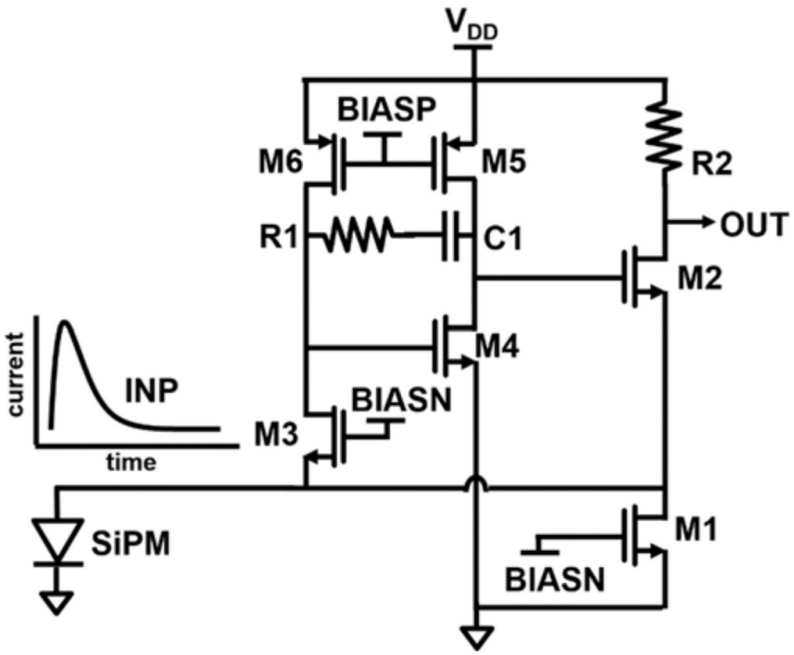

Fig. 2:
Proposed Front End Current Amplifier

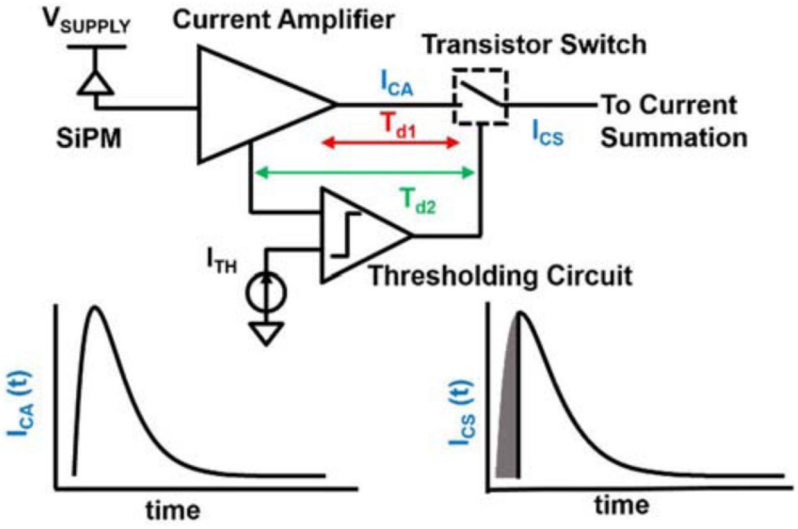

Fig. 3:
Illustration of clipping on a SiPM pulse rising edge.

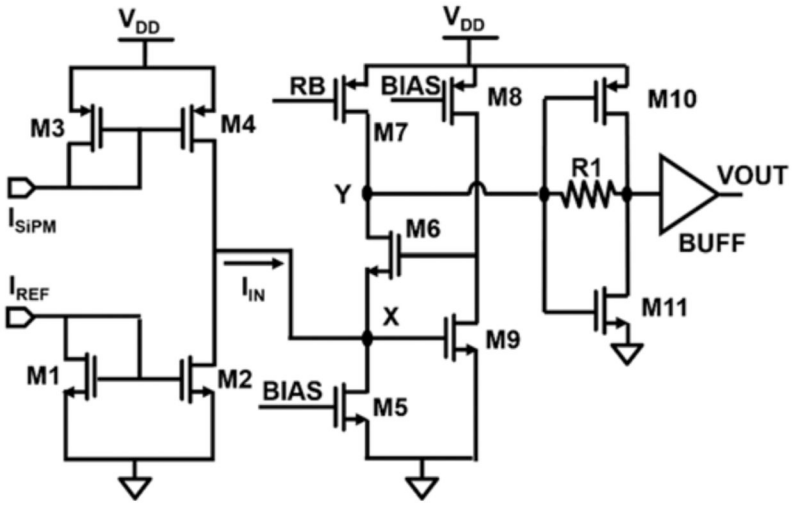

Fig. 4:
Current Comparator

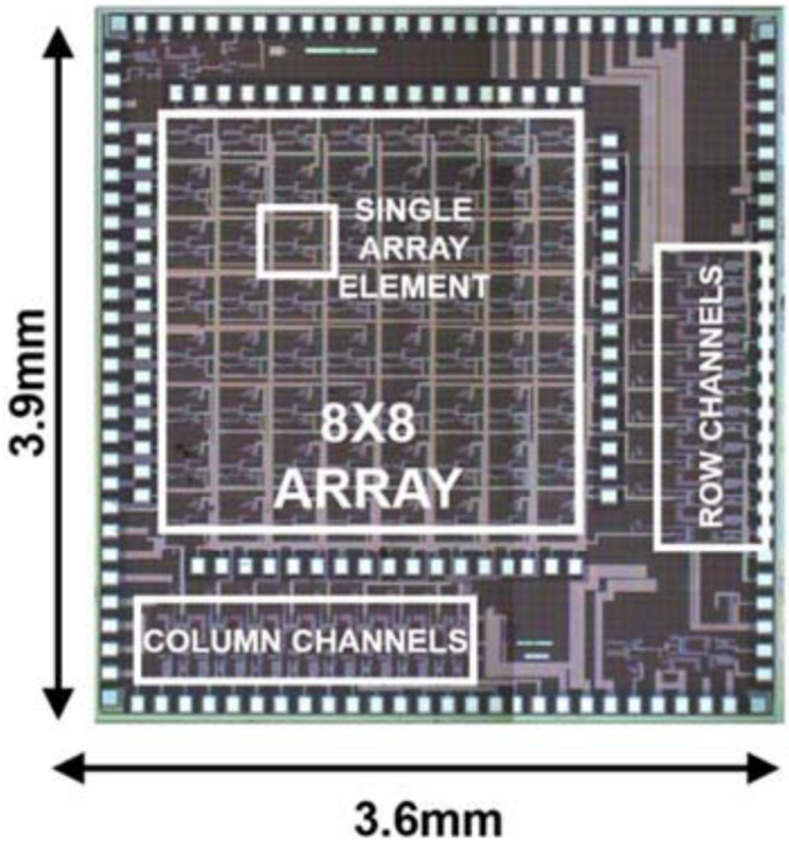

Fig. 5:
Die Photo

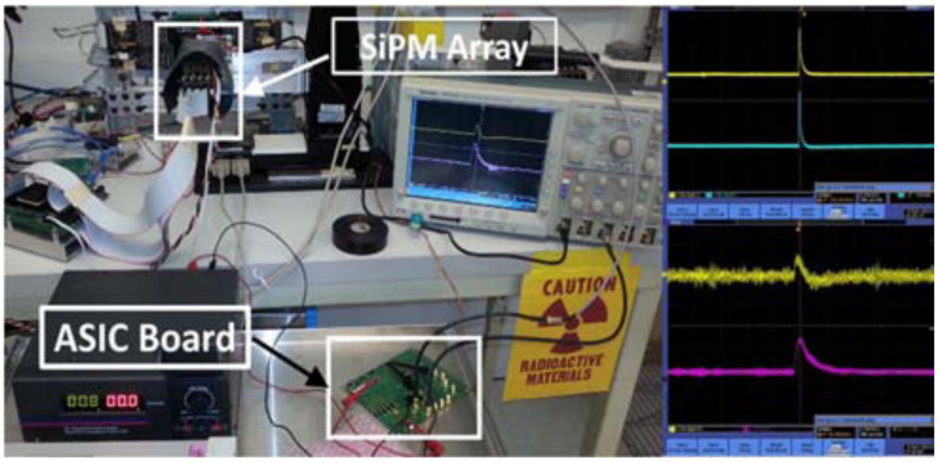

Fig. 6:

Left - Test board mounted on a detector test bench, Right - (top) Data from pulse generator, Right - (bottom) data from the detector test bench.

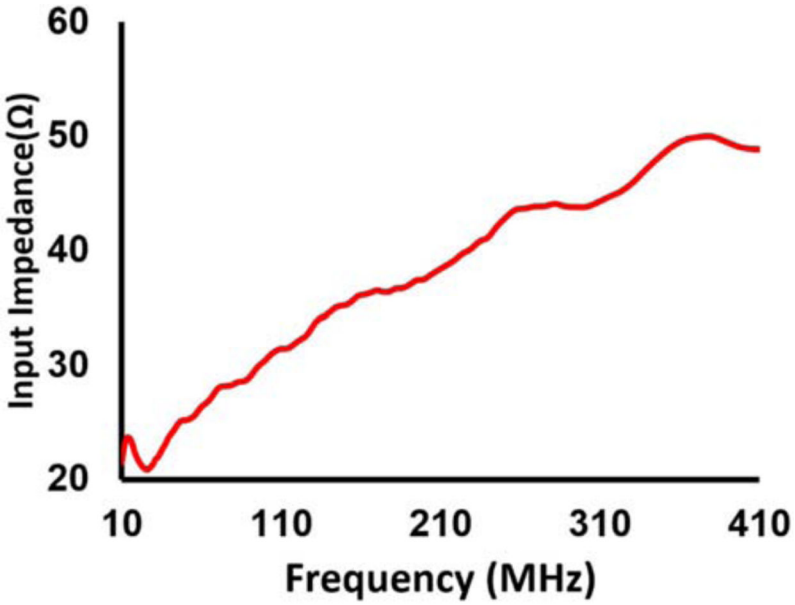

Fig. 7:
Input Impedance of Front End Amplifier

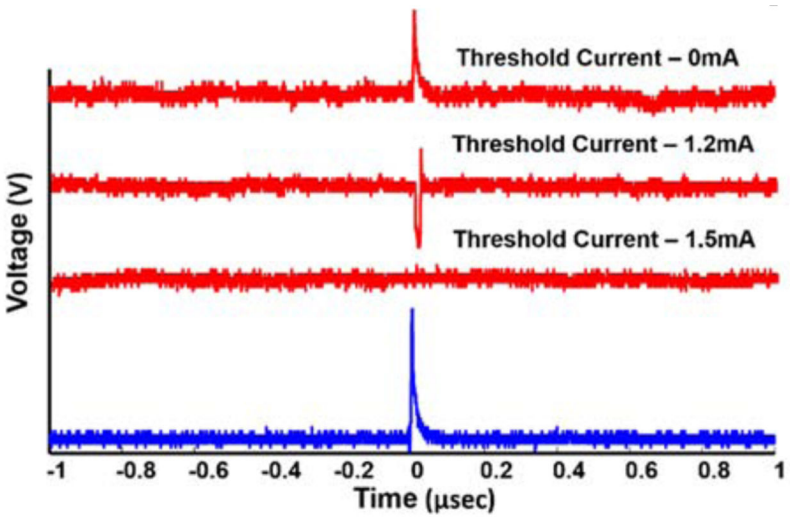

Fig. 8:
Threshold Detection using different reference current levels (Blue-Input, Red - Output).

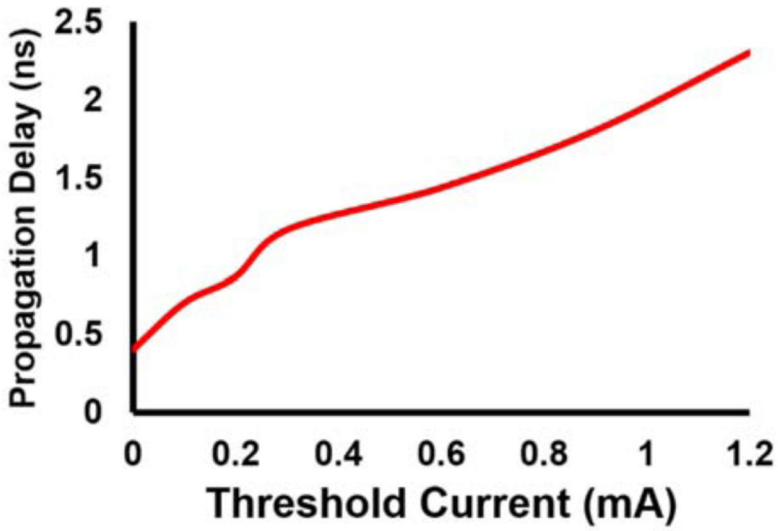

Fig. 9:
Propagation Delay and clipping of rising edge