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Scalable Manufacturing of Single Nanowire Devices Using Crack-Defined Shadow Mask Lithography

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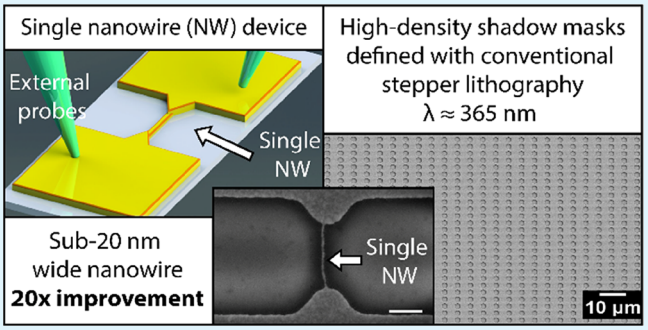
Supporting Information

ABSTRACT: Single nanowires (NWs) have a broad range of applications in nanoelectronics, nanomechanics, and nanophotonics, but, to date, no technique can produce single sub-20 nm wide NWs with electrical connections in a scalable fashion. In this work, we combine conventional optical and crack lithographies to generate single NW devices with controllable and predictable dimensions and placement and with individual electrical contacts to the NWs. We demonstrate NWs made of gold, platinum, palladium, tungsten, tin, and metal oxides. We have used conventional i-line stepper lithography with a nominal resolution of 365 nm to define crack lithography structures in a shadow mask for large-scale manufacturing of sub-20 nm wide NWs, which is a 20-fold improvement over the resolution that is possible with the utilized stepper lithography. Overall, the proposed method represents an effective approach to generate single NW devices with useful applications in electrochemistry, photonics, and gas- and biosensing.



KEYWORDS: *single nanowire devices, gold nanodevices, metal nanowires, self-aligned electrodes, shadow mask evaporation, crack lithography*

INTRODUCTION

Nanowires (NWs) are one-dimensional nanoscale structures, that is, structures featuring a width and depth of a few tens of nanometers or less but with a much longer length. As a result of their high surface-to-volume ratios, NWs have interesting properties such as enhanced gas sensing, controlled catalysis, and surface-enhanced Raman scattering.[1−5] NWs also have a broad range of applications in nanoelectronics, nanomechanics, and nanophotonics.[6−10] The lateral dimension in single-crystalline NWs leads to quantum confinement and ballistic transport effects, which are important for field-effect transistor and single-electron transistor applications.[11−13] In light of these promising features, extensive research has been dedicated in the last two decades to the fabrication of NWs and their integration with electronics in a scalable fashion.

A wide range of techniques exist to produce NWs, such as epitaxial, chemical, and thermal growth with and without template structures,[14−17] direct writing using focused ion beams (FIBs), and electron beam lithography (EBL).[18−20] However, these methods are not compatible with large-scale manufacturing of single NW devices (Figure 1a) because they rely on serial processes, being either the scan-based lithographic step or the pick-and-place strategy for each individual NW. Even when careful schemes are adopted to avoid the handling of the individual NWs, bottom-up grown NWs have a wide distribution of geometries and are possible for a limited set of materials.[21] The lack of large-scale manufacturing for single NW devices has been a major roadblock in developing any application involving NWs outside a research laboratory. A scalable alternative technique is sidewall lithography, which is based on the conformal deposition of a thin film on prepatterned structures and subsequent anisotropic etching.[22,23] However, this method is only suitable for a limited number of NW materials, and all NWs on a substrate necessarily have an identical width (defined by the thickness of the deposited film), which severely limits the flexibility of sidewall lithography.

A promising fabrication alternative potentially providing both material flexibility and scalable manufacturing is shadow mask (or stencil) lithography.[24−26] In this approach, a masking layer featuring nanogaps is interposed between the target substrate and the source of the evaporated material in a highly parallel fashion. Thus, the material is deposited only on the unmasked substrate areas. Physical vapor deposition (PVD) allows a wide selection of materials to be deposited for forming NW structures, and no postprocessing after the deposition of the NW material is needed because no etching or lift-off processes are involved to obtain single NWs. The dimensions of the individual NWs and their positioning on the surface of the substrate are also well controlled. However, if the apertures

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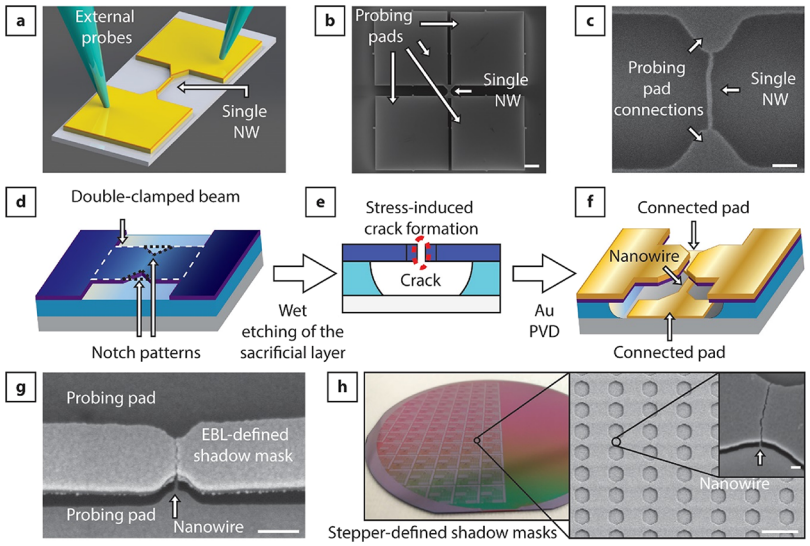

Figure 1. Concept and realization of single NW devices. (a) Conceptual drawing of a single NW device and (b) SEM image of a fabricated device in a four-point configuration. Scale bar, 20 μm. (c) Top-view SEM image of a fabricated single Au NW. Scale bar, 100 nm. (d) Lithographic patterning of a notched double-clamped beam structure in the TiN layer. (e) Isotropic chemical etching of the Al_2O_3 layer and fracturing of the TiN bridge, leading to nanogap formation. (f) Conceptual perspective view of a fabricated crack-defined shadow mask after evaporation of a thin Au film, with the formed single NW device on the SiO_2−Si substrate. (g) SEM image (side-view) of a formed Au NW below the TiN shadow mask. Scale bar, 200 nm. (h) Process scalability. A 100 mm diameter wafer was patterned using i-line stepper lithography (image on the left). The top-view SEM image in the center shows a density of 40 000 shadow masks per square millimeter. The side-view SEM image on the right displays a formed Au NW featuring a width of 15 nm. Scale bars: 5 μm for the top-view SEM image and 100 nm for the side-view SEM image.

in the shadow mask layer are in the sub-nanometer range, the reusability of the stencil is limited, as it would need further processing to clean the stencil after use, and these processes could damage the stencil or modify the geometries of the nanoscale features. A single-use stencil or limited reusability is an important concern if the definition of nanoscale patterns is performed with slow and serial techniques such as EBL, or FIB ablation, making this kind of approach unsuitable for batch fabrication.

To that end, several research groups have investigated wafer-scalable alternatives to produce nanoscale patterns for shadow mask lithography, including nanosphere lithography, interference lithography, and membrane stacking.[27−33] However, these techniques are limited to periodic arrays of identical structures, and achieving a fine dimensional control in the sub-100 nm range with this approach is still an open challenge. Moreover, the use of stencils formed with these techniques would lead to the formation of high-density vertical NWs, which is not ideal for the realization of single NW devices. Moreover, the vertical structures require one or more integration steps, during which the NWs are exposed to chemical or coated with other materials, limiting the range of possible applications. The possibility to produce planar NWs of the arbitrary material is a great advantage for device prototyping.

A scalable approach to produce shadow masks for the realization of planar NWs is based on fracture and delamination (crack lithography) approaches to generate nanoscale features in shadow masks or stencils for NW fabrication, including approaches demonstrated on the wafer scale.[34−40] However, these approaches result in poorly controlled NW networks in which single NWs are not defined in a controllable and repeatable way. The combination between optical lithography and crack formation can generate single NWs with controlled position.[41−43] However, all NWs on the substrate necessarily have the same width defined by the batch thermal or chemical processes which generate the cracks. The scalable fabrication of individual NWs featuring sub-20 nm widths using crack lithography is, to the best of our knowledge, unreported in previous works.[44−46]

Here, we address the limitations in scalability and control of existing fabrication approaches for single NW devices and demonstrate the wafer-scale manufacturing of single NW devices. In this work, we formed sub-20 nm wide nanogaps in a shadow mask layer made of titanium nitride (TiN) by controlled crack formation in notched beam structures.[47,48] The crack-defined nanogap structures were used as shadow mask elements during PVD of the NW material to realize single NW devices consisting of individual NWs that are electrically connected to self-aligned contact pads (Figure 1b,c). In contrast to the alternative direct writing techniques which could achieve the same high-resolution patterning, our approach is suitable for large-scale manufacturing of single NW devices with sub-20 nm widths because the crack-defined nanogaps are obtained in a parallel and fully scalable processing scheme. We fabricated single NWs featuring sub-20 nm widths realized using stepper technology, thereby demonstrating the wafer-scale compatibility of our technique. We also explored the compatibility of our technique with different NW geometries and evaporated materials. In this case, we used EBL-defined shadow masks because EBL is more suitable for rapid and efficient adaptations of the patterns defining our experimental device structures.

RESULTS

Shadow Mask and Single NW Device Manufacturing.

To realize single NW devices, our approach consists of first generating nanogaps in a shadow mask using controlled crack formation. For the shadow mask formation, we used atomic layer deposition (ALD) to deposit a thin film of a brittle

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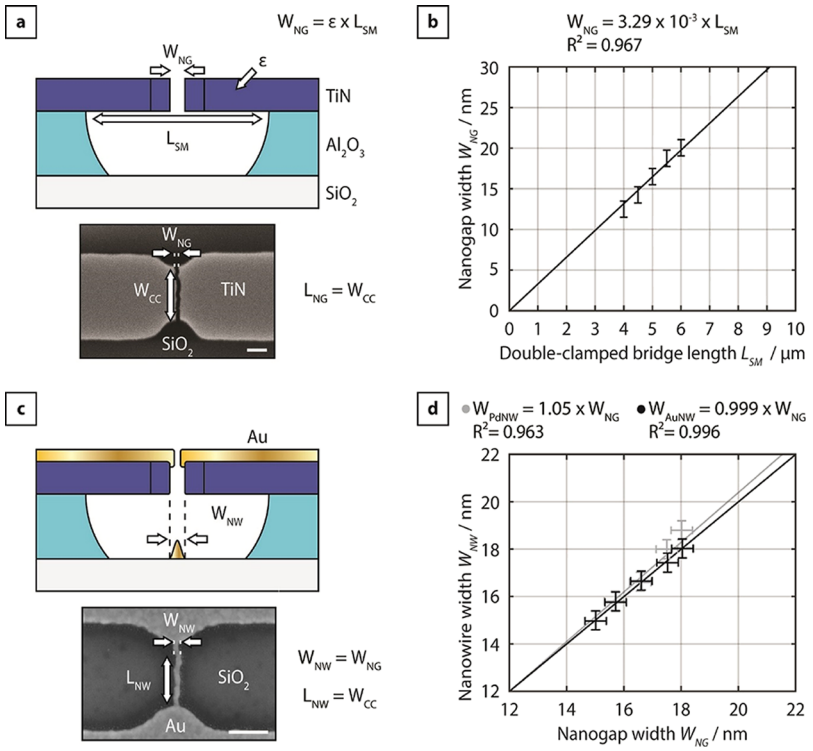

Figure 2. Control of the nanogap and NW dimensions. (a) Schematic illustration and top-view SEM image of a crack-defined nanogap in the TiN layer. The nanogap width W_{NG} is in a first-order approximation equal to the length L_{SM} times the stored elastic strain ε in the TiN layer. The nanogap length L_{NG} is defined by the width of the notched constriction W_{CC}. Scale bar, 200 nm. (b) Graph showing the proportionality between the micrometric length of the suspended shadow mask and the nanometric width of the nanogap. The resulting fit is in agreement with the previous results on crack-defined nanogap generation.[35] (c) Schematic depiction and top-view SEM image of a formed single NW. The NW length L_{NW} and width W_{NW} are defined by W_{CC} and W_{NG}, respectively. Scale bar, 200 nm. (d) Graph comparing the measured W_{NG} and the resulting W_{NW} for Au and Pd NWs.

material (TiN) with residual tensile stress, on top of a sacrificial layer (Al_2O_3), on an oxidized silicon (SiO_2–Si) substrate. The TiN film was subsequently patterned to obtain a doubly clamped beam structure with a notched constriction (Figure 1d). Next, the notched beam structure was release-etched by wet chemical etching of the sacrificial layer underneath. During the release-etching, the notched constriction of the beam structure fractured as a result of built-up stress. Dubois et al. have shown that an optimized geometry of the notched beam can lead to a very high yield of fracture.[47,49] Upon fracture, the initially intact beam structure was split in two separate cantilevers that released their tensile stress by contraction. The contraction of the cantilevers defined a nanogap separating the two cantilevers (Figure 1e), thereby completing fabrication of the shadow mask.

Then, we formed the single NW devices using a single step of PVD of the selected NW material through the shadow mask. In the directional deposition process, the evaporated material is free to pass through the crack-defined nanogap in the shadow mask and lands on the target substrate, thereby forming NWs. The deposition also produced large areas of the same material directly connected to the NW extremities, which served as electrical probing pads on the target substrate (Figure 1f). The NW positioning corresponded to the placement of the crack-defined nanogaps, whose positions were defined lithographically by the placement of notches, allowing for high placement accuracy of the NWs on the surface of the substrate (Figure 1g).

Scalable Manufacturing of Single NW Devices. The shadow masks presented in this paper were produced by either EBL or i-line stepper lithography. We used EBL to pattern the beam structures as a proof of concept and to have flexibility in adjusting designs of the shadow mask for the morphological and electrical characterization of the NWs. On the basis of the optimized design, we then generated a lithographic mask and used i-line stepper lithography (nominal resolution ≈ 400 nm) to demonstrate that the fabrication of the shadow masks can be massively parallelized using optical lithography. In both cases, because the sub-20 nm features of the nanogaps are crack-induced, we avoid the need to pattern them directly, which would require high-resolution serial patterning techniques. We achieved wafer-scale patterning and release-etching of the shadow masks and generated sub-20 nm nanogap features on a 100 mm diameter silicon (Si) wafer in a highly parallel fashion (see Experimental Section for details on the fabrication of stepper-defined shadow masks defined by stepper lithography). The shadow mask geometry has been adjusted to comply with the resolution capability of conventional stepper lithography and to achieve crack formation during the release-etching of the shadow mask.

After evaporation, we used scanning electron microscopy (SEM) to confirm the formation of NWs using a stepper-defined shadow mask with sub-20 nm wide crack-defined nanogaps (Figure 1h). Compared with the nominal resolution of the stepper, this is a 20-fold improvement in lateral resolution of the resulting structures. Considering a density of 40 000 shadow masks per square millimeter, it is possible to

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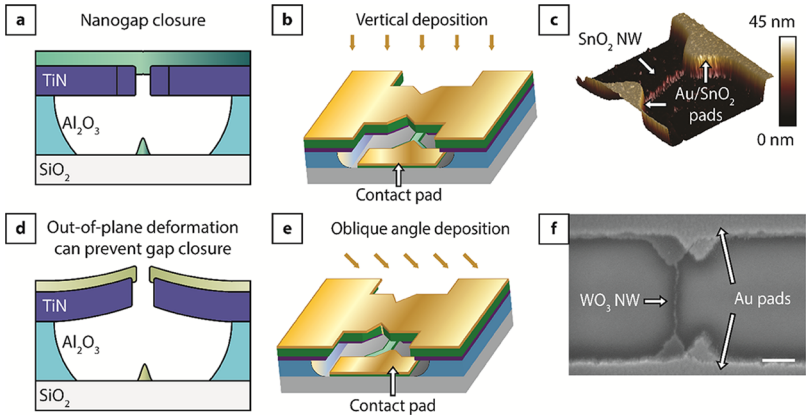

Figure 3. Fabrication schemes for contact metallization of single NWs. (a) Schematic drawing of nanogap closure. (b) Schematics for self-aligned contact metallization for closed nanogaps. (c) AFM image of a single NW with metal contacts, where we first deposited SnO_2 until nanogap closure and then deposited Au to create self-aligned electrical probing pads connecting the NW. Scale bar, 200 nm. The AFM image provides a clearer view of the SnO_2 NW. (d) Schematic drawing of a nonclosed nanogap due to out-of-plane deformation of the shadow mask during deposition. (e) Schematic drawing for self-aligned contact metallization for nonclosed nanogaps. (f) SEM top-view image of a single NW, where WO_3 was deposited without achieving nanogap closure. The subsequent oblique angle evaporation of Au then achieved contact metallization without forming a second NW, which would have otherwise covered the WO_3 NW. Scale bar, 200 nm.

fabricate more than 25 000 single NW devices on a single 100 mm diameter wafer, using the same dimensions as the device shown in Figure 1c. The complete process takes 10−15 h of cleanroom processing, depending on the number of materials and steps of depositions. Moreover, Dubois et al. have shown a 99.7% cracking yield over 1200 devices using stepper lithography, demonstrating the reproducibility of the controlled crack formation in combination with batch lithography.[49]

Dimensional Accuracy of Controlled Crack-Defined Nanogaps. Besides the possibility to produce large numbers of single NW devices in a highly scalable fashion, our methodology allows the control of the width W_{NW} and length L_{NW} of each and every NW with nanoscale accuracy. This is because W_{NW} and L_{NW} are set by the width W_{NG} and length L_{NG} of the crack-defined nanogaps, respectively, both of which are defined by the lithographic pattern of the shadow masking cantilevers. Specifically, W_{NG} is controlled by the length L_{SM} of the suspended part of the cantilevers (Figure 2a).[47] W_{NG} and L_{SM} are in a first-order approximation proportional to each other with the stored elastic strain ε of the TiN layer as proportionality constant with

$$W_{NG} = \varepsilon \times L_{SM} \quad (1)$$

where ε is equal to the internal stress of the electrode layer, s, divided by its Young's modulus: E

$$\varepsilon = s/E \quad (2)$$

Moreover, L_{NG} is defined by the width W_{CC} of the notched constriction of the cantilever where the crack propagates. Because W_{CC} and L_{SM} are independent geometrical variables defined lithographically, so are L_{NG} and W_{NG}. We will later see that this geometrical control of the crack-defined nanogap dimensions is translated into NWs of similarly well-defined dimensions after PVD.

An SEM analysis of a total of 50 devices and 5 devices per design confirms that the widths of the nanogaps obtained from different shadow mask designs are linearly proportional to the total length of the suspended shadow mask, as predicted by eq 1 (Figure 2b). The value of the proportionality constant is comparable to what was previously reported for the same stack of materials but different thicknesses of the sacrificial layer.[47]

Fabrication and Morphological Characterization of Individual NW Devices. To demonstrate the ability to control the geometry of the NWs, we used EBL for prototyping, varying the geometry of the notched beam structures, and then performed a PVD (Figure 2c). We designed NWs with two distinct lengths L_{NW}, which were defined by the widths of the notched constrictions of the suspended beam structures W_{CC}, namely, 400 and 250 nm. For each NW length design, we included a subset of different designs for shadow mask length L_{SM}, ranging from 4 to 6 μm, in steps of 0.5 μm to obtain NWs featuring small but controllable increments in widths. Here, we chose gold (Au) as the evaporated NW material because it allows high-resolution imaging of the resulting nanostructures using SEM. Au further exhibits various interesting electrical, chemical, and plasmonic properties, which makes it a highly relevant material for NWs with a wide range of applications. We repeated the study with palladium. Palladium (Pd) is a noble metal featuring strong electrocatalytic properties, and palladium NWs are utilized for sensing application, in particular as high-performance hydrogen sensors.[50,51] It cannot be easily patterned using lift-off masks made of photoresists because of its high melting point.

The SEM analysis of five Au and five Pd NWs per design confirmed the successful implementation of our method, whereby different shadow mask designs produced different geometries of the resulting NW structures (Figure S1). The NW geometries were further characterized by removing the suspended shadow mask. This was done by applying an adhesive tape to the TiN shadow mask layer and peeling off the tape. SEM analysis confirms that the suspended cantilevers are effectively removed with this simple method, thereby leaving the NWs unmasked and accessible for precise visual characterization. The linear fit of the relation between the width W_{NG} of the crack-defined nanogap in the shadow mask layer and the width W_{NW} of the resulting NW indicates a faithful transfer of the geometry from the shadow mask to the formed NW (Figure 2d). Because W_{NG} is controlled by L_{SM}, we were able to control the geometry of the NW by tuning the micrometric geometry of the shadow mask pattern, which can

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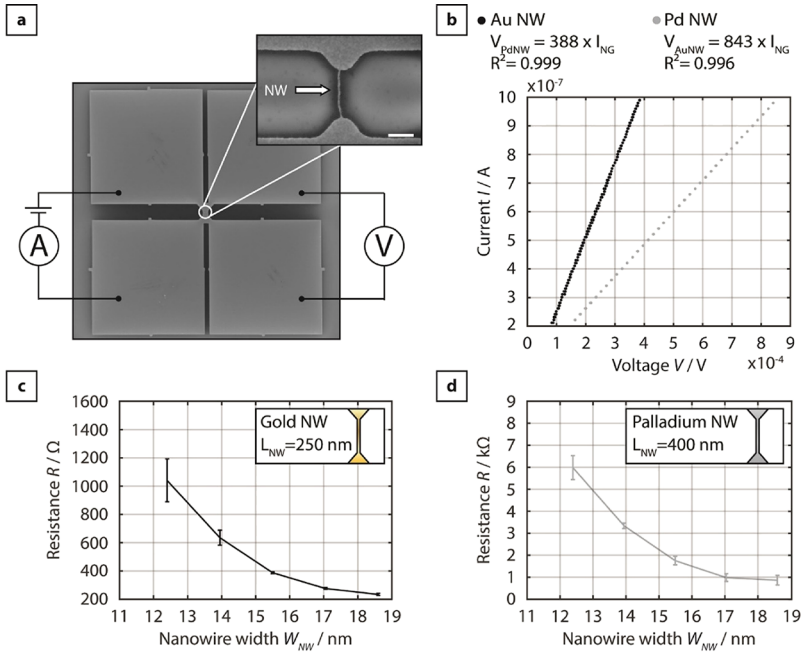

Figure 4. Electrical characterization of single NW devices. (a) Four-point configuration for electrical characterization, with top-view SEM images of a complete device and inset with a single NW. Scale bars: 20 μm for the complete device and 200 nm for the inset. (b) $I-V$ curves of single NW devices made of Au and Pd featuring the same geometry, exhibiting linear $I-V$ relations. The width and length of the NWs were 20 and 400 nm, respectively. The values of resistance of the NWs are approximately 1 order of magnitude higher than the ones calculated using the bulk sheet resistance for Au and Pd, indicating that the electrical conduction is influenced by the surface roughness scattering in the polycrystalline NW structures. (c,d) Graph showing the electrical resistance of single NW devices made of Au and Pd vs W_{NW}, respectively.

be realized with optical lithography, as we have demonstrated. Changing the length of the initial beam structure by 500 nm leads to around 2 nm difference in the NW width, thereby allowing very fine control of NW dimensions, even for large tolerances in the pattern generation of the initial beam structures. It is worth noting that the Pd NWs tend to be wider than the Au NWs.

To investigate the reason of this difference and test the versatility of our approach in terms of NW materials, we produced single NW structures made of various materials such as gold, platinum, palladium, tungsten, tin, and metal oxides (Figure S2). We observed that the suspended shadow mask behaves as a bimorph cantilever, bending out of plane. This bending mostly occurs during the evaporation, as the deposited material on the suspended shadow masks cools down. The amount of bending is a function of the temperatures, thicknesses, and thermal and mechanical properties of the deposited NW material and the TiN layer of the shadow mask, and it should be therefore predictable and repeatable. Longer cantilevers are softer, so bending has a stronger influence than on short cantilevers. Importantly, it was observed that the extent of shadow mask bending is a function of the out-of-plane stiffness of the cantilevers in the shadow mask layer, as well as the thickness and mechanical properties (such as residual stress and elastic modulus) of the deposited material(s). In particular, it appears that the deposition of Pd generates more out-of-plane bending in the shadow mask as compared to that of Au. Nevertheless, the resulting nanogap widening is not exceeding 10% of the initial W_{NG}.

Complete Single NW Devices with Self-Aligned Contact Pads. The formed NWs are connected to large areas that are used for electrical contacts. To establish an optimal electrical connection, it is useful to have a thicker layer of conductive materials than the one forming the NWs. In our approach, a thick layer for contact metallization can be obtained during the same deposition step that produces the thinner NWs. When a sufficiently thick layer of the NW material is deposited, narrow nanogaps become closed off, which can be exploited for self-aligned metallization, or passivation, of the electrical contacts (Figure 3a). The closing of nanogaps is the result of deposition of the evaporated material at the edges and sidewalls of the shadow mask in the nanogap areas. This deposition-induced nanogap narrowing is significant when W_{NG} approaches the thickness of the evaporated material, which is the case for our sub-20 nm crack-defined nanogaps. Here, we exploit nanogap closure to form self-aligned contact pads at the end of nonmetallic NWs for easy device integration without any additional lithographic step (Figure 3b). In fact, more of the same or different materials can be deposited for electrical connection or passivation of the areas connected to the NW, without being deposited on the NW site. As a proof of concept, we deposited tin oxide (SnO_2) to form single NW devices until the nanogaps were closed. Then, we deposited Au as the electrical contact layer. During this deposition, the SnO_2 NW was protected by the closed nanogap in the shadow mask, while the large areas at the ends of the NW were metalized in a self-aligned fashion. In the atomic force microscopy (AFM) image, the metal oxide NW can be distinguished from the rest of the thicker Au-coated surfaces (Figure 3c). As an additional feature, self-aligned passivation of metal contacts can be obtained when an electrically insulating material is evaporated after nanogap closure.

The self-aligned metallization and passivation concepts also work without nanogap closure, which is, for example, the case when the cantilevers in the shadow mask exhibit significant

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out-of-plane deformation after the deposition of a specific combination of materials and thicknesses (Figure 3d). This is the case for certain combinations of materials and thicknesses (see Figure S2 in the Supporting Information). In this case, it is possible to selectively metalize or passivate the probing pad areas at the NW ends by exploiting angled evaporation in combination with the high aspect ratio between the nanogap height and width (Figure 3e).[52] The high aspect ratio of the nanogap prevents the formation of a second NW made of Au, allowing metallization of the contacts without short-circuiting or covering the NW. As a proof of concept, we deposited tungsten oxide (WO_3) to form single NW devices by positioning the surface of the sample perpendicularly to the vapor incidence direction. We then tilted the sample to achieve 45° of inclination between the normal of the sample surface and the vapor incidence direction and deposited a Au layer. SEM analysis confirmed the successful metallization of the contact pad areas without the formation of a second NW structure made of Au (Figure 3f). The resulting metal contacts are not positioned at the exact extremities of the NW because the angle of the deposition shifts the position of the Au notches with respect to the previously formed NW.

Electrical Characterization of Au and Pd Single NW Devices. To establish that the controlled NW geometry translates into a precise predictable electrical behavior of the NWs, we characterized the electrical resistance of different Au and Pd NWs, using a four-point measurement configuration (Figure 4a). The Al_2O_3 etching undercuts the shadow mask layer, preventing short-circuiting between the shadow mask layer and the single NW devices. In this way, electrical probing of the NWs could be performed directly after evaporation, without the need for further processing steps. As previously described, the formed NWs were readily connected to electrical probing pads consisting of the respective metal material. We have found a linear Ohmic-like behavior in the 0.1−1 mV range while cycling the current through the NW devices (Figure 4b). We then tested the resistance of NWs with respect to their width for both Au and Pd NWs. The resulting values of resistance are demonstrating control and predictability of the NW resistances based on the design parameters of the crack-defined nanogaps in the shadow mask.

Moreover, we plotted the resistance of NWs with respect to their width for Au and Pd NWs (Figure 4c,d). The resistance of the NWs expectedly decreases with increasing W_{NW}, confirming the ability to control the resistance of the NW structure via the width of the crack-defined nanogaps of the shadow mask. The electrical resistance of the formed single NWs has a nonlinear dependence of the W_{NW} for both metals. This nonlinear dependence is partially due to the gap narrowing effects during evaporation. The decreasing W_{NG} is affecting the amount of material deposited on the substrate and so the NW thickness t_{NW}. As a consequence, the NW cross section is decreased, which was confirmed by the AFM measurements of the t_{NW} for different W_{NG} (Figure S3). The reduction in t_{NW} is also reflected in the increasing standard deviation of the resistance and in the decreasing yield of obtaining electrically measurable NWs for increasingly narrow NWs. This is particularly noticeable for Au NWs, for which almost no out-of-plane deformation of the shadow mask occurs to compensate for the gap narrowing. Another factor potentially contributing to the nonlinear behavior observed in Figure 4c is the electrical properties of thin metallic films and NWs with decreasing material thickness. For sub-20 nm thick films, the resistivity can increase by orders of magnitude because of surface scattering and grain boundary effects, as described by Fuchs−Sondheimer and Mayadas−Shatzkes models.[53−55]

DISCUSSION

The presented methodology allows the fabrication of single NW devices in a scalable fashion. The large number of devices that can be reliably produced in a short time is interesting both for industrial applications, where single NW devices have to be produced in large quantities and for rapid and scalable prototyping in a research environment. In fact, the manual isolation of individual NWs and contact patterning for a very limited number of devices takes comparable or even longer time than a full wafer processing round with our technique, which can produce up to 5000 single NW devices per square centimeter simultaneously using space-efficient management of probing pads. Moreover, the nanoscale patterns are formed by controlled-crack formation in the TiN layer, which is induced by built-up of stress during the wet etching of the Al_2O_3 sacrificial layer. This high-yield batch process bypasses the needs for stencil reusability and the challenges associated with the cleaning of conventional stencils with sub-20 nm features. Instead, a limit of our technique is that only narrow lines can be produced by controlled crack lithography. Although this is a limitation to the general use of crack-defined nanogaps for the manufacturing of shadow masks and stencils, it is perfectly fitting the application as shadow masks for single NW devices.

The predictable and controllable dimensions of the crack-defined nanogaps in the shadow mask are passed on to the NWs during the evaporation step, as confirmed by the SEM, AFM, and electrical results. The described process can be used to form single NWs featuring controlled positions, dimensions, and widths as narrow as 13 nm. The characterized values of the electrical resistance of the single NW devices are constant given a specific design and well-discriminated between different designs (Figure 4c,d). Therefore, the effective cross section of the NWs can be controlled with the microscale lithographic pattern of the shadow mask layer. This is a further confirmation of the ability to control the NW geometry with nanoscale precision. This level of dimension control, coupled with the ability to generate different NW geometries in terms of thickness and width on the same substrate, is the main advantage of this technique with respect to previous reports of cracking-assisted fabrication.[41,43] Moreover, the TiN layer is a hard mask that is compatible with high temperature or ultrahigh vacuum deposition. Compared to conventional stencil lithography, the use of controlled crack formation in suspended beam structures allows us to bypass the challenges associated with fabricating nanogaps in shadow masks while preserving the nanometric precision in geometries and positions. Additionally, ALD Al_2O_3 and TiN are widespread processes that are known to be highly uniform in thickness and in material properties over large wafer sizes, which is why they have made it to the semiconductor industry.[56] Thus, we expect our methodology to be readily scalable to larger wafer sizes without compromising on the uniformity of the NW dimensions.

However, ALD TiN is a polycrystalline material that preferentially cracks along grain boundaries.[47] The jagged geometry of the crack path affects the geometry of the nanogap and ultimately of the NW. Solutions to improve this issue include lowering the grain size by means of lowering the

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substrate temperature, although care has to be taken to avoid affecting the residual tensile stress responsible for the controlled crack formation. Another solution would be to use a single-crystalline material instead of the polycrystalline TiN layer. This approach could potentially also improve the predictability of the crack path but would severely limit process integration and accessibility of the method.

The presented technique is compatible with different NW geometries and evaporated materials but has constraints in the fundamental limits of shadow mask lithography. It is not possible to form single-crystalline NWs using electron beam evaporation. In this sense, our work does not compete with technologies based on the bottom-up growth of single-crystalline NWs of well-established materials such as silicon or zinc oxide. Instead, the technique provides an opportunity to generate NWs of individually controlled geometry and position from materials which are not available in the former approach. The compatibility of shadow masking with PVD implies that virtually any PVD-compatible material is compatible. The growth mechanisms by island coalescence is also affecting the possible geometries and degree of crystallinity of the NWs. The evaporated material landing on the surface of the substrate grows by first forming disconnected islands. The surface diffusion and the critical thickness that the islands need to reach for coalescence are fundamental limits to the minimum thickness and cross section of NWs formed by evaporation on a nonengineered surface. Moreover, the electrical conduction is influenced by tunneling and hopping-assisted transport between the NW grains.[57] To improve the conduction and lower the resistance of the NWs, the substrate could be treated prior to deposition to limit that diffusion and enhance the growth of more crystalline (larger grain size) NWs. Another approach is to increase the deposited thickness to be well above the average grain size of the NW material to achieve the standard value of sheet resistance values. We have shown that our technique is compatible with a relatively thick sacrificial layer (up to 200 nm for the EBL-defined nanogaps), which allows for thicker films or stacks of different materials while still ensuring electrical insulation from the top TiN layer. Nevertheless, the observed $I-V$ relations of the formed NWs are Ohmic-like in the 0.1−1 mV range. This linear $I-V$ behavior in the low-power regime is ideal for sensing application.

A common issue in shadow mask lithography is the blurring, defined as a broadening of the geometrical dimensions of the evaporated structure of the substrate with respect to the shadow mask feature.[58,59] In our study, the high crack height to crack width aspect ratio tends to limit the geometrical blurring, and the halo-blurring effect caused by the surface diffusion of the material atoms landing on the substrate was minimized by the low substrate temperature and deposition rate. As a result, we could not observe any significant blurring affecting the NW geometry.

CONCLUSIONS

In summary, we have developed a method utilizing scalable shadow mask lithography to produce single NW devices featuring sub-20 nm NW widths. A wide range of materials can be used for the NWs with a variety of electrical, chemical, and optical properties. By relying on controlled crack formation to generate the nanogaps in the shadow mask, we were able to form nanoscale structures using a scalable manufacturing approach. We prepatterned the shadow mask with >200 nm critical feature size and formed crack-defined nanogaps with sub-20 nm controllable widths. We have also demonstrated the compatibility of this fabrication method with i-line stepper lithography, thus achieving a 20-fold improvement in resolution with respect to the nominal resolution of our stepper. The combination of scalable manufacturing, dimensional control, and self-alignment of the NWs to the electrical contacts and probing pads makes this approach attractive for large-scale realization of NW devices targeted at applications in gas sensing, micro-optics, and spintronics. Additional features such as cantilever removal, nanogap closure, and angle evaporation allow the fabricated single NW devices to work in in-liquid conditions and the possibility to contact non-metallic NWs without additional fabrication complexity.

EXPERIMENTAL SECTION

Fabrication of Crack-Defined TiN Shadow Masks Defined by EBL. A 100 mm diameter, 525 μm thick p-doped single-crystalline silicon wafer (100) was used as the substrate. A 2.5 μm thick SiO_2 layer was thermally grown on the silicon wafer by wet oxidation. Then, a 200 nm thick layer of Al_2O_3 and a 70 nm thick layer of TiN were deposited successively using ALD without breaking the vacuum in between the two deposition steps. Al_2O_3 was deposited at a temperature of 200 °C in 2000 cycles using trimethylaluminum (pulse time 70 ms, purge time 500 ms) and water (H_2O, pulse time 175 ms, purge time 750 ms) as precursors. TiN was deposited at a temperature of 350 °C in 2000 cycles using titanium tetrachloride ($TiCl_4$) (pulse time 150 ms, purge time 500 ms) and ammonia (NH_3) (pulse time 1 s, purge time 1 s) as precursors. The probing pads and notched beam structures were patterned in the TiN film using a 180 nm thick e-beam lithography mask (positive resist, ZEP7000, Zeon Chemicals, Japan; exposed in a Raith e-beam system at 25 keV acceleration voltage with an area step size of 8 nm and an area dose of 84 μA s/cm^2) in combination with an anisotropic plasma etch (Applied Materials Precision 5000 Etcher) at a chamber pressure of 200 mTorr and a radio frequency (RF) power of 600 W in a mixture of boron trichloride (BCl_3) at 40 sccm flow, chlorine (Cl_2) at 15 sccm flow, nitrogen (N_2) at 15 sccm flow, and tetrafluoromethane/oxygen (CF_4/O_2) at 15 sccm flow. The resist mask was subsequently removed by a combination of wet stripping with a remover (Rem700, Micro Resist Technology, Germany) at 60 °C for 120 s and a dry plasma cleaning (PVA TePla model 300 Plasma System). The ashes resulting from the plasma cleaning were removed by rinsing the samples with a remover (Microposit remover 1165, MicroChem). The beam structures were released by the sacrificial isotropic etching of the Al_2O_3 layer in a KOH bath at room temperature for 80 min, forming the cracks in the beam structure and thereby creating the nanogaps that were used to define the NW structures. Thereafter, the devices were dried using a critical point dryer (BalTec CPD 408), thus preventing stiction of the suspended cantilevers to the substrate by avoiding liquid−air interfaces in the drying process.

Fabrication of Stepper-Defined Shadow Masks Defined by Stepper Lithography. For this experiment, the same substrate and material stacks were used but with different layer thicknesses (50 nm Al_2O_3, 70 nm TiN). The notched bridges in the TiN layer were first defined in a resist mask (MEGAPOSIT SPR-700) on the wafer scale using a projection stepper system (Nikon NSR TFHi12 I-line Stepper, dose 190 mJ/cm^2). The resist mask was hard-baked for 60 s at 110 °C. The resist mask was transferred to the TiN layer by an anisotropic plasma etch (Applied Materials, Precision 5000 Etcher, at a chamber pressure of 200 mTorr and an RF power of 600 W using a mixture of BCl_3 at 40 sccm flow, Cl_2 at 15 sccm flow, CF_4-O_2 at 15 sccm flow, and N_2 at 15 sccm flow for 40 s). The resist mask was subsequently removed with a remover (MicroResist Rem-700) at 60 °C for 5 min. The TiN-notched bridges were released by wet chemical etching of the aluminum oxide sacrificial in an aluminum etch solution (MicroChemicals) for 35 min at 65 °C.

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Formation of Single NW Devices by PVD through Crack-Defined Shadow Masks. We used the TiN shadow mask with the cracked cantilevers to define single NWs with connected electrical probe pads on the SiO_2−Si substrate using a Provac PAK 600 electron beam evaporation system. The NWs were generated by line-of-sight evaporation through the defined cracks on the cantilevers of the shadow mask. To obtain line-of-sight evaporation, the chips with the shadow mask were mounted on the planetary holder of the evaporator at a distance of 50 cm from the material crucible, with the cantilever plane being at a 90° angle with respect to the direction of the impinging evaporated molecules. The planetary holder with the material target was kept still (no rotation) during evaporation. The processing chamber was kept at a pressure of below 7×10^{-7} mbar, providing a long mean free path for the molecules. To improve the resolution of the fabricated NWs, we attempted to reduce the average dimension of the evaporated particles by keeping the material deposition rate below 0.4 Å/s. This was achieved by setting the electron beam parameters to 15 kV and 80 mA. Minimizing the electron beam power also helped in reducing out-of-plane bending of the suspended cantilevers,[60] resulting from thermal expansion mismatch between the TiN cantilevers and the deposited NW material. To demonstrate the flexibility of our methodology in terms of materials for the NWs, we realized and evaluated Au and Pd NWs. To promote material growth and enhance adhesion to the substrate, a 2 nm layer of chromium (Cr) was evaporated, prior to deposition of the desired NW material. Information about the evaporation of other materials is available in the Supporting Information.

SEM Evaluation of W_{NG} in Shadow Masks and Resulting NW Widths. All NW designs were evaluated by measuring both the widths of the nanogaps in the shadow mask and of the resulting NWs using a ZEISS Ultra-55 SEM with no sample tilt. Each data point in Figure 2b,c corresponds to the average of the measurements of five devices, and the error bar corresponds to the reading error of W_{NG} from the SEM images. The image resolution was 2048 × 1536 pixels or higher, and the minimum magnification was 180 000×. The measurement error of W_{NG} and W_{NW} using the SEM images was estimated to be 2 nm and it was caused by a combination of image blur of the edges of the nanostructures during image acquisition and manual placement of the measurement bars to define the NW edges using the built-in software measurement tool. The linear fits are obtained using the least squares method with regression through the origin. For top-view SEM images, the shadow masks were removed after PVD of the NW material, by applying an adhesive tape on the shadow mask layer and then removing the tape together with the suspended cantilevers.

Sample Preparation and AFM Thickness Evaluation of NW Structures. To perform an AFM analysis of the NW structures, the suspended cantilevers were removed after the evaporation step. This was done by applying an adhesive dicing tape (1007R-8.5 Silicone Release Agent-free Blue Adhesive Plastic Film, 80 μm thickness, SPS-Europe BV, The Netherlands) on the TiN layer so that the suspended shadow mask cantilevers could adhere to the tape. When the tape was stripped from the sample, most of the suspended cantilevers were mechanically removed. A successive rinsing with deionized water removed debris generated during the removal procedure (see the Supporting Information). After cantilever removal, the NW structures were analyzed using a Bruker FastScan AFM system in in-liquid peak force mode.

Electrical Characterization of the Single NW Devices. The NW structures were connected to electrical probing pads in the same layer and made of the same material. The insulating substrate (SiO_2) ensured electrical conduction through the NW structure only. We also verified the electrical isolation of single NW devices with respect to the rest of the shadow mask layer, by placing one probe on the contact pads of the NW device and one on the surrounding TiN layer, measuring resistances larger than GΩ. The line-of-sight deposition through the suspended shadow mask resulted in electrical insulation of the single NW devices on the SiO_2 substrate with respect to the TiN shadow mask layer and thus testability of the single NW devices. Single NW devices were tested using a Cascade Summit 11000 semiautomated probe system and a Keithley 4200-SCS semiconductor characterization system in a four-probe configuration. For the $I-V$ curves, we swept the current from 200 nA to 1 μA and measured the voltage drop across the NW. After the set current reached 1 μA, the current was ramped in the opposite direction to return to 200 nA in order to detect possible hysteretic effects. The measurements were performed at (23.5 ± 1) °C and at (30 ± 1)% relative humidity. Each data point presented in Figure 4c,d corresponds to the average of the electrical resistance measurements of up to five devices. NWs whose resistance was too high to be properly measured were discarded in this graph. The error bar corresponds to the standard deviation.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.8b19410.

Set of NW designs; material flexibility and limitation of our shadow masking technique; and effect of gap narrowing and closure on the thickness of NWs (PDF)

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Author Contributions

A.E. and V.D. contributed equally. V.D. proposed and demonstrated the concept by designing and fabricating sample structures. A.E. fabricated and characterized all the devices. A.E. analyzed the data. A.E. and V.D. co-wrote the manuscript. A.E., V.D., F.N., and G.S. discussed the results and commented on the manuscript. The manuscript was written through the contributions of all authors. All authors have given approval to the final version of the manuscript.

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Notes

The authors declare no competing financial interest.

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