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# Small-Area Radiofrequency-Energy-Harvesting Integrated Circuits for Powering Wireless Sensor Networks

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**Abstract:** This study presents a radiofrequency (RF)-energy-harvesting integrated circuit (IC) for powering wireless sensor networks with a wireless transmitter with an industrial, scientific, and medical (ISM) of 915 MHz. The proposed IC comprises an RF-direct current (DC) rectifier, an over-voltage protection circuit, a low-power low-dropout (LDO) voltage regulator, and a charger control circuit. In the RF-DC rectifier circuit, a six-stage Dickson voltage multiplier circuit is used to improve the received RF signal to a DC voltage by using native MOS with a small threshold voltage. The over-voltage protection circuit is used to prevent a high-voltage breakdown phenomenon from the RF front-end circuit, particularly for near-field communication. A low-power LDO regulator is designed to provide stable voltage by using zero frequency compensation and a voltage-trimming feedback. Charging current is amplified N times by using a current mirror to rapidly and stably charge a battery in the proposed charger control circuit. The obtained results revealed that the maximum power conversion efficiency of the proposed RF-energy-harvesting IC was 40.56% at an input power of  $-6$  dBm, an output voltage of 1.5 V, and a load of 30 k $\Omega$ . A chip area of the RF-energy-harvesting IC was  $0.58 \times 0.49$  mm<sup>2</sup>, including input/output pads, and power consumption was 42  $\mu$ W.

**Keywords:** radiofrequency; ISM 915 MHz; energy-harvesting IC; native MOS; Dickson voltage multiplier; over-voltage protection circuit; low-dropout regulator; charger control circuit

## 1. Introduction

Energy harvesting for supplying power to low-power electronic devices has recently become mainstream research. The lifetime of a battery can be extended using a developed self-sustainable power supply. Bito et al. designed a flexible wearable radiofrequency (RF) energy harvester for off-the-shelf two-way talk radios of 2 W using inkjet printing technology, and E- and H-field energy harvesters were verified using a light-emitting diode and microcontroller communication module [1]. Tian et al. presents an integrated solution for a flexible direct current (DC)–DC converter by embedding a flexible polyimide printed circuit board and an inductor made of flexible ferrite-polymer composite in a wire [2]. A wearable RF-energy-harvesting device, which comprises a U-shaped dipole antenna, matching network, RF-DC converter, and DC–DC converter, was presented in [3] for supplying power to smart jewelry. This design converts a 915-MHz RF signal into a constant DC output voltage of 3.1 V at an input power of  $-6$  dBm, which is suitable for supplying power to a fitness monitor pendant

under standby mode. An experimental comparison in [3] shows that the Dickson topology has high efficiency at a high input power.

A commercial power supply or battery can be used as a stable power source for providing power to wireless sensor networks (WSNs). However, these power supplies have a finite lifetime, have a large size, incur high maintenance cost, and cause environmental pollution. RF energy harvesting was introduced because of potentially long lifespan, low-power consumption, and small size [4]. In this process, ambient energy is emitted from various sources, such as television (TV), radio, wireless Internet, satellite communication, and base stations, which is converted into feasible DC voltages. WSN devices powered by RF energy can be used in several applications, such as telemetry systems, RF tags, home automation, equipment monitoring, access control, and prolongation of lifespan of powered devices [5,6]. In [7], a five-stage orthogonally switching charge pump rectifier with a voltage boosting network was used for an RF energy harvester. The rectifier provides a DC voltage and power conversion efficiency (*PCE*) of 1.3 V and 33.72%, respectively, with a load of 100 k $\Omega$  from an RF source of  $-13$  dBm at an ISM frequency.

The WSNs are fabricated using low-power circuits, particularly by integrating with an antenna and a voltage multiplier for a stable power supply [8,9]. A combination of a two-stage Villard multiplier with a three-stage Dickson voltage multiplier was proposed to increase output voltage and power efficiency [10]. A Villard–Dickson power harvester circuit can produce an output voltage of 4 V with an efficiency of 3.9% and an output voltage of 8.8 V with an efficiency of 14.6% without and with a matching circuit, respectively, at an input signal of 4.1 dBm from a TV station [10]. A microstrip matching circuit and zero-biased diode were used to improve the performance of the designed energy-harvesting device.

The Internet of Things (IoT) is a well-known platform, wherein each physical object is connected to the Internet without requiring human interaction. Few people check for regular supply of power to IoT, excluding WSNs. To supply power to these communication devices for a long duration, a self-sustainable power system is required for complex networks [11]. A feasible technique is to harvest RF energy from external environmental sources, which could be used as an auxiliary power supply for increasing the battery life [12,13]. In general, RF energy-harvesting bands from ISM (900–928 MHz) and WLAN (2.4/5 GHz) have received considerable attention because they can cover cities and countries due to their continuous emission as commercial bands [14–16]. In [17], RF energy harvesting employed a Wi-Fi band at a frequency of 2.4 GHz by using the P21XXCSR-EVB evaluation board from Powercast. Four types of antennas and an RF-energy-harvesting evaluation board are included in this research. Experiments have shown that power losses in air and antennas have a stronger effect on the total efficiency of the system than the losses in the RF energy harvester. The RF-energy-harvesting system can be improved using antenna arrays, particularly for supplying power to low-power sensors and IoT devices.

Most previous studies have used an individual energy-harvesting source to supply power to low-power sensors and IoT devices. However, the available environmental energies affect the input power of the RF transmitter (Powercast Corporation) at a frequency of 2.4 GHz. Sensors and IoT devices are always installed on the ceiling of a room. For uniform RF transmission and increasing communication distance, this study employed a TX91501 RF transmitter from Powercast Corporation [18], which provides an output power of 3 W at an ISM band of 915 MHz, with a maximum transmission distance of 12–15 m. Moreover, a 1-dBi bipolar antenna was used as a receiving antenna to design an RF-energy-harvesting chip. Figure 1 shows the proposed RF-energy-harvesting system, which includes a Powercast transmitter, receiving antenna, RF-energy-harvesting IC, and power source.

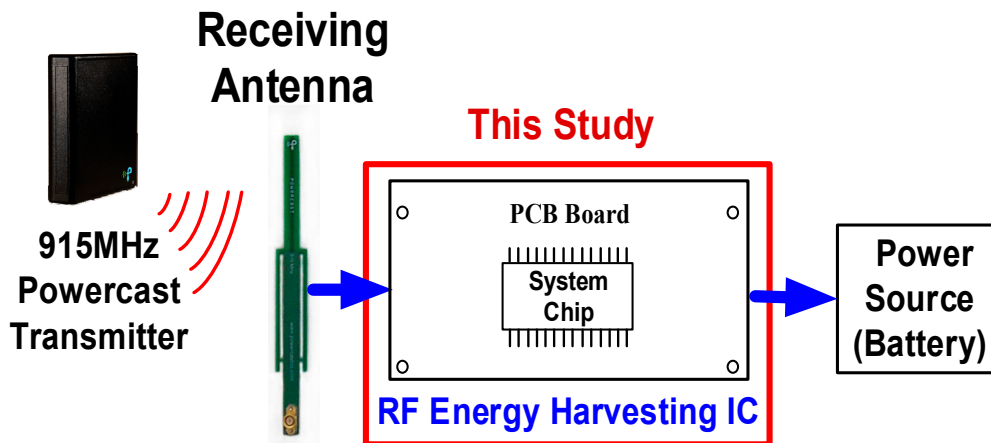


Figure 1. Proposed RF-energy-harvesting system.

The following section elucidates the circuit topology of the designed RF-energy-harvesting IC. Sections 3 and 4 present the simulated and measured results and conclusions, respectively.

## 2. Circuit Topology of RF-Energy-Harvesting Integrated Circuit

Figure 2 shows a functional diagram of the RF-energy-harvesting IC, which receives RF energy from the receiving antenna, and this energy charges energy storage devices. Thus, the proposed IC is used as a backup stable power source. An off-chip matching network from MuRata Manufacturing Co. Ltd. was used to guarantee maximum power transfer. The RF-DC rectifier received the transferred RF energy from a matching network and converted this energy into DC voltage. An over-voltage protection circuit was then designed to protect the RF-DC rectifier when the output voltage of the designed rectifier was higher than the breakdown voltage [19]. A stable voltage of 1.5 V is passed through the low-power LDO circuit and sent to the charging control circuit for charging storage devices such as a battery.

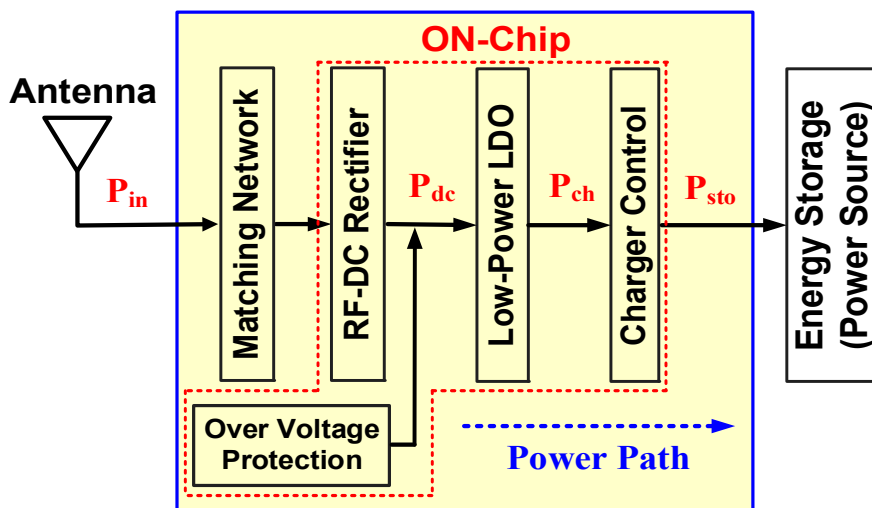


Figure 2. Functional diagram of RF-energy-harvesting IC.

### 2.1. Matching Network

Because of an antenna impedance of  $50 \Omega$ , the input impedance of the matching network must be matched to  $50 \Omega$ . This matching circuit is used to not only guarantee maximum power transfer but also obtain maximum conversion efficiency. If the matching network includes capacitor  $C$  and inductor  $L$ , maximum power transformation is obtained from an antenna to a load. Source impedance

$R_a$  must be equal to the conjugate input impedance  $Z_{in}$  of the matching network [20]. The maximum output power  $P_{L,max}$  can be expressed as follows:

$$P_{L,max} = |I_a|^2 \times \Re[Z_{in}] = \frac{V_a^2}{4R_a} \quad (1)$$

where  $V_a$  is the peak voltage of the antenna.  $I_a$  and  $Z_{in}$  are the input current and input impedance of the matching network, respectively.

In this study, the impedance of the antenna and the input impedance of the RF-DC rectifier were  $50 \Omega$  and  $240.4 - j473.9 \Omega$ , respectively. The impedance of the matching network must be equal to  $50 \Omega$  [21]. Simulations were performed with ADS software and component datasheet provided from MuRata Company, and inductor  $L$ , labeled as LQG15HS\_02, and capacitor  $C$ , labeled as GRM15, were used to complete the matching network. Moreover, authors paid more attention toward self-resonant frequencies (SRFs) for selecting a suitable inductor. The operating frequency of the matching network must be lower than the SRF of the selected inductor. The larger the inductor is, the smaller the SRF is. For example, the minimum SRFs were 1000 and 800 MHz for  $L \leq 47 \mu\text{H}$  and  $L \geq 56 \mu\text{H}$ , respectively. If input power was set to  $-10 \text{ dBm}$  at an operating frequency of 915 MHz, a suitable inductor lower than  $47 \mu\text{H}$  was selected.

## 2.2. RF-DC Rectifier

For an  $N$ -stage rectifier, a pair of a metal-oxide-semiconductor field-effect transistor [MOSFET ( $M_p$ )] and capacitor ( $C_p$ ) can be considered as a rectifier with a small ripple voltage across  $C_p$ . An averaged output voltage of the  $(p + 1)^{\text{th}}$  stage can be expressed as follows:

$$V_{O(p+1)}(V) = V_{O(p)}(V) + V_{boost}(V), \quad (2)$$

where  $V_{O(p)}$ ,  $V_{O(p+1)}$ , and  $V_{boost}$  are the output voltage of the  $p^{\text{th}}$  stage (present voltage), output voltage of the  $(p + 1)^{\text{th}}$  stage (next voltage), and incremental voltage of each stage [22], respectively. Approximation in charge computation was used to provide the incremental voltage  $V_{boost}$  as follows:

$$V_{boost}(V) = V'_{in} - V_{tn} - \left( \frac{15\pi}{8} \times \frac{I'_{Oeff} \sqrt{2V'_{in}}}{\mu_n C_{ox}(W/L)} \right)^{2/5}, \quad (3)$$

where  $V'_{in}$ ,  $V_{tn}$ ,  $I'_{Oeff}$ ,  $\mu_n$ , and  $C_{ox}$  are an effective voltage amplitude, the threshold voltage of an NMOS transistor, effective loading current, electron mobility, and a gate oxide capacitor, respectively.  $W$  and  $L$  are the width and length of the MOSFET, respectively.  $I'_{Oeff}$  and  $V'_{in}$  can be given as follows:

$$I'_{Oeff} = I_0 + \frac{I_{S0}}{\pi} \left( \frac{W}{L} \right) \left( 1 - e^{-V'_{in}/V_T} \right) \left( 1 + \lambda_{sub} V'_{in} \right), \quad (4)$$

$$V'_{in} = \frac{C_t}{C_t + C_{par}} \quad (5)$$

where  $I_0$ ,  $I_{S0}$ ,  $V_T$ ,  $\lambda_{sub}$ ,  $C_t$ ,  $C_{par}$ , and  $V_{in}$  are the initial loading current, saturation current, thermal voltage, channel length modulation coefficient, total capacitance value of all capacitors, parasitic capacitance at each stage, and peak amplitude of an input signal of a voltage rectifier, respectively.

If the body effect is ignored, the output voltage of the  $N$ -stage rectifier is as follows:

$$V_{ON}(V) = N \times V_{boost}(V) = N \times \left( V'_{in} - V_{tn} - \left( \frac{15\pi}{8} \times \frac{I'_{Oeff} \sqrt{2V'_{in}}}{\mu_n C_{ox}(W/L)} \right)^{2/5} \right), \quad (6)$$

According to the simulation results, many rectifiers are used for achieving the maximum efficiency. For example, 2-, 4-, 6-, 8-, 10-, and 16-stages are designed with respect to different loading currents or peak voltages [22]. For a rapid charging mechanism and stable power source at an operating frequency of 917 MHz, this study adopted a 6-stage voltage rectifier with a small threshold voltage of 0.45 V.

Figure 3 shows a single-ended 6-stage Dickson voltage multiplier, which was published in [22]. It includes 6 diode-connected MOSFETs ( $M_1$ – $M_6$ ) and 6 capacitors ( $C_1$ – $C_5$  and  $C_L$ ). All transistors and capacitors are identical. A bottom plate, which is marked using a bold line, exhibited a large parasitic capacitance. It is grounded to reduce loss or is connected to the input terminal  $RF_{in}$ , which is fed from the matching network.

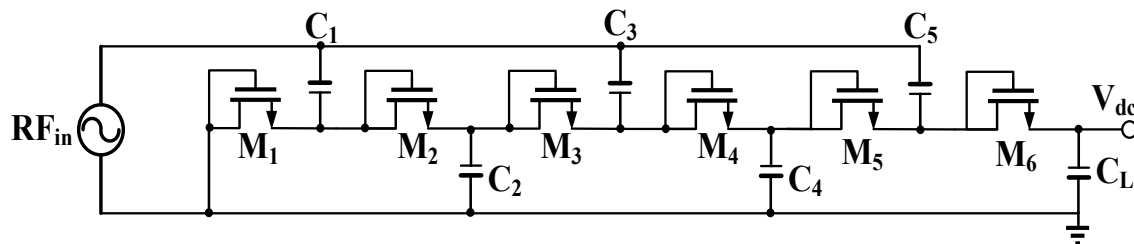


Figure 3. Six-stage Dickson voltage multiplier circuit.

If the input signal of the voltage rectifier was sinusoidal with  $RF_{in} = V_{in} \cos 2\pi ft$ , where  $V_{in}$  and  $f$  are respectively the peak amplitude and operating frequency, the DC output voltage  $V_{dc}$  could be obtained for a charge transfer with a load capacitor  $C_L$ . The capacitor is sufficiently large to store the transferred charge and to reduce the output ripple voltage [22].

If the voltage multiplier was in a steady state,  $RF_{in}$  was greater than or equal to zero for  $0 \leq t \leq \pi/4$  and  $3\pi/4 \leq t \leq \pi$ , and  $RF_{in}$  was less than or equal to zero for  $\pi/4 \leq t \leq 3\pi/4$  in the first time cycle  $T$  ( $= 1/f$ ).  $RF_{in}$  charged the capacitor  $C_1$  through the MOSFET  $M_1$  for  $RF_{in} \leq 0$ , and a steady voltage of  $V_{in} - V_{TH}$  was then stored in  $C_1$  by reducing a threshold voltage  $V_{TH}$ . Voltage was subsequently changed to  $V_{in} + (V_{in} - V_{TH})$  across the capacitor  $C_1$  for  $RF_{in} \geq 0$ .  $M_2$  was the conducting MOSFET, and the voltage of  $C_2$  was charged to  $2 \times (V_{in} - V_{TH})$  by reducing a threshold voltage  $V_{TH}$  of  $M_2$ . In the second time cycle ( $2T$ ),  $RF_{in}$  charged the capacitor  $C_2$  to  $V_{in} + 2 \times (V_{in} - V_{TH})$  for  $RF_{in} \leq 0$ , and a steady voltage of  $3 \times (V_{in} - V_{TH})$  was passed through  $M_3$  and stored in  $C_3$ . For  $RF_{in} \geq 0$ , the voltage of  $C_3$  was abruptly changed to  $V_{in} + 3 \times (V_{in} - V_{TH})$ , and  $M_4$  was the conducting MOSFET. A steady voltage of  $4 \times (V_{in} - V_{TH})$  was generated across the capacitor  $C_4$ . After the third time cycle ( $3T$ ) was completed, a steady voltage of  $6 \times (V_{in} - V_{TH})$  was generated without a body effect across the load capacitor  $C_L$ . The ideal output DC voltage  $V_{dc}$  could be expressed as follows:

$$V_{dc}(V) = 6 \times (V_{in} - V_{TH}), \quad (7)$$

Equation (7) indicates that the larger the threshold voltage  $V_{TH}$  is, the smaller the DC output voltage  $V_{dc}$  is. Threshold voltage  $V_{TH}$  is highly correlational to a semiconductor process. A conventional CMOS has an inherent threshold voltage of approximately 0.45 V for the standard TSMC 0.18 process, whereas a low threshold voltage of 28 mV was obtained using a conventional MOS. The conventional MOS was used to not only develop a new RF-DC rectifier but also to enhance power efficiency, particularly for an ultra-low input power of less than  $-10$  dBm.

### 2.3. Over-Voltage Protection Circuit

Figure 4 presents an over-voltage protection circuit used to prevent the occurrence of a high-voltage breakdown phenomenon during NFC [19]. The output DC voltage  $V_{dc}$  of the RF-DC rectifier was

connected to the proposed protection circuit, and two PMOSs ( $M_1 - M_2$ ) and two NMOSs ( $M_8 - M_9$ ) were diode-connected. Two bias voltages  $V_A$  and  $V_B$  could be expressed as follows:

$$V_A = V_{dc} - (|V_{OD1}| + |V_{tp1}|) - (|V_{OD2}| + |V_{tp2}|), \quad (8)$$

$$V_B = V_{OD9} + V_{tn9}, \quad (9)$$

where  $V_{ODi}$ ,  $V_{tpi}$ , and  $V_{tni}$  are the overdrive voltage of the  $i^{\text{th}}$  MOSFET, threshold voltage of the  $i^{\text{th}}$  PMOS, and threshold voltage of the  $i^{\text{th}}$  NMOS. Under a common-mode operation, the two bias voltages were identical (i.e.,  $V_A = V_B$ ). The DC output voltage of the RF-DC rectifier can be expressed as follows:

$$V_{dc} = (|V_{OD1}| + |V_{tp1}|) - (|V_{OD2}| + |V_{tp2}|) + (V_{OD9} + V_{tn9}), \quad (10)$$

Furthermore, the two bias voltages  $V_A$  and  $V_B$  could be derived from resistors ( $R_1 - R_2$ ,  $R_{ds1} - R_{ds2}$ , and  $R_{ds8} - R_{ds9}$ ). Thus, the following can be derived:

$$V_A = \frac{R_1}{R_{ds1} + R_{ds2} + R_1} \times V_{dc}, \quad (11)$$

$$V_B = \frac{R_{ds9}}{R_2 + R_{ds8} + R_{ds9}} \times V_{dc}, \quad (12)$$

where  $R_{dsi}$  was the conduction impedance of the  $i^{\text{th}}$  diode-connected MOSFET, which is expressed as  $(g_{mi} + g_{mbi})^{-1}$  with the transistor transconductance  $g_{mi}$  and body effect transconductance  $g_{mbi}$ .  $R_1$  and  $R_2$  are constant resistors. The larger the bias current  $I_{Ri}$  of the  $i^{\text{th}}$  resistor is, the larger the transconductance  $g_{mi}$  is and the smaller the conduction resistor  $R_{dsi}$  is.

If the output DC voltage  $V_{dc}$  of the RF-DC rectifier was higher than the aforementioned voltage [Equation (11)], the bias voltage  $V_A$  was larger than the bias voltage  $V_B$  because of the reduced conduction impedance  $R_{dsi}$  with the large resistor current  $I_{Ri}$ . The difference between  $V_A$  and  $V_B$  was amplified, and the differential output voltage  $V_O$  was used to control the conduction current  $I_O$  of the output transistor  $M_O$ . The larger the dc voltage  $V_{dc}$  is, the larger the conduction current  $I_O$  is. Thus, a stable DC output voltage ranged from 1.69 V to 1.76 V with an input power ( $P_{in}$ ) ranging from -14 dBm to +10 dBm. Please note that the voltage variations of two biased voltages,  $V_A$  and  $V_B$ , will be suppressed in the PVT (process, supply voltage, and temperature) variation. For example, if the resistor  $R_1$  is reduced with PVT variation, the bias current  $I_{R1}$  is enlarged. Then both conduction resistors,  $R_{ds1}$  and  $R_{ds2}$ , are decreased by the large bias current  $I_{R1}$ . As a result, three resistors,  $R_{ds1}$ ,  $R_{ds2}$  and  $R_1$ , are reduced simultaneously to suppress the impact of PVT variation.

#### 2.4. Low-Voltage Low-Dropout Regulator

Because of an input voltage with inference and input power limitation, a low-voltage and low-power LDO regulator is required for supplying a stable and clean voltage to the next stage. The designed LDO regulator was used for regulating the output variation in the over-voltage protection circuit and for providing a stable voltage  $V_{dd}$  of 1.5 V to the charger control circuit. Figure 5 shows the proposed low-voltage LDO regulator, which includes a reference voltage, a current source, an error amplifier, a pass transistor, a feedback network, frequency compensation, and a load. A CMOS reference voltage  $V_{ref}$  was generated and inputted to the positive terminal (+) of an error amplifier (EA). The negative terminal (-) of the EA was connected to the feedback network. A comparison between the reference voltage  $V_{ref}$  and a feedback value indicates that the voltage difference between the positive and negative terminals was amplified as an output voltage of the EA, which was connected to a pass transistor for providing a stable supply voltage  $V_{dd}$  by controlling the load current flow through the pass transistor [23].

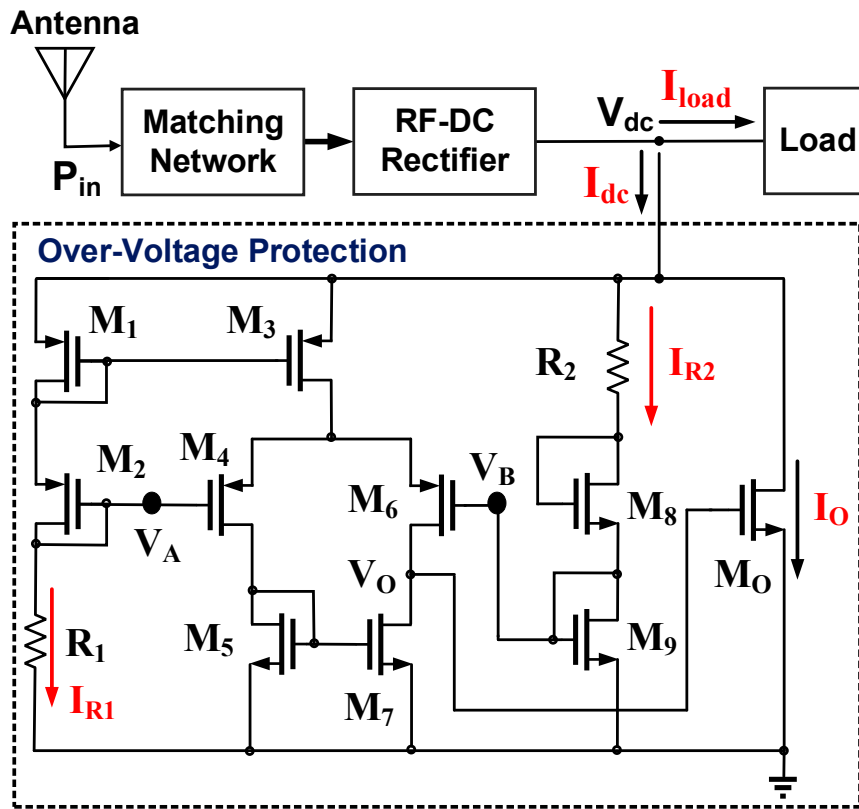


Figure 4. Proposed over-voltage protection circuit.

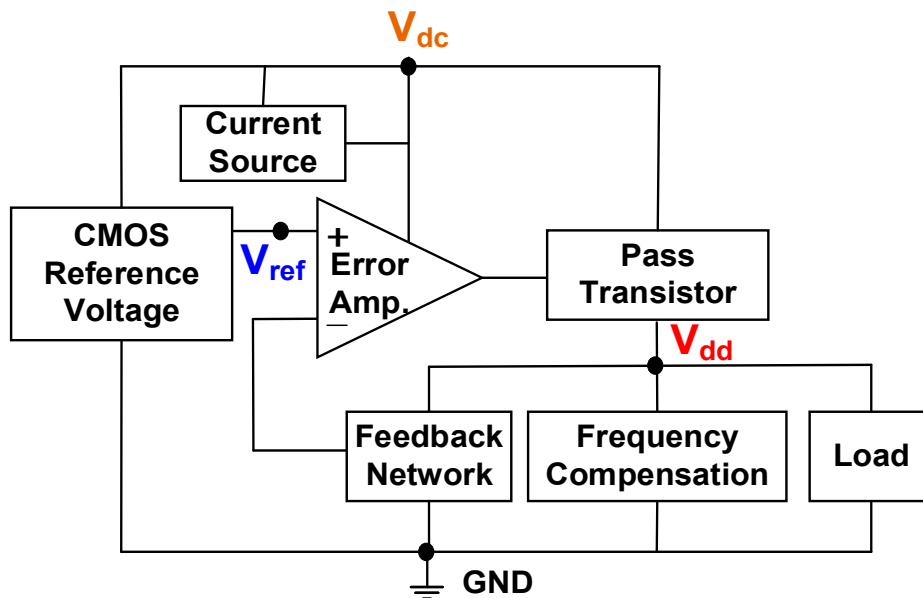


Figure 5. Proposed low-voltage LDO regulator with a reference voltage, a current source, an error amplifier, a pass transistor, a feedback network, frequency compensation, and a load.

Figure 6 shows the complete circuit of the adopted CMOS reference voltage [24]. The supplied voltage  $V_{dc}$  could be maintained at a possible voltage of 0.7 V when all transistors operated in the subthreshold region. A compensation capacitor  $C_C$  was added between the drain of  $M_{N1}$  and ground (GND) to improve circuit stability by increasing the phase margin. Assume that  $I_2 = 100 \times I_1$ ,  $W_{MP2} = 100 \times W_{MP1}$ , and  $W_{MN2} = 100 \times W_{MN1}$ . The voltage of node X was equal to that of node Y (i.e.,  $V_X = V_Y$ ).

Thus, the drain–source voltage of  $M_{P2}$  ( $V_{DS,MP2}$ ) was equal to that of  $M_{P3}$  ( $V_{DS,MP3}$ ). Two bias currents ( $I_2$  and  $I_3$ ) were identical without channel length modulations of  $M_{P2}$  and  $M_{P3}$ . If two NMOSFETs operated in the subthreshold region, the voltage difference across the resistor  $R_1$  is given as follows:

$$V_{R1} = V_{GS,MN2} - V_{GS,MN3} = nV_T \times \ln \frac{(W/L)_{MN3}}{(W/L)_{MN2}}, \quad (13)$$

where  $n$  and  $V_T$  are the subthreshold region swing parameter and thermal voltage, respectively. The  $n$  is a constant and  $V_T$  is a parameter independent of the process. Thus, process variations do not influence  $V_{R1}$ .  $V_{GS, MNi}$  and  $(W/L)_{MNi}$  are the gate–source voltage and the ratio of width to length for the transistor  $M_{Ni}$ , respectively. Equation (13) indicates that a temperature coefficient (TC) is positive for the resistor's voltage  $V_{R1}$ .

Voltage reference  $V_{ref}$  can be written as follows:

$$V_{ref} = V_{R2} + V_{GS,MN2} = 2.01 \times \frac{R_2}{R_1} \times V_{R1} + V_{GS,MN2}, \quad (14)$$

where  $V_{R1}$  and  $V_{R2}$  are voltage differences across resistors  $R_1$  and  $R_2$ , respectively, and  $V_{GS,MN2}$  is the gate–source voltage of the transistor  $M_{N2}$  with a negative TC. A positive TC was combined with a negative TC in an integrated circuit to obtain the desired reference voltage  $V_{ref}$  with zero temperature dependence [24]. The simulation result shows that the reference voltage  $V_{ref}$  varied from 499.035 mV to 502.855 mV with respect to the supplied voltage  $V_{dc}$  from 1.7 V to 2.0 V at a quiescent current of 34 nA.

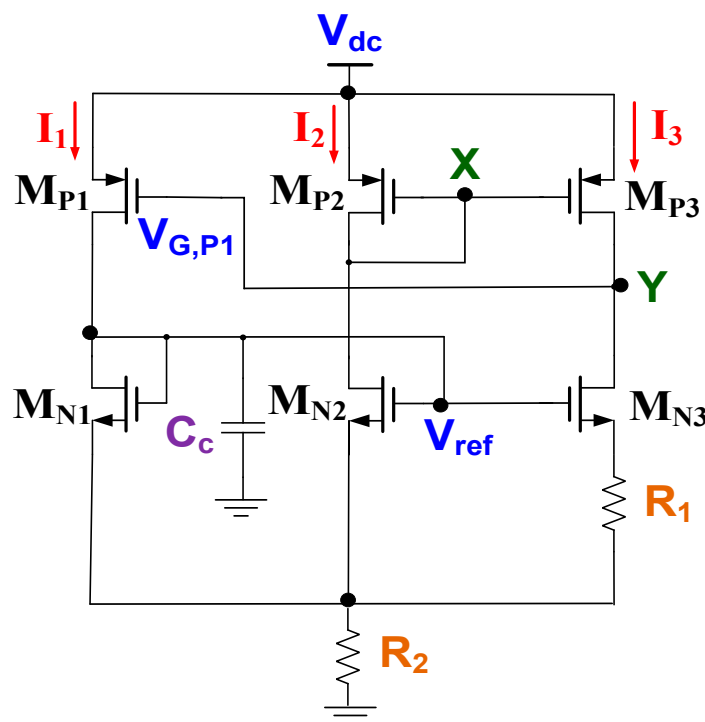


Figure 6. Complete circuit of the adopted CMOS reference voltage.

Figure 7 shows the complete circuit of a low-voltage LDO regulator. The EA was a CMOS two-stage amplifier, which was designed to regulate the supplied output voltage  $V_{dc}$  of the low-voltage LDO regulator by controlling the gate voltage of the pass transistor  $V_{err}$ . The first stage had a p-channel differential input pair with an n-channel current mirror active load for a high gain  $A_{V1}$ . The second stage is generally configured as a simple common source stage to allow maximum output swings with gain  $A_{V2}$  [25]. Bias currents were copied through the current source by controlling the resistor  $R_3$ .



The voltage swing at  $V_{err}$  was equal to  $V_{dc} - |V_{OD,MP6}| - V_{OD,MN6}$  with overdrive voltages,  $V_{OD,MP6}$  and  $V_{OD,MN6}$ , of MP6 and MN6, respectively. The overall voltage gain  $A_V$  can be derived as follows:

$$\begin{cases} A_{v1} = -g_{m,MP7} \left( r_{ds,MP8} \parallel r_{ds,MN5} \right) \\ A_{v2} = -g_{m,MN6} \left( r_{ds,MP6} \parallel r_{ds,MN6} \right) \\ A_v = A_{v1} \times A_{v2} \end{cases} \quad (15)$$

where  $g_{m,MPi}$  and  $r_{ds,MPi}$  are the transconductance and conduction resistance of the  $i^{\text{th}}$  PMOS, respectively.  $g_{m,MNi}$  and  $r_{ds,MNi}$  are the transconductance and conduction resistance of the  $i^{\text{th}}$  NMOS, respectively.

Zero frequency  $\omega_z$  can be modified by placing a resistor  $R_z$  in series with the compensation capacitor  $C_z$  [26]. If  $R_z \geq (g_{m,MN6})^{-1}$ , then  $\omega_z \leq 0$ . Zero may be moved into the left-half plane for cancelling the first nondominant pole  $\omega_{p2}$ . The compensation resistance  $R_z$  is then given as follows:

$$R_z = \frac{1}{g_{m,MN6}} \left( 1 + \frac{C_1 + C_2}{C_z} \right), \quad (16)$$

where  $C_1$  and  $C_2$  are total capacitances at node E before  $C_z$  was added and that at node  $V_{err}$ , respectively. Moreover, the increasing  $C_z$  moves the dominant pole to a lower frequency without affecting the second pole. This effect ensures that the designed amplifier is more stable [25]. The simulated results indicate that DC gain, phase margin, and unit-gain bandwidth were 50 dB,  $60^\circ$ , and 1.57 MHz, respectively, at a supplied voltage of 1.7 V and quiescent current of 223.22 nA.

The feedback network was a voltage-trimming network and comprised four diode-connected PMOSs ( $M_{P10}$ – $M_{P13}$ ) and an adjustable voltage,  $V_A$ , which is generally connected to a voltage of 1.4 V. Three PMOSs were designed to complete coarse adjustment, whereas the NMOS  $M_{P10}$  was used to perform fine-tuning by controlling the adjustable voltage  $V_A$ . To stabilize the LDO regulator, phase characteristics were adjusted such that a phase shift was less than  $180^\circ$  at gain crossover. Frequency compensation is completed by connecting a resistor  $R_F$  in series with a filter capacitor  $C_F$ . The loop gain was zero at  $s_z = -(R_F C_F)^{-1}$ .

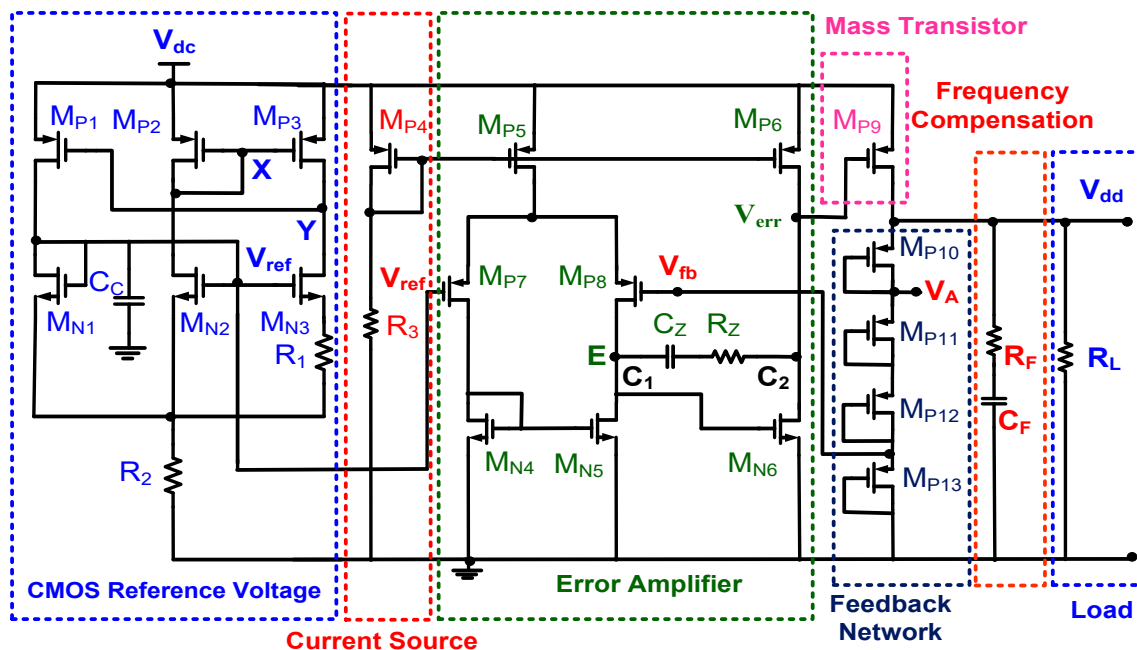


Figure 7. Complete circuit of the low-voltage LDO regulator.

### 2.5. Charge Control Circuit

Figure 8 presents the charge control circuit, which was used to control the charge in the battery by using the supplied output voltage  $V_{dd}$  of the LDO regulator. The control circuit comprised a differential pair ( $Q_1$ – $Q_3$ ), current mirror ( $Q_4$ – $Q_5$ ), and comparator (Comp) to prevent the overcharging of the battery. Channel length modulation and body effect were assumed negligible, and the differential pair operated in a saturation region. The battery was charged using a constant current, which was generated using  $Q_1$  and  $Q_2$  with two bias voltages ( $V_{B1}$  and  $V_{B2}$ ). When the battery voltage  $V_{bat}$  was lower than the reference voltage  $V_{ref}$ , the output voltage of the comparator increased to a high level (1) and  $Q_3$  was turned off. Two constant currents of  $Q_1$  and  $Q_4$  simultaneously flowed into  $Q_2$ . The conduction current of  $Q_5$  was amplified  $N$  times with  $(W/L)_5 = N \times (W/L)_4$  when it was passed through the current mirror  $Q_4$ – $Q_5$ . This large current rapidly charged the battery. If  $V_{bat}$  was higher than  $V_{ref}$ , the output voltage of the comparator was low (0) and  $Q_3$  was turned off. Two constant currents of  $Q_1$  and  $Q_3$  simultaneously flowed into  $Q_2$ . Moreover,  $Q_4$  and  $Q_5$  were turned off, and the battery was not further charged.

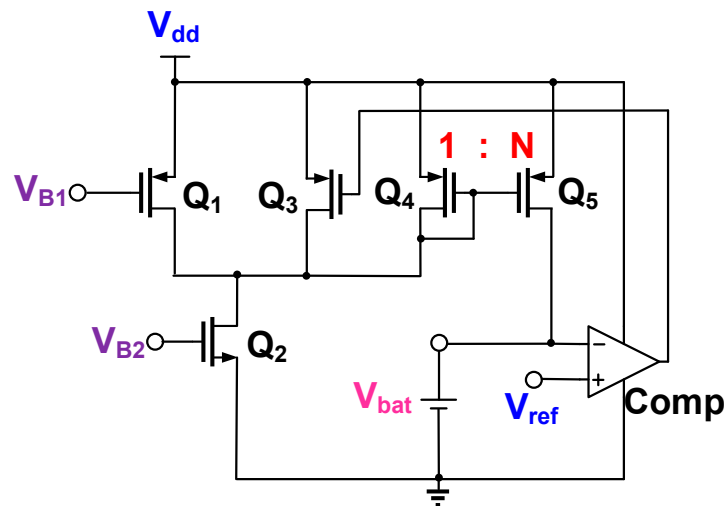


Figure 8. Complete circuit of charge control circuit.

### 3. Simulated and Measured Results

Figure 9 presents the simulated output voltage of the RF-DC rectifier by using a signal analyzer (EXA N9010A) at a distance of 10.0 cm between the antenna and rectifier. The operating frequency was 915 MHz, and the equivalent load was 1 M $\Omega$ . The simulation results revealed a minimum output voltage of 0.746 V at an input power  $P_{in}$  of  $-20$  dBm, and a maximum output voltage of 21.693 V at  $P_{in} = +20$  dBm. The proposed RF-energy-harvesting chip requires the over-voltage protection circuit to prevent the breakdown phenomenon, which is generated by high output voltages, particularly for NFC. Figure 10 shows the simulated DC output voltages of the RF-DC rectifier with over-voltage protection, which were limited from 1.773 V to 1.809 V with respect to the input power  $P_{in}$  from  $-13$  dBm to  $+20$  dBm. Figure 11 presents the simulated PCE of the RF-DC rectifier with over-voltage protection, which is termed the rectifier PCE. It was approximately 43.601% at an input power of  $-7$  dBm. PCE is defined as that in [26]:

$$PCE(\%) = \frac{P_{dc}}{P_{in}} \times 100\% = \frac{I_{dc} \times V_{dc}}{P_{in}} \times 100\% \quad (17)$$

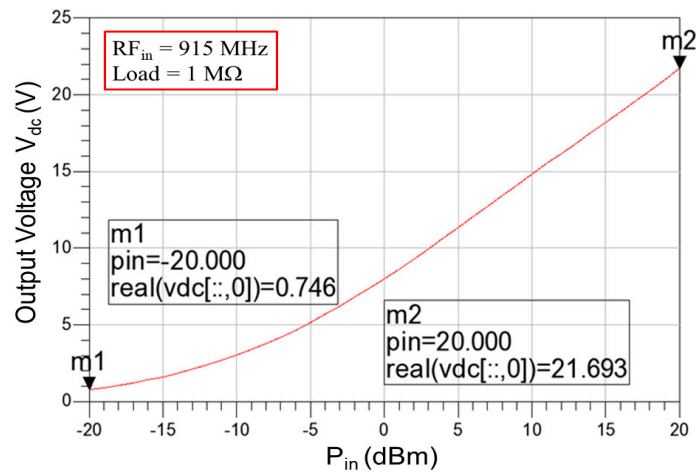


Figure 9. Simulated output voltage of the RF-DC rectifier with respect to the input power from  $-20$  dBm to  $+20$  dBm.

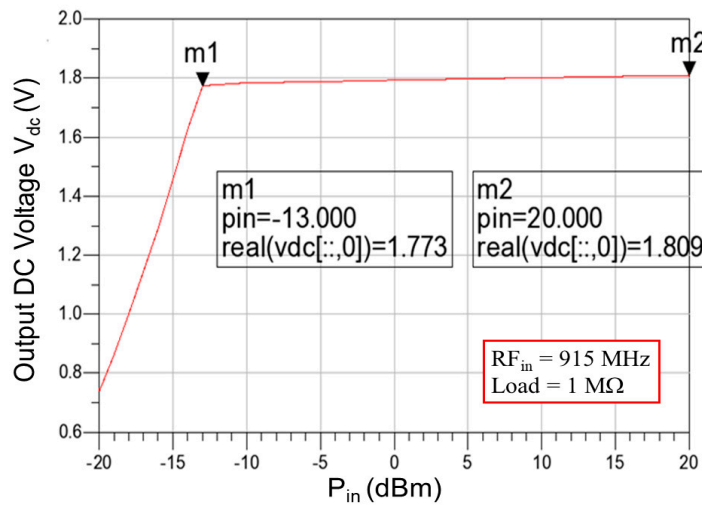


Figure 10. Simulated DC output voltages of the RF-DC rectifier with over-voltage protection.

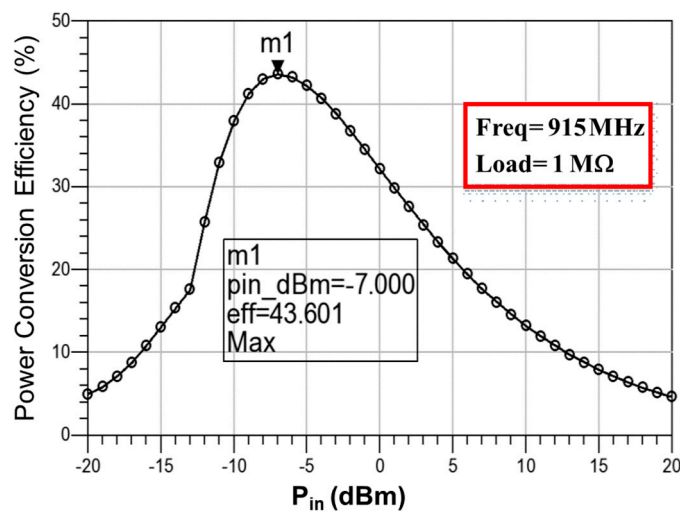


Figure 11. Simulated *PCE* of the RF-DC rectifier with over-voltage protection (rectifier *PCE*), whose *PCE* was approximately 43.6% at the input power of  $-7$  dBm.

The proposed LDO regulator provides a stable output voltage of 1.5 V and a load current of 30  $\mu\text{A}$  to the next stage-charge control circuit. When the input voltage varied from 1.7 V to 2.0 V and the reference voltage was 1.4 V, the LDO regulator performed with a quiescent current of 317 nA, and a maximum power efficiency of 84.835% was obtained at an input power  $P_{in}$  of  $-10$  dBm. Figure 12 shows the simulated line regulation of the proposed LDO regulator. When the input voltage was varied from 1.7 V to 2.0 V, the output voltage changed from 1.5 V to 1.5108 V, and a line regulation of 36 mV/V was obtained. Figure 13 presents the simulated load regulation of the proposed LDO regulator. As the output current varied from 0.0  $\mu\text{A}$  to 10.0  $\mu\text{A}$ , the output voltage changed from 1.499952 V to 1.499968 V. A load regulation of 1.6 mV/mA was then obtained [27].

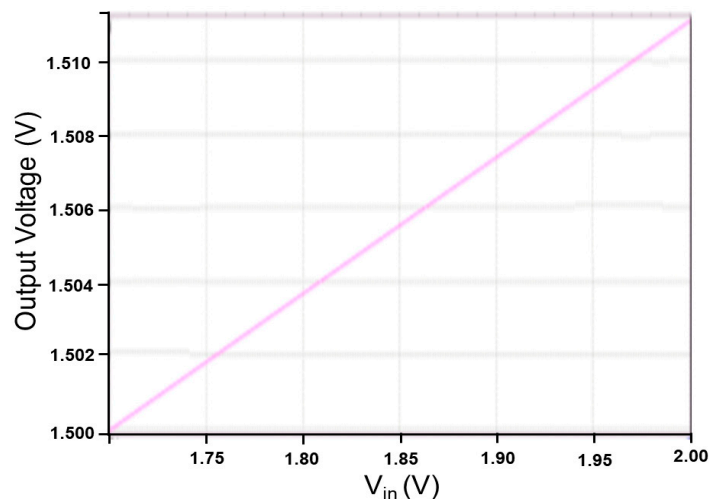


Figure 12. Simulated line regulation of the proposed LDO regulator.

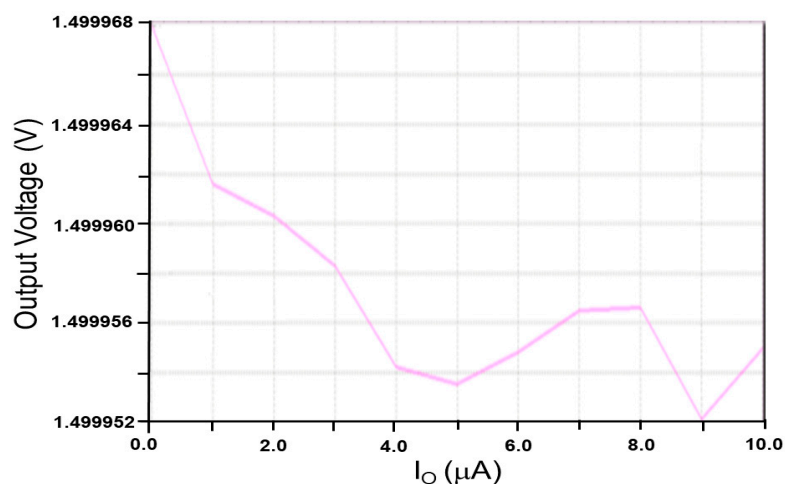


Figure 13. Simulated load regulation of the proposed LDO regulator.

The charge control circuit was inputted with a pulse waveform, which is gradually ramped up from 1.2 V to 1.5 V, to charge the battery with the charging current of 16  $\mu\text{A}$ . When the battery voltage was charged to 1.4 V at 2.002 ms, the charging current decreased sharply, thereby reducing the charging speed. Finally, the voltage of the battery increased to 1.50 V with zero charging current. Figure 14 shows the simulated battery voltage and charging current of the charger control circuit. The maximum power efficiency of the charge control circuit was 84.835% at an input power  $P_{in}$  of  $+20$  dBm.

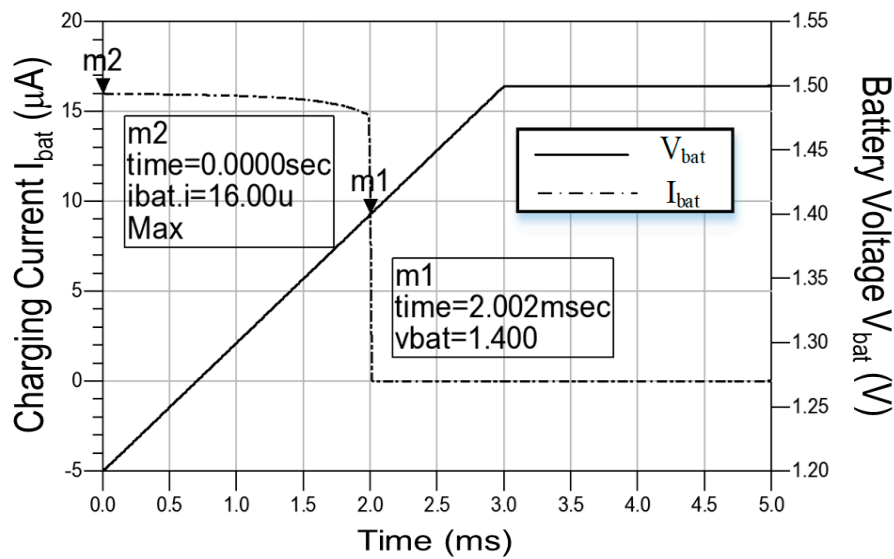


Figure 14. Simulated battery voltage and charging current of the charger control circuit.

When all functional blocks were verified, the RF-energy-harvesting chip could be implemented using the standard TSMC 0.18  $\mu\text{m}$  1P6M CMOS process. Figure 15 shows the layout of the proposed RF-energy-harvesting IC, which comprised the RF-DC rectifier, over-voltage protection circuit, CMOS voltage reference, LDO regulator, and charge control circuit. The over-voltage protection circuit, low-voltage LDO regulator, and charge control circuit of the RF-DC rectifier required 33  $\mu\text{W}$ , 5  $\mu\text{W}$ , and 4  $\mu\text{W}$ , respectively, to charge the battery to 24  $\mu\text{W}$ . The simulation results revealed that charging current was 16  $\mu\text{A}$  at  $N = 55$ , and the over-voltage protection mechanism was started at 2.002 by setting the output voltage of the over-voltage protection circuit, output voltage of the charger control circuit, and reference voltage at 1.7 V, 1.5 V, and 1.4 V, respectively. Figure 16 shows the simulated total power conversion efficiency of the proposed RF-energy-harvesting IC, which was termed the system PCE. The maximum system PCE was 29.873% at an input power  $P_{in}$  of  $-12$  dBm. The maximum rectifier PCE was reduced to the same value at  $P_{in} = -12$  dBm by integrating all designed circuits into a single chip (Figure 11). Table 1 summarizes the performance and compares it with that of other RF-DC rectifiers. The simulated maximum rectifier PCE in this study was superior to the PCEs of previously published RF-DC rectifiers. Table 2 presents the simulated specifications of the proposed RF-energy-harvesting IC.

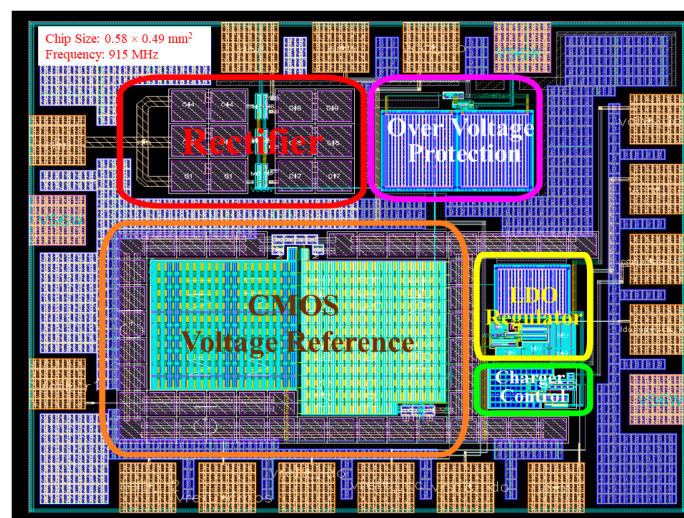


Figure 15. Layout of the proposed RF-energy-harvesting IC.

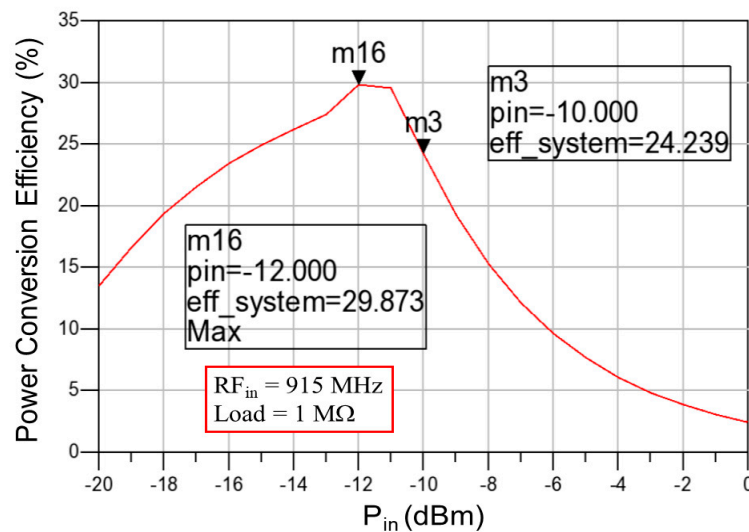


Figure 16. Simulated total PCE of the proposed RF-energy-harvesting IC.

Table 1. Summary of performance and its comparison with those of previous RF-DC rectifiers.

Reference (year)	[19] 2013	[28] (2014)	[29] (2017)	This Work
Process	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$	65 nm	0.18 $\mu\text{m}$
Input power	-7 dBm	-21.2 dBm	-17.7 dBm	-7 dBm
RF frequency	5.2 GHz	925 MHz	900 MHz	915 MHz
Rectifier stages	5	7	5	6
Matching circuit	On-chip	Off-chip	Off-chip	Off-chip
Maximum PCE	42%	43%	36.5%	43.6%

Table 2. Simulated specifications of the proposed RF-energy-harvesting IC.

Parameters	Designed Specifications
Technology process	TSMC 0.18 $\mu\text{m}$ 1P6M CMOS process
RF frequency ( $f_{in}$ )	915 MHz
Input power range ( $P_{in}$ )	-13 ~ +20 dBm
Output dc voltage ( $V_{dc}$ )	1.773 ~ 1.809 V
Maximum PCE of rectifier	43.603%
LDO output voltage ( $V_{dd}$ )	1.50 V
Charging current ( $I_{bat}$ )	16 $\mu\text{A}$
Maximum PCE of RF IC	29.873%
Chip area (include pads)	$0.58 \times 0.49 \text{ mm}^2$

The matching network was completed with off-chip components to have an input impedance of approximately  $50 \Omega$ . Figure 17 shows the matching network, which was designed to obtain not only maximum power transfer but also maximum conversion efficiency. The E5071C network analyzer was used to measure the input impedance against various input powers. Moreover, multiple sets of matching circuits were designed to ensure that each set of the matching circuit exhibited an input return loss ( $S_{11}$ ) of less than -25 dB. For example, an input impedance of  $51.464 - j \times 1.3071$  could be achieved with an input return loss ( $S_{11}$ ) of -34.271 dB by putting a parallel inductance (L) of 7.5 nH and a series capacitance (c) of 22 pF on a printed circuit board (PCB). Figure 18 shows the measured input return loss in the Z-smith chart at an input power and RF frequency of 0 dBm and 915.0000 MHz, respectively.

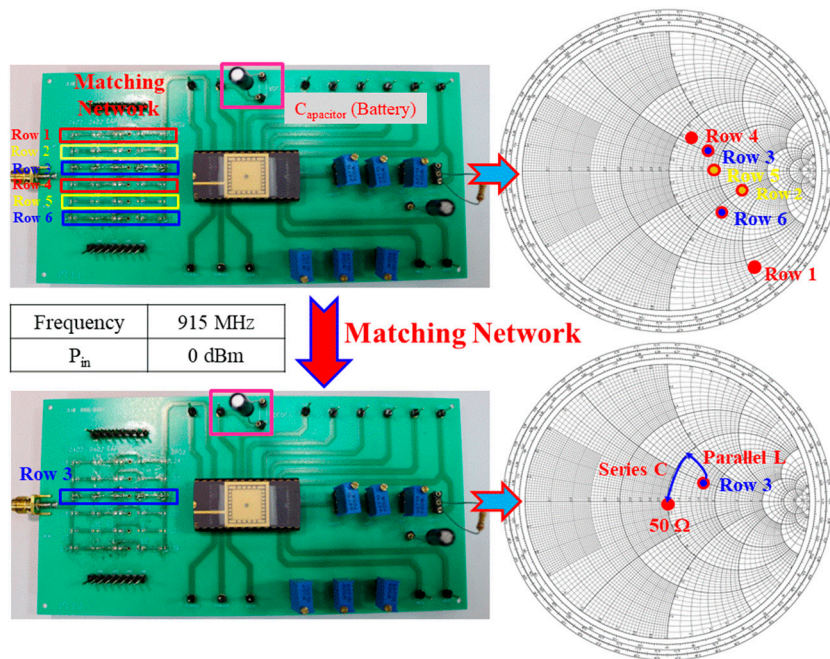


Figure 17. Matching network used to obtain an input impedance of approximately 50 Ω.

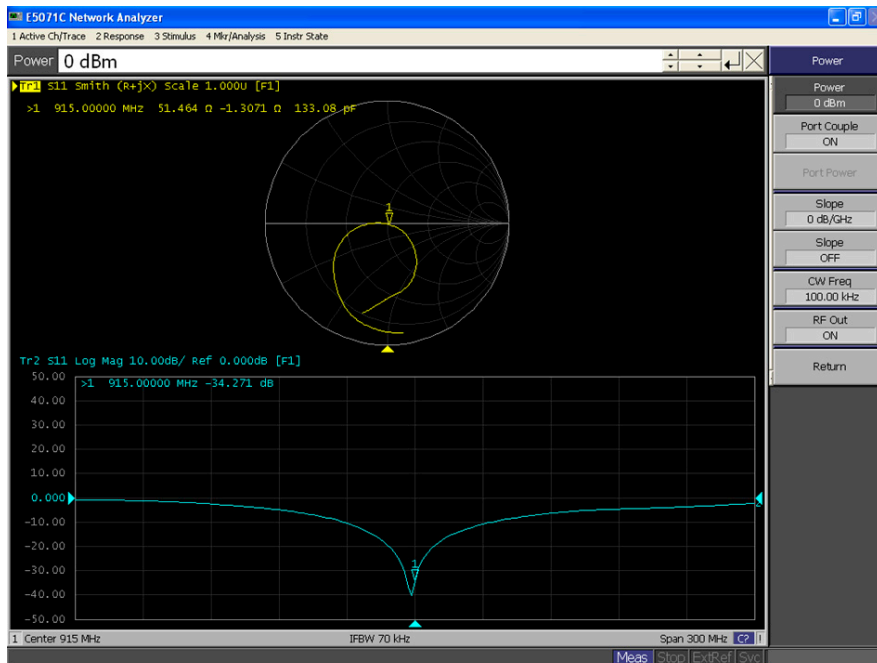


Figure 18. Measured results in the Z-smith chart at an input power of 0 dBm and RF of 915.0000 MHz.

Figure 19 shows the measurement platform of the designed RF-energy-harvesting IC with capacitor, which includes the PCB ( $15.576 \times 7.906 \text{ cm}^2$ ), network analyzer (Agilent E5071C), RF-IC ( $0.58 \times 0.49 \text{ mm}^2$ ), Powercast transmitter (TX91501), and multimeter (CNN 38). By connecting the receiving antenna to the matching network on the measured PCB, the multimeter measures the output voltage of approximately 1.702 V by setting a distance of 2.45 m between the Powercast transmitter and PCB, with an input power of 0.0 dBm. Figure 20 shows the measured setup of the proposed RF-energy-harvesting IC.

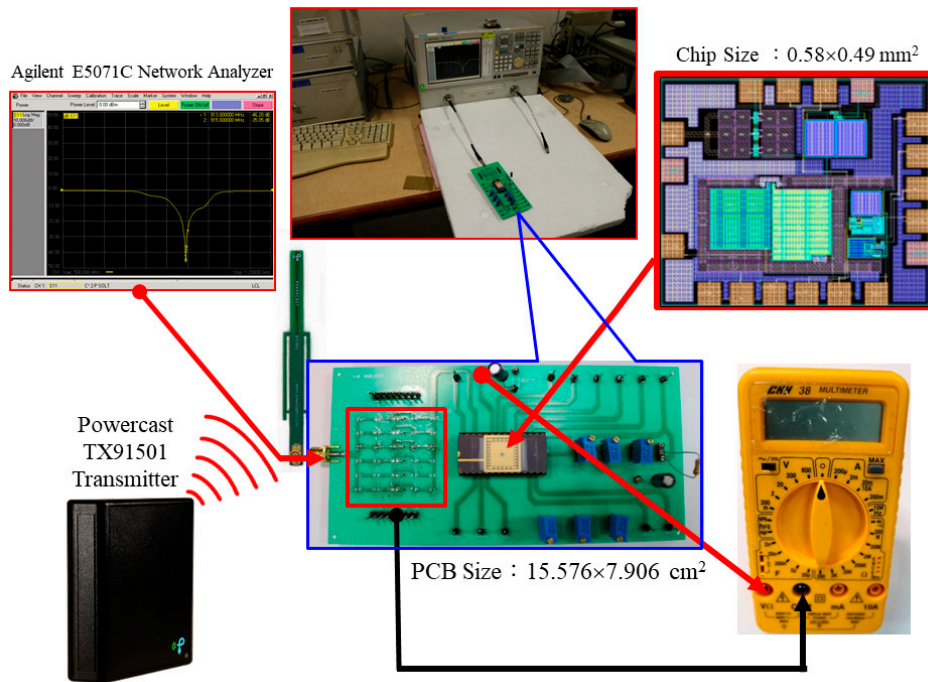


Figure 19. Measurement platform of the designed RF-energy-harvesting IC with capacitor.

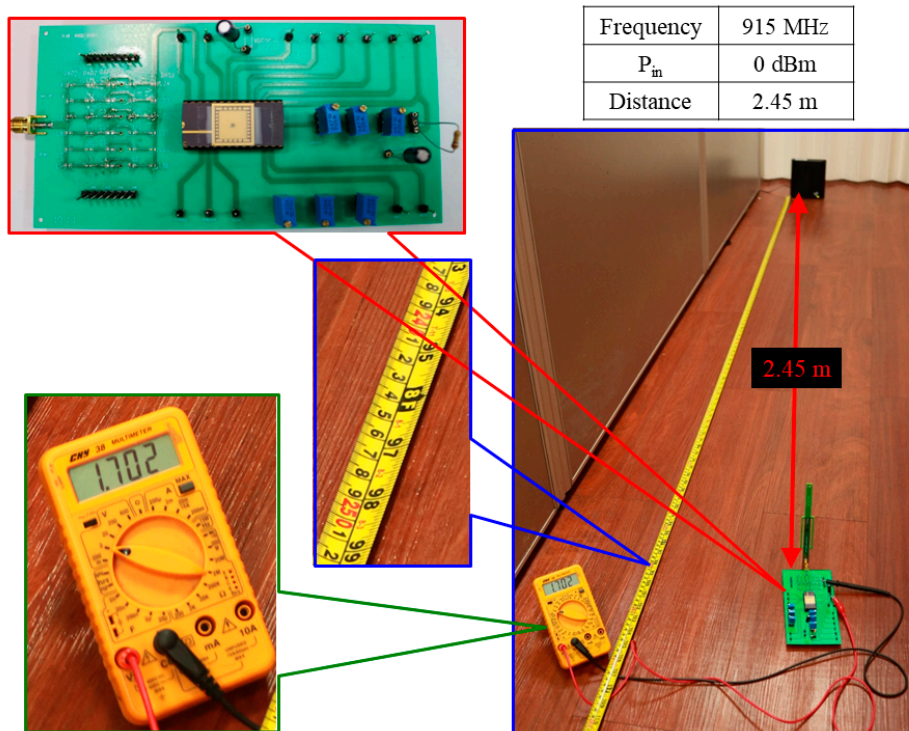


Figure 20. Measured setup of the proposed RF-energy-harvesting IC.

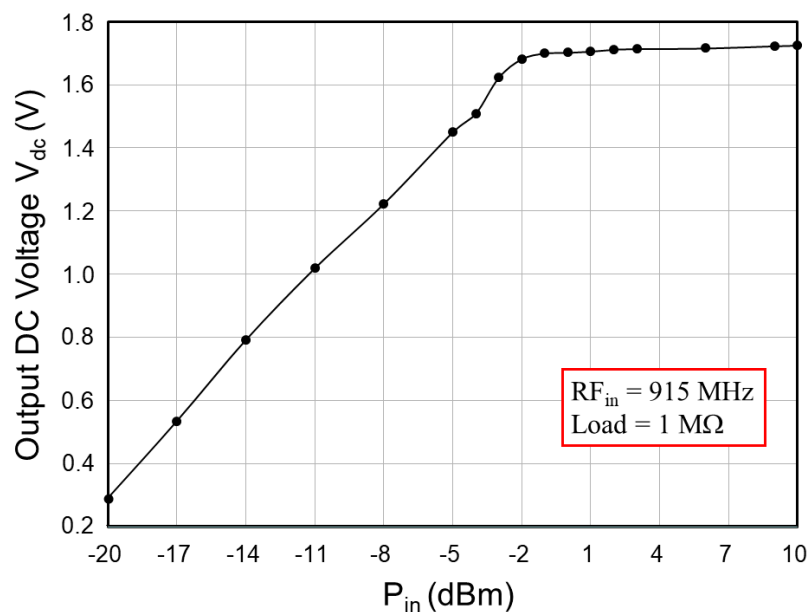
Table 3 summarizes the results for the designed RF-DC rectifier with the over-voltage protection circuit. Because the distance between the Powercast transmitter and test PCB was provided, the input power  $P_{in}$  (dBm), input return loss  $S_{11}$  (dB), and DC output voltage  $V_{dc}$  (V) were measured after the input impedance  $Z_{in}$  ( $\Omega$ ) and its corresponding matching circuits [L (nH) and C (pF)] were completed. The results showed that the DC output voltage  $V_{dc}$  varied from 0.291 V to 1.725 V with respect to the distance from 5.45 m to 0.55 m. The measured output voltages were lower than the simulated



results. A stable charging voltage  $V_{dd}$  can be obtained through the LDO regulator. Figure 21 shows the measured DC output voltage  $V_{dc}$  of the designed RF-DC rectifier with the over-voltage protection circuit with respect to the input power  $P_{in}$  from  $-20$  dBm to  $+10$  dBm. Please note that the measured DC output voltages were limited from  $1.682$  V to  $1.725$  V with respect to the input power from  $-2$  dBm to  $+10$  dBm in Figure 21.

**Table 3.** Measured input power  $P_{in}$  (dBm), input return loss  $S_{11}$  (dB), and output DC voltage  $V_{dc}$  (V) with respect to distance (m) between the transmitter and test PCB, input impedance  $Z_{in}$  ( $\Omega$ ) and its corresponding matching circuits [L (nH) and C (pF)] for the RF-DC rectifier with the over-voltage protection circuit.

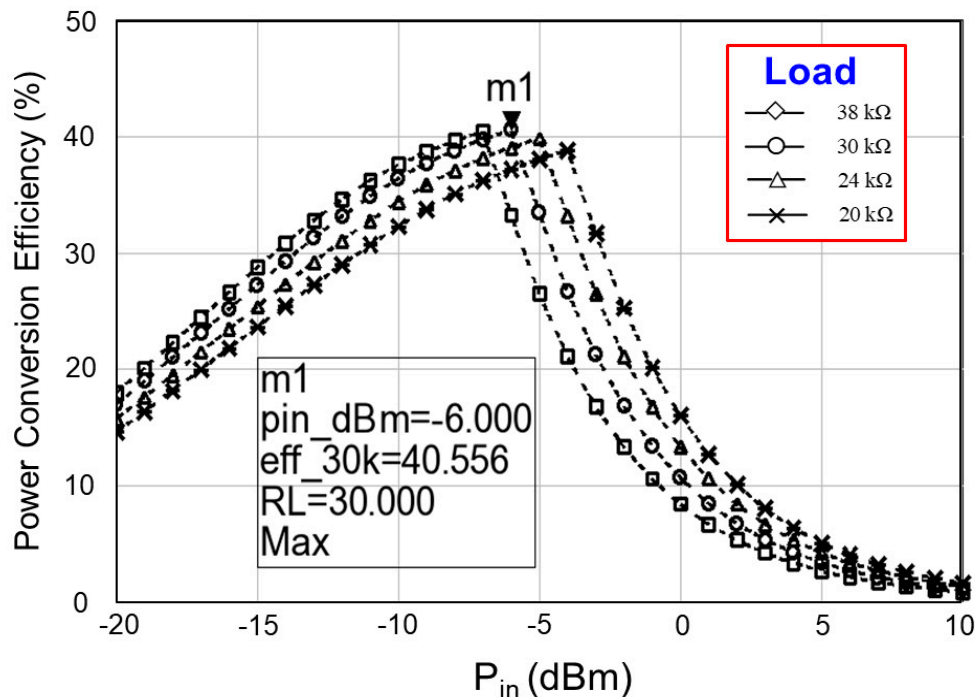
Distance (m)	$Z_{in}$ ( $\Omega$ )	Matching Circuits		$P_{in}$ (dBm)	$S_{11}$ (dB)	$V_{dc}$ (V)
		Parallel (L)	Series (C)			
5.45	$50.548 - j \times 2.294$	2.4 nH	38 pF	-20	-28.1	0.291
5.12	$52.043 - j \times 2.893$	3.6 nH	32 pF	-17	-28.4	0.535
4.66	$53.916 - j \times 1.260$	6.8 nH	29 pF	-14	-32.6	0.792
4.25	$51.784 - j \times 2.789$	8.6 nH	26 pF	-11	-29.8	1.019
3.93	$52.784 - j \times 2.699$	6.6 nH	24 pF	-8	-28.4	1.223
3.60	$48.561 - j \times 6.422$	5.6 nH	22 pF	-5	-33.0	1.450
3.30	$52.109 + j \times 3.382$	5.6 nH	22 pF	-4	-28.3	1.509
3.15	$53.942 - j \times 1.324$	6.2 nH	22 pF	-3	-28.0	1.623
2.90	$54.226 + j \times 2.072$	6.2 nH	22 pF	-2	-26.9	1.682
2.70	$53.369 - j \times 11.324$	6.8 nH	22 pF	-1	-29.0	1.700
2.45	$51.464 - j \times 1.307$	7.5 nH	22 pF	0	-34.3	1.702
2.25	$51.581 + j \times 7.158$	10 nH	10 pF	1	-35.4	1.706
1.68	$49.710 - j \times 4.909$	10 nH	10 pF	2	-26.1	1.712
1.50	$53.573 + j \times 1.835$	12 nH	10 pF	3	-28.2	1.714
1.00	$54.669 - j \times 1.756$	22 nH	10 pF	6	-26.4	1.716
0.68	$53.350 - j \times 2.136$	68 nH	10 pF	9	-28.3	1.723
0.55	$50.655 - j \times 4.093$	100 nH	10 pF	10	-27.7	1.725



**Figure 21.** Measured DC output voltages of the RF-DC rectifier with over-voltage protection with respect to the input power.

Finally, the simulated rectifier  $PCE$  was 43.601% at an input power  $P_{in}$  of  $-7$  dBm, and the simulated system  $PCE$  was 29.873% at an input power  $P_{in}$  and a load resistor of  $-12$  dBm and  $1$  M $\Omega$ ,

respectively. The limitation of system integration is the reduction of the  $PCE$  from 43.601% to 29.873%. The improvement of the system  $PCE$  is a crucial concern. This study focused on increasing the system  $PCE$  by changing the load resistor from 20 k $\Omega$  to 38 k $\Omega$ . Figure 22 exhibits the measured system  $PCE$  with respect to the input power  $P_{in}$  (dBm) and load resistor. The larger the load resistor is, the smaller the input power is. A large load resistor reduces load current, whereas it increases charging current  $I_{bat}$  for the abrupt charging of the battery. This phenomenon provides the maximum system  $PCE$  at a low input power. A trade-off was observed between the load resistor and the maximum system  $PCE$ . Moreover, the results indicate that the largest system  $PCE$  of 40.556% was observed at a load resistor of 30 k $\Omega$  and an input power  $P_{in}$  of  $-6$  dBm.



**Figure 22.** Measured  $PCE$  of the proposed RF-energy-harvesting IC (system  $PCE$ ) with respect to the input power (dBm) and load resistor ( $\Omega$ ).

Table 4 shows the measured electrical characterizations of the proposed RF-energy-harvesting IC, which includes the power consumption, power delivery, and other electrical characterization facts. Table 5 summarizes the performance and compares the performance with that of other RF-DC rectifiers and RF-energy-harvesting ICs. The maximum rectifier  $PCE$  obtained in this study was superior to that in [30], and the maximum  $PCE$  of the RF-energy-harvesting IC was superior to that in [31]. Several RF-DC rectifiers have been studied in the past few years; however, studies on system integration, such as RF-energy-harvesting ICs, have been rare. Furthermore, the IC proposed in this study exhibited low power consumption and a small chip area. It is possible to decrease the labor cost significantly by eliminating the future maintenance efforts to replace batteries. At close range, this proposed IC can be used to trickle charge for low power devices including GPS, tracking tags, wearable sensors, and consumer electronics. At long range, this transmitted power can be used for battery-based or battery-free remote sensors for factory automation, structural health monitoring, and industrial control. In future work, the power conversion efficiencies ( $PCEs$ ) of the rectifier and RF-energy harvesting chip can be improved by reducing the energy consumption of each proposed circuit.

**Table 4.** Measured electrical characterizations of the proposed RF-energy-harvesting IC.

Parameters (unit)	Values
RF frequency (MHz)	915
Input impedance ( $\Omega$ )	$51.464 - j \times 1.3071$
Input power (dBm)	0
Distance between Powercastand PCB (m)	2.45
Matching components	$L = 7.5 \text{ nH}$ and $C = 22 \text{ pF}$
Load resistor ( $k\Omega$ )	30
Measured PCB ( $\text{cm}^2$ )	$15.576 \times 7.906$
Maximum <i>PCE</i>	$40.566\% @ P_{in} = -6 \text{ dBm}$
Output voltage (V)	1.50
Power consumption ( $\mu\text{W}$ )	42
Chip area ( $\text{mm}^2$ )	$0.58 \times 0.49$

**Table 5.** Summary of performance and its comparison with those of other RF-DC rectifiers and RF-energy-harvesting ICs.

Reference (year)	[30] (2018)	[31] (2018)	[32] (2016)	[33] (2017)	This Work
Process ( $\mu\text{m}$ )	0.13	0.18	0.18	0.13	0.18
RF frequency (MHz)	915	900	900	2000	915
Matching circuits	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip
Input power range (dBm)	$-35 \sim -15$	$-30 \sim +0$	$-26 \sim -8$	$-35 \sim +5$	$-20 \sim +10$
Stages (Rectifier)	10	5	2	3	6
Maximum <i>PCE</i> (Rectifier)	$42.8\% @ P_{in} = -16 \text{ dBm}$	—	$78.2\% @ P_{in} = -12 \text{ dBm}$	$73.9\% @ P_{in} = 4.34 \text{ dBm}$	$43.6\% @ P_{in} = -7 \text{ dBm}$
Output voltage (V) (Rectifier)	2.32	—	1.0	3.5	1.725
Maximum <i>PCE</i> (RF harvesting IC)	—	$32.8\% @ P_{in} = -2 \text{ dBm}$	—	—	$40.56\% @ P_{in} = -6 \text{ dBm}$
Output voltage (V) (RF harvesting IC)	—	1.77	—	—	1.50
Load resistor ( $k\Omega$ )	500	500	—	2	30
Chip area ( $\text{mm}^2$ )	0.0296	16.56	—	0.954	0.2842
Power ( $\mu\text{W}$ )	—	—	—	—	42

#### 4. Conclusions

This study proposed an auxiliary power integrated chip (IC) to supply power to the WSN with a Power cast transmitter of ISM 915 MHz. The RF-energy-harvesting IC was designed and fabricated using the standard TSMC 0.18  $\mu\text{m}$  1P6M CMOS process. The externally matched capacitors and inductors were manufactured in the matching network by MuRata Company. On integrating the externally matched components with the designed RF-energy-harvesting IC, the simulated results showed that the maximum *PCEs* of the rectifier and harvesting IC were 43.6% and 29.873%, respectively, at an ISM band of 915 MHz, an input power of  $-7 \text{ dBm}$ , and a load of  $1 \text{ M}\Omega$ . The output voltage of the RF-DC rectifier with the over-voltage protection circuit was limited from 1.773 V to 1.809 V with the varying input power from  $-10 \text{ dBm}$  to  $+20 \text{ dBm}$ . A stable voltage of 1.5 V was supplied to the charge control circuit passing through the LDO circuit. Measurements validated that the designed RF-energy-harvesting IC works successfully. The output voltage  $V_{dc}$  varied from 0.291 V to 1.725 V with respect to the distance from 5.45 m to 0.55 m. The large load resistor reduced load current; however, it sharply increased the charging current to charge the battery abruptly. This phenomenon provided the maximum system *PCE* at low input power. A trade-off was observed between the load resistor and the maximum system *PCE*. Furthermore, the maximum rectifier *PCE* of this study was superior to that in [30], and the maximum *PCE* of the RF-energy-harvesting IC was superior to that in [31]. Measurements indicate that the IC used in this study exhibited low power consumption and a small chip area. The proposed energy harvesting IC can be used in both ambient source and dedicated

source [34]. Another possibility offered by the use of microelectronic substrates is on-chip photovoltaic generation with integrated photodiodes [35,36].

**Author Contributions:** This study was completed by four authors. Y.-J.L. and J.-Y.S. designed and implemented the proposed chip; C.-K.C. completed the system integration and measurements; and G.-M.S. analyzed the data and wrote the paper.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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