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Metrology for the next generation of semiconductor devices

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Abstract

The semiconductor industry continues to produce ever smaller devices that are ever more complex in shape and contain ever more types of materials. The ultimate sizes and functionality of these new devices will be affected by fundamental and engineering limits such as heat dissipation, carrier mobility and fault tolerance thresholds. At present, it is unclear which are the best measurement methods needed to evaluate the nanometre-scale features of such devices and how the fundamental limits will affect the required metrology. Here, we review state-of-the-art dimensional metrology methods for integrated circuits, considering the advantages, limitations and potential improvements of the various approaches. We describe how integrated circuit device design and industry requirements will affect lithography options and consequently metrology requirements. We also discuss potentially powerful emerging technologies and highlight measurement problems that at present have no obvious solution.

Keywords

nanometrology; AFM; SEM; CD-SAX; TEM; Scatterometry

For over 50 years Moore's law has been associated with dramatic decreases in the size (scaling) of components used to fabricate integrated circuits (IC). Scaling has resulted in faster computers and the miniaturization of a wide range of electronics products, but in the next 15 years scaling is expected to either reach its functional limits or a point where cost and reliability issues outweigh the benefits[1-3]. Within those 15 years, the industry is

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projected to introduce the smallest and most complex devices yet[4]. For example, by 2024 the gate length of ICs is projected to be 6 nm, and instead of being planar in orientation, the gate will wrap around vertically configured nanowires. The benefits of these devices – including improved current flow and control, low power consumption, and faster switching – are clear[5] and manufacturing methods are being optimized. What is less obvious are the measurement methods needed to adequately characterize their nanoscale dimensions.

As devices shrink in size, and become more three-dimensional (3D) in shape, the relative importance of metrology increases. For example, for some products, more than 50% of the manufacturing steps can involve measurement or characterisation. We are also now approaching the point where each atom's position and type within a 3D device needs to be known. And this is in an environment where billions of these devices are required in each chip, and all of them must work to a tight specification. Metrology's role in IC manufacturing includes exploratory research, technology development, and process control[6]. Understanding the metrology needs[5,7] of a device requires knowledge of key design parameters, including their patterning options[8] and measurement requirements, as well as available measurement solutions, their capabilities and limits.

In this Review Article, we examine current and proposed device structures, and their key metrology requirements. We describe some of the main instruments used, and consider their capabilities, limitations, and potential improvements. We also outline some potentially disruptive techniques/trends for metrology and identify measurement problems with no obvious solutions. Although the measurands (what is being measured) described below are specific to the IC industry, due to the nanoscale size and complexity involved, methods developed for IC metrology often represent fundamental new capabilities that are later used in other areas.

Integrated circuit device structures

Integrated circuit scaling has been made possible by concurrently reducing device geometrical dimensions, increasing drive current, and reducing voltage. This is increasingly difficult to do because of the rising importance of parasitics (for example, coupling capacitance due to feature proximity) and higher manufacturing costs[9]. In addition to geometrical scaling, new device structures and designs that allow better drive current scaling[10-12], better connections to the device and better interconnect are needed[13,14]. The 2017 International Roadmap for Devices and Systems (IRDS)[15] addresses the mainstream device structures that will drive technology development in the next 15 years (Fig. 1a,b).

The fin-based field-effect transistor (FinFET)[15] will remain the mainstream device option until 2021 when gate all around (GAA) devices would need to be introduced to provide enhanced performance at smaller dimensions due to better electrostatics control[9,16]. Lateral GAA (LGAA), which is closer to FinFETs in structure, would be implemented first, followed by vertical GAA (VGAA). It is also projected that from 2021 onwards, 3D assembly integration schemes will support heterogeneous integration as well as memory-on-logic co-integration. Scaling is projected to stall in 2027 (Fig. 1b) because of process and electrical limits. These limits include but are not limited to: worsening resistance and time-

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dependent-dielectric-breakdown in the metals[17]; worsening coupling capacitance between gate and drain[9]; worsening short-channel behaviour due to gate length[16]; and mobility degradation by reduced device width and mechanical stability of fins and GAA devices[11].

In addition to these eventual limitations, the advances in chip design create major challenges for future semiconductor patterning, and addressing these with new techniques has created new metrology challenges. Patterning challenges arise largely because lithography resolution is continually getting smaller (see select device parameters in Fig. 1b). Also, printed features are small enough that random variations (stochastic effects) in the amount and position of molecules can now create small variations in pattern fidelity that have substantial effects on device performance[18]. As such, controlling roughness[19-24] (or more generally, feature uniformity[25]) is critical. Also, these stochastic effects[26] are large enough relative to the smaller device dimensions that missing patterns or random open and short defects must be thoroughly inspected for.

Furthermore, the trend towards structures that are smaller and more complex in all directions introduces new dimensional parameters to be controlled and changes how old ones are measured. For example, going from a planar FET device to a FinFET device meant that not only does roughness in the width of the gate feature affect performance, but also roughness in the width of the fin. With GAA structures, both the device size and the roughness affect performance and have to be measured[4]. Also, going from a lateral GAA to a vertical GAA means that the gate is now a film thickness instead of being estimated by linewidth measurement, thereby requiring different analysis techniques. The advent of 3D stacking, and 3D very large-scale integration (3DVLSI)[14,27,28] will add many steps to IC production process, and since these are fully functional tiers, destructive characterization would be prohibitively expensive. This will put a premium on high yield and low defects for each process step. How to do this in a practical and economically viable way is still an open question.

Beyond VGAA, several emerging device candidates have been proposed as replacements for complementary metal-oxide-semiconductor (CMOS) devices. These include transistors that incorporate new materials, such as graphene, carbon nanotube (CNT), and transition metal chalcogenides (for example, molybdenum disulphide (MoS_2)) (Fig 1c, d)[29,30]. Although most of the dimensional parameters are not yet defined, methods that are applicable to 2D materials-based structures are highlighted throughout the review. While structure of most proposed beyond CMOS structures are not necessarily more complex than those of VGAA structures, this might change as specific technologies advance. Currently, for dimensional parameters, VGAA structures and stacked chips (3DVLSI)[31] are some of the most complex structures available.

In addition, new computing approaches such as neuromorphic computing are driving IC design and will have challenges for 3D and materials metrology[32]. Neuromorphic chips aim to mimic the way the brain (or biological systems in general) solves problems. Here, the computing components (neurons) and memory (synapses) are connected in a neural network and can continually change and optimize their response to inputs. An example of this type of chip uses the memristor[33-35], which combine both resistive and memory components, and

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could be implemented in a broad range of materials[32,34,36,37] using crossbar designs (Fig. 1e). Figure 1f shows a cross-sectional scanning electron microscopy (SEM) image of a 3D stacked cross-bar Si nanowire array memristor implementation[38]. Figure 1g shows 8 × 8 nm^2 memristors in a crossbar array[25,32]. Implementations with densities as large as 4.5 $Tbit/in^2$ (with crossbar of around 2 nm by 2 nm) have also been proposed[39]. Neuromorphic chips could be integrated into 3DVLSI stacks such as the resistive random-access memory (RRAM) shown in Fig. 1aiv.

Whatever the eventual dimensions for beyond CMOS structures, basic measurement questions still hold: what is the measurand, what is the measurement model (instrument, sample, measurement physics, etc.) and when is it valid, how small a feature can one measure with good repeatability, and what are the error sources?

Metrology challenges for complex IC device structures

The most difficult metrology challenges involve device structure (shape and layout) complexity, new materials, and the statistical limits of controlling sub-5 nm stochastic processes for dimensional, compositional, surface, and interfacial measurements where a less than 10 % deviation from nominal size could affect device performance[6].

Measurements at near atomic scale dimensions are sometimes limited by physical property changes due to decreasing size (quantum confinement, typically starting at <10 nm). An instrument's inherent capability could be restricted by the physical inaccessibility of the measurand, presence of other materials, the positioning system needed to obtain the required data, and noise. For example, VGAA's orientation results in non-uniform instrument sensitivities at different depths, and smaller confined target volumes, making them harder to measure than LGAA.

Nanoscale roughness (surface, line edge, etc.) is proving challenging to evaluate. This is partly because roughness values are not intrinsic parameters of a surface. For example, two surfaces (or line edges) could have the same roughness value, but differ in texture, frequency components, and impact on function. Two surfaces could also have the same apparent final texture, but the underlying frequency components were produced at different stages with differing impacts on subsequent processes. Furthermore, although roughness could add to measurement noise, instrument noise (not due to roughness) can also be mistaken for feature roughness, requiring unbiased analysis techniques. Recent work aims to identify evaluation methods based on roughness origin and impact[23,24,40], and instrumentation and procedures[19,24,41].

High aspect ratio structures or devices with multiple layers such as 3DVLSI or 3D stacked Si memristor crossbars (Fig. 1f) would be particularly challenging due to the required depth of focus, presence of low-contrast materials, and possibility of beam damage, among others. The signal to noise ratio (SNR) of localized information (such as single particle defects) and film thickness from deep and multi-layered structures (including GAA) could be quite low due to the increased depth. With the advent of new lithography techniques (such as multi-patterning), smaller features sizes, number of masks per wafer layer, and increased density,

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overlay is more important than ever, and will be critical for stacked chips. The overall measurement process (instruments, sampling, data analysis, metrologist, etc.) needs to include an understanding of the nanoscale materials' properties[42], possible sources of error, and of the physics of the measurement.

Integrated circuit metrology challenges include but are not limited to measurement of surface and interfacial properties, thickness variation, line edge/width roughness (LER and LWR), defects for stacked nanowire, and complex material stacks (layers)[7,43-45]. Other challenges include measurement of strain[46], defect density, composition, and material dielectric interfaces for 2D and 3D materials. More broadly, most of the challenges involve measurement of dimensional, compositional, and interconnect parameters for 3D structures such as GAA nanowire, and 3DVLSI[47] where each technology level could have different metrology needs. Select dimensional parameters and requirements from the 2017 IRDS metrology roadmap[4] include VGAA nanowire diameter (6 nm), half pitch (7 nm), nanowire roughness and uniformity (0.3 nm) for the years 2030 to 2033; gate length (14 nm) and surface roughness (0.12 nm) for the years 2027 to 2033.

Advanced metrology techniques

Measurements are needed in all aspects of IC research and development, integration, manufacturing process control, and test. This requires instruments with a wide range of underlying physics[6,48] including light, electron, X-ray, and surface forces, among others, and that span over several orders of magnitude in sensitivity. The parameters being measured include critical dimensions (size and shape), film thickness, surface and interface properties, physical properties, defects, and associated parameters that help illustrate structure-function relationships. The methods described below (and related implementations) are used to address most of the dimensional metrology needs outlined in the previous section. They are by no means the only instruments used, but these with their applications are key to all aspects of IC fabrication. Table 1 shows comparison of key metrological quantities for the instruments described below.

Scanning electron microscopy (SEM).

This is one of the most versatile techniques used for in-line IC measurements, uses a finely focused electron beam to scan over the sample. The beam/sample interaction produces secondary and backscattered electrons (and other signals) which are acquired by detectors, to determine feature shape and size (and composition) with sub-nanometre scale resolution[49].

Specialized critical dimension SEMs (CD-SEMs) are optimized for IC manufacturing, and due to their stringent design requirements, have for the last few decades been central to some key improvements in SEMs[49]. Enhancements such as low-electron landing energy (typically 300 eV to 800 eV), high-efficiency through-lens secondary electron detectors, and fast and accurate sample-stages, tailored for repeatable, non-destructive high-speed imaging and measurements of features on semiconductor wafers have made CD-SEMs one of the indispensable instruments of IC production.

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CD-SEMs provide top-down images yielding critical IC dimensional parameters such as linewidth (see Fig. 2ai), edge roughness[50], and contact holes[47], and could produce 3D information (Fig. 2aii) if the beam is tilted[49,51,52] CD-SEMs are capable of measuring 7 nm feature size FinFET and nanowire devices[47], but could be extended to features of sub-5 nm if measurements are coupled with simulation and modelling to optimize measurements and results interpretation (Fig. 2a,b,c)[49,53]. SEMs are also used with other techniques[47,5354] (see hybrid metrology below) to obtain information on parts of a feature that cannot be measured directly. SEM is used for overlay measurements, and high voltage SEM has been proposed as a viable candidate for overlay of buried layers[47,55]; and contour metrology, where the required information are planar two-dimensional profiles used to verify optical proximity correction [56,57]

The top performance of modern SEMs is not limited by the focusing ability of their electron-optical columns[58], but rather by error sources such as drift, vibration, beam damage, charging and contamination. CD-SEM measurements can be made traceable to the SI (Systeme International d'Unites or International System of Units) definition of length using calibrated samples, or displacement interferometry, which can also be used to monitor and compensate for sample-stage motions. Although traceability is not always emphasized in IC metrology, structures such as proposed memristor crossbars[39] with an active area of around 2 nm by 2 nm, would require accurate measurement techniques since their sizes determine available space for computing functions, and overall packing density.

New results from Monte Carlo secondary electron simulations interpolated with measurements from a single image show agreements of less than 1 nm with other techniques[52,53]. Figure 2aiii shows overlaid SEM and transmission electron microscopy (TEM) profiles with a difference of less than 1 nm. Here, the size and shape parameters for libraries of predicted yield vs positions for different feature geometries are adjusted until library values best match the measured image. Such models require a thorough understanding and application of the physics of signal generation and detection, sample properties, error sources, and can be used to optimize measuring conditions and instruments settings (Fig. 2b,c).

New fast imaging[58-61] with sparse and optimized beam-scanning schemes has been developed to acquire only the needed information. Deep learning algorithms for denoising SEM images can bring unprecedented improvement both in speed and in imaging performance. A recent example denoises low dose SEM images by removing the additive white Gaussian noise (from the detector electronics) and the underlying Poisson-Gaussian noise of the image using patch-based algorithms[62]. Another report[63] uses non-linear anisotropic diffusion as part of a machine learning scheme to denoise images for electron tomography.

Recent work shows the use of a single column SEM with multiple beams and detectors[64] configured for fast data acquisition from the region of interest (ROI). Here, multiple electron beams from a micro aperture array (illuminated by a Schottky field source) are focused on the sample, and the secondary electrons from the sample are simultaneously detected by multiple detectors. The system uses up to 91 electron beams and detectors in parallel, and

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have been applied to semiconductor wafers and masks. Signals from additional detectors could also provide energy and trajectory information of the electrons generated by the beam-sample interaction, and 3D maps of the features. Another recent implementation uses multiple beam energies[65]. Since the beam penetration depth depends on the beam energy, the backscattered electrons at each energy level contain different information that is then deconvolved and combined using a blind deconvolution algorithm. An improvement that would further enhance 3D image acquisition would be to extend tilt SEM to multiple angles and combine the images.

Other improvements that could extend the use of CD-SEMs for GAA and beyond include low-damage and very low-energy operation (coupled with electrons from higher brightness sources), very low-electron-energy variation, and use of innovative aberration-corrected electron-optical columns[66], eliminating electron-beam-induced contamination, and dose rate management to minimize sample damage. Low-energy operation would be useful in measuring beam-sensitive low-contrast materials or filaments in nanoionics memristors as was previously done for Ag filaments in an Ag/H2O/Pt structure[67] or other types of beyond CMOS resistive switches and selectors[68].

Critical dimension small angle X-ray scattering (CD-SAXS).

CD-SAXS[69, 70] is a variable angle, transmission SAXS[71] measurement where X-rays scattered from a periodic nanostructure are analysed to non-destructively determine the average shape of the nanostructure (Fig. 3a,b). CD-SAXS is essentially single crystal diffraction where the lattice is the period of the structure and the “atoms” are the repeating nanostructured elements. CD-SAXS is analysed using an inverse, iterative approach where the calculated scattering for a trial shape function is compared to the scattering data. The trial shape is modulated until the calculated scattering matches the scattering data. CD-SAXS requires high energy X-rays (> 17 keV) for transmission through the silicon wafer and low divergence due to the small scattering angles that must be measured. Since the data are in reciprocal space, the scattering angles get larger and easier to resolve when the length scales get smaller. This makes the technique useful for feature sizes projected for GAA devices. CD-SAXS has been used to characterize a variety of nanostructures including FinFETs, directed self-assembly (DSA) and multiple patterning structures (Fig. 3c,d)[72-75], and can be used to determine parameters such as sidewall angle (SWA), linewidth, and pitch. Roughness is obtained as the deviation from the average shape and can be separated into lateral and vertical components. The primary limitation for CD-SAXS is the brightness of available compact X-ray sources, which leads to long measurement times[72].

For next generation device architectures, the primary factors for CD-SAXS applicability are the scattering contrast and scattering volume. In non-resonant scattering with high energy X-rays, the contrast is related to the periodic changes in electron density. Materials with high atomic numbers and high density with empty space between them will scatter strongly, while low atomic number materials and structures with small changes in electron density will scatter weakly. With regards to scattering volume, the primary effects are due to the structure thickness/height. Tall structures such as VGAA and 3DVLSI will scatter strongly. Thin structures such as 2D materials will scatter weakly. For example, although sub 2.5 nm

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crossbars[39] can be measured by CD-SAXS (if array is 50 μm), the reduced cross-scattering caused by the small sizes would degrade the signal. The primary effect of the scattering strength on the measurement is throughput. Weakly scattering samples will require major improvements in compact X-ray source brightness for realistic CD-SAXS characterisation times. X-ray sources with tuneable energy would allow resonant scattering to highlight the position of specific elements in the nanostructure[76].

The key advantages of CD-SAXS relevant to next generation devices are the small X-ray wavelength, the ability to measure optically opaque materials, and the deep penetration that allows non-destructive measurement of complex stacks. These attributes of CD-SAXS make it one of a few methods capable of measuring complicated 3DVLSI stacks without cross-sectioning the film. Many steps in the manufacturing process will have structures where the top layer in a complex stack is optically opaque. Examples include metallization layers and amorphous carbon hard masks that are frequently used when patterning high-aspect ratio structures. Another advantage of CD-SAXS is that the result is the average of millions of devices. Imaging techniques such as cross-sectional TEM typically sample too few devices to have the statistical significance needed to extrapolate the results to the billions of devices in the typical integrated circuit. Currently, CD-SAXS is rarely used in the fab due to the long characterisation time, but is an area of intense research because of its advantages. Improvements in high-brightness sources (10 to 1000 times) for CD-SAXS would transform it from a synchrotron and lab-based instrument to an in-line tool. CD-SAXS measurements can be made traceable to the SI length, by using calibration samples, displacement interferometry or length gauges to monitor the translation of the detector. A related method called X-ray ptychography (not covered here) uses coherent X-ray sources, and has been used to create full 3D images of dense processor chips with 14.6 nm resolution[77] over more than 10 μm range.

Scatterometry.

Scatterometry[78-80] is a non-imaging optical technique that allows sub-nanometre model-based measurements of overlay effects[81,82], geometrical CDs and optical constants (e.g., n & k) of patterned arrayed structures (Fig. 4a,b). This technique, a specialized variant of ellipsometry, simultaneously captures several deep-subwavelength size variations well-below conventional resolution limits through polarization and intensity changes in scattered light (Fig. 4a). Overlay measurements determine displacements between subsequent patterned layers, while, optical critical dimension (OCD) metrology relies upon the parameterization of the nominal geometry (i.e., line height h, linewidth w, etc.) and each materials' complex index of refraction ($\tilde{n} = n + ik$) as inputs for electromagnetic scattering computations. Parametric variation leads to a library of simulated intensity results indexed to these parameters (Fig. 4c). Simulation-to-experiment fitting yields quantitative parametric values, while the parametric uncertainty hinges on both the sensitivity of the measurement to that parameter and on correlations among these parameters. For scatterometry-based overlay, displacement between the layers is determined from intensity variations among the diffracted orders from stacked gratings. Although image based overlay (using specialized optical imaging tools) has traditionally been used in the industry, scatterometry-based overlay[82,83] is increasingly popular due to its precision and process compatibility[47].

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Despite inherent ambiguities associated with multi-variable sensitivities, scatterometers are metrology workhorses for determining CD due to the speed of scattering measurements. As the fitting is an inverse problem without a unique solution (Fig. 4d), sensitivities may not be distinct (for example, h and w each may alter the scattering similarly). Thus, experimental design is optimized to adequately distinguish among parameters; often, the wavelength λ is scanned from the ultraviolet to the near-infrared (which provides increased sensitivity) for a few fixed angles of incidence. SI traceable scatterometry measurements are difficult due to the parametric correlations, the number of approximations required[84], and the subsequent difficulties in establishing a documented uncertainty budget[85].

Experimental methods used by the industry are evolving to more completely capture the physical characteristics contained within the scattered light. One key technique now applied to scatterometric measurements is Mueller-matrix spectroscopic ellipsometry (MMSE)[86,87], performed by augmenting the rotating linear polarizers often found in conventional scatterometry with specific combinations of rotating phase retarders. With this added polarization control and analysis, MMSE allows the capture of cross-polarization and includes depolarization effects ignored by conventional scatterometry. Feature asymmetries (e.g, fin bending) and errors in overlay patterning (e.g., pitch-walking) have recently been characterized using certain non-symmetric values within the measured 4 × 4 Mueller matrix from MMSE[88]. MMSE has also been used to study stress induced dimensional changes in Si and $Si/Si_xGe_{1-x}/Si/Si_xGe_{1-x}/Si/Si_xGe_{1-x}$ nanosheet fin structures[89], and DSA patterned contact holes[90]. New simulation studies listed 16 parameters and showed reduced parametric correlation for MMSE for a VGAA parameterization (Fig. 4e)[91]. Alternatively, new implementations have combined high-magnification optics and angular control to yield collection of the -1st and 1st diffraction orders from the arrayed features, and has been used industrially for overlay and OCD with spot sizes of about 10 μm in diameter[81].

Currently, ten or more parameters are modelled, but obtaining adequate measurement resolution (i.e., parametric values and uncertainties) becomes more difficult with increased structural and materials complexity. As such, new approaches to scatterometry target design and new methods that more fully utilize the wavelength-dependent optical materials properties $\tilde{n}(\lambda)$ are increasingly important, including tailoring of the optical penetration depth. For monitoring interconnects, cross-grating target approaches that harness surface plasmon polaritons have been proposed for further enhancing the parametric sensitivity to CDs as well as to rounding and shape deformation[92]. For all CDs, angles and λ are optimized to nominally limit the measurement depth to that of the parameterized geometry, while well-selected infrared λ permits the measurement of buried layers. For 3DVLSI, model-based infrared reflectometry (MBIR), can be considered a type of transmission scatterometry that allows dimensional measurements of high-aspect ratio features[93].

Looking forward, scatterometric metrology of arrays of integrated quantum dots and 2D materials will require not only a measure of periodicity common in lithography but also an even more complete treatment of the optical properties of each material. A prevailing approximation is that the wavelength-dependent dielectric function ε (where $\varepsilon = \tilde{n}^2$ for nonmagnetic materials) for patterned features may be treated as isotropic. For dimensionally confined systems (Fig. 4f), this assumption may break down (e.g., yield poor fits) thus

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requiring the accurate treatment of the anisotropy in $\varepsilon(\lambda)$ as a tensor[94, 95], and better treatment of this anisotropy is an area of continuing research for MMSE. Dimensional confinement is not just limited to 2D materials but also to features patterned from nominally isotropic materials but with sizes approaching near-atomic scales. Use of the full tensor adds parameters to the fitting, complicating the electromagnetic simulation while also increasing parametric correlations. However, implementing scatterometry as part of a hybrid metrology scheme (explained later) helps reduce parametric uncertainties.

Transmission electron microscopy (TEM).

Two modes of TEM[96] (Fig 5a,b) are mainly used for IC metrology, high resolution TEM (HR-TEM) and high-angle-annular-dark-field scanning TEM (HAADF-STEM). HR-TEM images are formed by interference patterns from diffracted and transmitted electrons from a coherent incident beam illuminating the entire ROI. The apparent fringes do not necessarily correspond to the actual atomic columns. HAADF-STEM imaging uses a focused electron probe scanned point-by-point across the ROI. The scattered electrons come from a single atom or atomic column, and are detected by an annular ring detector where the observed intensity is either proportional to the Rutherford cross-section ($\sim Z^2$) or monotonic contrast in Z (this is more common). The resolution of state-of-the-art instruments is about 0.05 nm[97], and is useful for current and future IC device measurement needs for 3D and 2D materials[98] including atomic and device structures (Fig. 5c,d)[99, 10], strain[46], interface analysis[44], and film thickness[101]. Whole GAA device cross-sections can be imaged at lower resolution, and specific locations at higher resolution.

However, images of “atomic locations” do not necessarily mean true atomic resolution. Reliable atomic resolution could be obtained by probe/sample deconvolution, or reconstruction of the exit-plane-wave-function which contains phase information corresponding to positions of the projected atomic locations. Resolution is influenced by lens spherical aberration and sample thickness, among others (see Fig 5g for select dimensional error sources). TEM’s SI traceability comes from atomic lattice measurements (through X-ray diffraction) and is one of the few techniques where the rigorous steps necessary for obtaining the best resolution the method has to offer virtually ensures that the measurements could be made SI length traceable[102].

Recently, automated focused ion beam (FIB) combined with STEM have been developed to extract site specific ultra-thin samples for reference metrology in an implementation referred to as CD-TEM[103], and are also used for TEM tomography, allowing 3D measurements. Work is underway to use the same type of automated FIB capabilities to fabricate on-demand functionalized critical dimension atomic force microscopy (CD-AFM) tips, and evaluate them in the TEM. The TEM information adds length traceability, but could also be used to model and correct tip induced geometric distortions. TEM tomography images combined with molecular simulations have been used to provide insight into the origin of defects in block copolymer materials used for DSA[104], leading to better designs of DSA templates.

Some of the most difficult samples to image with TEM are beam-sensitive low-contrast materials (e.g. CNT, graphene, MoS_2) proposed for beyond CMOS architectures (Fig. 1c,d).

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TEM ptychography (coherent diffractive imaging)[105] methods are under development to allow acquisition of high resolution images from low-contrast materials. One technique acquires simultaneous STEM and quantitative phase contrast images by locating a ptychographic camera at the high angle annular detector (Fig. 5b) and recording the non-aberration-corrected signals (needed for phase imaging). The signal is processed to obtain the phase image and then corrected for aberrations. Another new approach uses pixel array detectors with a large dynamic range and full field ptychographic techniques to recover the phase information[106]. The z-contrast images are complemented by the phase images, allowing practical imaging of 2D materials at high resolution. Other applications that will benefit from such beam-sensitive implementations include in-situ memristor characterisation[67], where TEM has been used to study the influence of geometry, and thickness variation in interfacial layers[107], among other parameters.

Compressed sensing was recently demonstrated for STEM[108], where the relevant information could be reconstructed from a subset of the acquired data. Here, the beam was blanked intermittently using a pseudorandom generator as it scanned the sample, limiting the dwell time and possible damage. Such techniques could be combined with TEM ptychography and used for low-contrast materials. A consideration would be to ensure that the reconstructed information is enough for metrology applications. The main limitation of the TEM is that it is destructive, most samples need to be cross-sectioned and thinned down to well below 100 nm. This precludes certain applications.

Atomic force microscopy (AFM).

The basic principles of AFMs involve positioning a small tip (<10 nm radius) to interact with the surface, where it can sense a wide range of forces while scanning the sample. For topography measurements, sub-nm resolution (<1 nm lateral and <0. 1nm vertical) is routine, and true atomic resolution is achievable under suitable conditions[109]. The variety of forces detected during the tip/sample interaction, including attractive and repulsive, induced by electrostatic, magnetic, and chemical coupling has resulted in modes that are optimized for specific physical properties (Fig. 5e). With the tip in near-contact, applications include direct probing of electric fields (electrostatic force microscopy), work functions differences (kelvin probe force microscopy)[110], and magnetic fields (magnetic force microscopy). Lateral resolution of about 10 nm to 20 nm has been demonstrated for these techniques. Important for nanoelectronics is the direct probing of carrier profiles; these could be obtained by sensing capacitance or spreading resistance changes at the tip-sample junction. These techniques have a lateral resolution ranging from 1 nm to 10 nm, high dopant gradient resolution (about 3 nm/dec) and dynamic range of $10^{15}$to 10^{21} (atoms/cm^3)[111]. However, shallower junctions and lateral dopant diffusion in 3D devices calls for a full 3D analysis attempted by different concepts but still challenging[111]. All AFM modes can be applied to IC measurements, here we focus on dimensional applications.

AFMs optimized for CDs (3D-AFM)[112-115] are used for nanowires and related dimensional parameters with uncertainties of less than 1 nm[116,117]. 3D-AFM, which uses two-axes cantilever vibration or tilting of the scanning head, eliminates certain tip-shape distortions[118], but the larger tips or the clearance needed for rotating heads limit trench sizes

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that could be measured. In topography mode, AFM is less sensitive to materials' differences and as such could be used for low-contrast materials such as those shown in Figure 1d or in probing memristor nanodevices[67] where it has been used to study the shape dependent performance of ribbed and planar TiO_2 structures[119]. AFMs can be made directly traceable to the SI length using displacement interferometry, or with calibrated samples[120-122]. See Fig. 5g for select error sources. A method to extract contours for OPC verification from CD-AFM images was recently demonstrated[123]. Since CD-AFM images contain reference sidewall data in the scan direction only, the techniques include profile extraction from orthogonal scan directions, filtering, and composite contour formation. The output could be used to directly verify OPC features, or calibrate CD-SEM OPC profiles.

For patterned features, the proximity of two sidewalls can make it difficult to interpret surface forces and limits the size of the tip that could be used. Recent work using distributed force models to interpret tip-sample interactions show that 3D-AFM sidewall measurement uncertainty could be reduced to less than 1 nm [124]. Studies with FIB fabricated ball-capped and bent CNT tips indicate that complex feature geometries could be imaged by using tips that are optimized for specific shapes[125]. Tip-wear[126], size, and shape characterisation[127] remain active areas of research because they affect the apparent size and shape of measured features. Activities includes developing wear resistant tips[116], wear monitoring techniques[128], and developing a fundamental understanding of nanoscale wear mechanism such as by systematically studying different external tip loading conditions and sliding distances, among other parameters[129]. Other activities include new tip characterization methods for CD-AFM using Si/SiO_2 heterostructures, reconstruction methods using dexel representation[130], and blind reconstruction[131]. Improved tip/cantilever technologies has been shown to increase positional stability (to < 0.03 nm)[132] and reduce drift, important for applications with sub-nm tolerances.

Among scanning instruments, AFMs are relatively slow, and although used in most areas of nanotechnology research, for fast paced measurements required in IC production, it is limited to niche applications or where faster options are unsuitable. Promising new research include non-raster scanning using contours of the feature to obtain 3D information. A recent example uses constant angular velocity spiral scanning in the centre and transitions to constant linear velocity toward the edge of the scan[133], reducing image acquisition time. Other proposed non-raster scanning strategies include rotational[112], spiral scanning[134,135], and two-dimensional Lissajous[136]. High speed AFMs (HS-AFM) combines small cantilevers (with low spring constants and high resonant frequencies), fast scanners and detectors, and vibration control to image samples at 10 to 20 frames/second (essentially video-rate speed)[137]. Although HS-AFM has been mostly applied to biological samples, it could be useful for IC applications where the general patterns are known, and the scan can be optimized accordingly.

Hybrid or combined metrology

No single instrument has the full capabilities (for example, resolution, speed, low levels of uncertainty) needed to characterize the whole set of parameters of complex devices, so the integration of multiple tools is required. As such, hybrid or combined metrology is one of

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the most important measurement strategies that could be used to extend the applicability of current instruments. Statistical and combinatorial methods have been used to allow complementary analysis techniques to be applied to the same area, utilizing the best measurement attributes of each technique[138].

Although multiple instruments are routinely used to obtain information (for example, correlative microscopy), statistical hybrid metrology methods for model-based measurements reduce parametric uncertainties for all parameters, not just those provided by a second instrument. For example, in scatterometry-based linewidth measurements, regression models include several parameters where values and uncertainties from instruments better suited for such measurements (e.g., CD-AFM for SWA, and LER), can be incorporated, thus constraining the set of potential fitting solutions (Fig. 4d)[139]. Improvements of as much as 4 nm for top width after OCD hybridization with AFM are common[138]. Other combinations include CD-SAXS and SEM[53, 140]; SEM and OCD[140, 141].; AFM and SEM[123].; AFM and TEM (Fig. 5f)[142].; HAADF-STEM and atom probe tomography[143]; OCD, X-ray fluorescence (XRF) and electrical characterisation[144].; and electrical, AFM, and optical[145].

A key issue that will increasingly affect all aspects of IC device measurements is traceability[145, 146]. Given that properties and functionality at the nanoscale are governed by absolute size, traceability of nanoscale dimensional measurements is crucial to the success of nanomanufacturing, and indispensable for valid comparisons of the results of various measurement techniques. This is necessitated by smaller feature sizes and hybrid metrology implementations mentioned above. Note that traceability does not necessarily ensure high precision or accuracy and only indicates that the results can be traced through an unbroken chain of measurements to a standard or reference. Measurement precision and stability as currently used by the industry are still more important than absolute accuracy/traceability for most applications. Traceability is not a priority if either the instrument or process is unstable. If the measurement tolerance is large enough and the resolution of the instrument is good enough, then measurement precision and instrument fleet matching can be adequate.

However, traceability to a reference becomes important when comparing different instruments, combining their results, or comparing results of measurements made at different facilities[147]. Also, in some cases, the size and performance dependence of the measurand could preclude methods that are not traceable. For example, the channel thickness and placement of gate electrode for the proposed 1 nm gate length MoS_2 transistor shown in Fig. 1d affects performance. When comparing the performance of such transistors, sub-nm deviations could produce very different results, and instrument traceability (with its associated rigorous analysis of error sources) is one of the few ways to help identify and eliminate errors at this length scale. The same goes for the proposed around 2 nm by 2 nm device areas for the memristors[39], where sub-nm differences could represent a considerable change in overall area, and hence device density and performance.

A related issue to consider when using different instruments for the same parameter is methods divergence[148], which is when different techniques produce different results for the same nominal measurand due to differences in error sources, dimensionality/content

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definition [149], probe-sample interaction, and measurand definition. Two techniques could each have a measurement precision of less 0.1 nm, but deviate by more than 3 nm, indicating that each instrument's response to the same parameter is different. Examples include an offset of 2.7 nm between the middle CD as measured by CD-AFM and EUV scatterometry[150] and a difference of 0.8 nm in CD for nominally 13 nm lines as measured by CD-SAXS and model-based library SEM[53]. In these cases, traceability to a reference (and carefully identifying the error sources) could help reduce deviations[140], and clarify if these are fundamental differences in the measurement physics. In addition, standardized parameter definitions and sample registration methods need to be implemented to ensure agreement at the nanoscale. At reduced dimensions, understanding these factors will be fundamental to rectifying apparent discrepancies.

Emerging and potentially disruptive technologies

In addition to hybrid or combined metrology, the following technologies have the potential of fundamentally changing the way IC metrology is done due to the nature of the problems they address and their broad applicability.

Advanced data analytics.

Advanced data analytics refer to methods used for big data handling, inference, prediction, and decision making, and include machine learning (ML) and deep learning[151] among others. Due to fully automated measurements throughout the IC manufacturing process, large amounts of data that could be mined for insight are already being collected. For example, high resolution SEM and interferometric optical microscopy can easily produce gigabits of data in a single set of measurements[152]. Although metrology has always been computationally intensive, what is different about the new methods and makes them potentially disruptive are their autonomous or semi-autonomous implementation and applicability to different aspects of IC such as material discovery[153], development, manufacturing, and test. An approach that is gaining wide application is ML, which uses computational techniques to learn information directly from data without the use of physical models. This is proving to be useful in situations where the system is not well understood or has too many variables with unknown correlations. Different types of ML models can use known input and output data to develop predictions of similar input data (supervised) or could use just input data to find hidden patterns, structure, or correlations (unsupervised). For metrology, this could be extremely helpful for parameters that cannot be directly measured, but could be correlated with measurable quantities. In cases where physical systems modelling is computationally intensive (or some relationships are not fully understood), ML can be used to develop data driven models that are faster and can discern previously unidentified connections between process parameters and decrease time to solution. Results from ML can also help reduce physical modelling variables.

ML and other advanced data analytics techniques are already being applied to a wide range of metrology issues and can be used for specific measurands or for factory wide applications. For example, deep learning techniques have been applied to image recognition, automatic categorization, and labelling of images. SEM data was trained to recognise and

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classify features such as 1D nanowires, 2D films, and 3D patterned surfaces among others[154], leading to not only faster analysis of individual images but also correlations within the data. In another example, a neural network was trained with resist shrinkage and CD-AFM data and Bayesian probabilistic weight determination was used to estimate CDs for EUV resist trenches[155]. The results showed lower measurement uncertainties when compared with other methods, and highlights how ML could be used to optimize a hybrid metrology setup. Cognitive learning (a type of ML) has also been used to speed up complex characterisation and analysis of IC features, such as object detection, classification, and automated measurements[156]. In another example, pre-exposure metrology data from ultraviolet level sensor of a lithography system was used to predict clamped wafer shape, and then hierarchical clustering with dendrograms provided insight on overlay[157,158]. Other interesting uses include autonomous probe tip monitoring and reconditioning, where a neural network was trained (by a small set of images) to identify isolated dangling bonds at the end of a tip and to apply electrical pulses to sharpen the tip[159]; using ML to develop sampling strategies for OCD and XRF for electrical test prediction; and pattern analysis and prediction for automated design layout[160]. Note that ML and related techniques could be implemented as part of established automated process control (APC)[161] and virtual metrology techniques currently used in the industry, and the information linked to factory wide data or applied to other metrology issues[138, 155, 157, 158, 162] Virtual metrology refers to "…the technology of prediction of post process metrology variables (either measurable or nonmeasurable) using process and wafer state information that could include upstream metrology and/or sensor data " and would benefit from these techniques[163].

More broadly, Kalinin et al. have proposed a framework for using data analytics to advance the scientific discovery process[164]. They illustrate how advances in acquisition techniques and data analytics could be used to capture, transfer, and compare multimode microscopy data to a wide body of work stored in "multimodel response libraries" thus reducing the time between data acquisition and when it becomes useful "community-wide knowledge." This is an interesting concept, and although much broader in scope (with some intellectual property issues to consider), it could be particularly useful for metrology. Information on instrument response to different samples, operating conditions, and applications from a wide range of users could be used to improve instrument capability, and would complement APC, hybrid and virtual metrology.

Sub-wavelength imaging techniques.

These techniques allow imaging beyond classical diffraction limits and can be particularly useful if configured to characterize nanodevices parameters not covered by the examples above. Promising techniques include, plasmonic assisted optical focusing[165] which can focus light to subwavelength size and can detect optical losses, chemical properties, and defects in hard to reach areas of device structure. Evanescent waves[166] which could be leveraged to use near field nonresonant effects to produce nanoscale-(<25 nm) resolution frequency-independent imaging from the visible to the THz regimes. A technique that could be borrowed from biological imaging is super resolution microscopy. Here, different measurands are imaged by localizing and activating different parts of the sample[167], measuring them separately and then combining them to achieve a resolution that one image

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could not have produced. These methods are not optimized for IC applications and in some cases the resolutions are relatively large, but their capabilities make them promising candidates for further investigation, and if successful could make an impact on IC metrology.

Open measurement questions

Although progress has been made in improving instrument capabilities, challenges (and opportunities) remain. Noise is the most pervasive, and comes from a variety of sources (including vibration, shot noise, probe/sample interaction, detector, and stray EM fields). Even if an instrument has the capability to discern 1 nm differences, noise at just below that level could make some measurements unfeasible or dramatically increase the uncertainty. More specifically, for VGAA, key patterned features such as 6 nm holes need to be measured at the bottom and the top to check for dimensional variation in the hole. At a different length scale, the advent of stacked chips means that measurement of (10s of μm long) through-silicon-vias[168] would be critical. For 3DVLSI structures, the presence of different technologies at each layer could make it difficult for techniques (even those with sufficient depth of focus) to simultaneously capture multiple parameters due to differences in material contrast.

Unfortunately, no single method has the range and/or resolution to adequately make these measurements. New defect detection capabilities are needed. Optical instruments at present wavelengths are not adequate for single-particle defect inspection, and higher resolution instruments do not have the range and throughput needed[54]. Although electron beam techniques are widely used, assessing beam damage for thin structures is difficult. This limits the type and thickness of samples that could be measured.

Conclusions

The 1994 National Technology Roadmap for Semiconductors[169], projected a minimum feature size of 0.35 μm for 1995. By comparison, the smallest device width projected by the IRDS for the years 2027-2033 is 6 nm (Fig. 1b). As device sizes shrank, and new lithography techniques and materials were introduced, the underlying device architecture stayed the same. That changed with the introduction of FinFETs, and is about to change again with GAA, 3DVLSI, and eventually to a yet to be defined beyond CMOS architecture in what was recently referred to as the era of hyper-scaling[170].

We reviewed the main IC dimensional metrology instruments that would be used for these devices, their capabilities, limitations, and potential for improvement. These techniques already play key roles in IC dimensional measurements or, in the case of CD-SAXS, have the potential to do so. The combination of small feature sizes, functionally important non-planar parameters, and increased significance of stochastic effects means that no single instrument would be able to meet the demands of some of the measurands. Hence, improved instruments, hybrid metrology, increased use of modelling and simulation, or adaptations from other fields are needed. Overall, current instrument limitations are mostly driven by

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engineering issues, rather than the underlying physics (Table 1). This does not make the limitations any less daunting, but indicates that there is room for improvement.

Looking forward, advanced data analytics could help ensure that only the data needed for critical decisions are collected, thereby reducing the overall cost. The use of techniques such as machine learning and measurement physics modelling in combination with process information would not only solve metrology problems, but could help develop completely new measurement techniques for these end of roadmap devices. It is also possible that technological advances could obviate the need for some measurements. Defect tolerant systems for neuromorphic chips is an area of active research[171,172], and could be applied more broadly. In such systems, the chips can learn to work around certain deficiencies (dimensional variations, for example) and reallocate resources to optimize performance. Such implementations would not remove the need for all measurements but could help in specific scenarios where measurements are prohibitively expensive.

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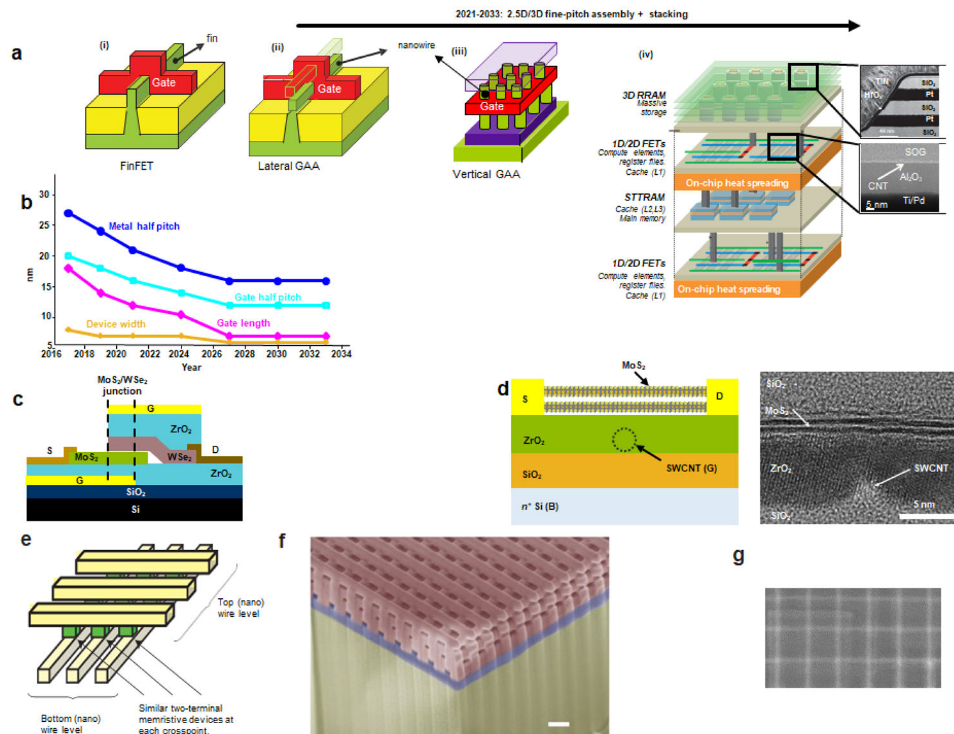

Figure 1 |. Proposed advanced IC devices.

a, Evolution of device architectures as forecasted by the IRDS. (i) FinFET is projected to be the leading device option until 2021 while gate-all-around (GAA) device and 3D assembly stacking are projected to commence in 2021. Beyond 2027 3D device stacking is projected to start with vertical FETs. (ii) for lateral GAA, the fin is now composed of several nanowires or nanosheets whose size and uniformity would need to be controlled. (iii) for VGAA, the gate is now horizontal (while channel orientation become vertical), and becomes a film measurement with multiple stacks. (iv) 3DVLSI have different technologies stacked together, in addition to VGAA metrology issues, interconnect metrology becomes important. **b**, Scaling projection of key dimensions such as metal half-pitch, gate (poly) half-pitch, gate length, and device width. **c**, Schematic diagram of proposed vertical heterostructure tunnel field-effect transistor using 2D materials (MoS_2 and WSe_2) and cross-sectional TEM image of a representative device showing top and bottom gates. The gate is a film measurement, so interface properties, film homogeneity, and defects are key metrology issues. **d**, Schematic diagram of proposed 1D2D-FET with a MoS_2 channel and single wall carbon nanotube (SWCNT) gate and a representative TEM cross-sectional image showing a SWCNT gate, ZrO_2 gate dielectric, and bilayer MoS_2 channel. Both the channel material and CNT would be challenging to measure. **e**, Schematic diagram of crossbar structures for high density memristor circuits. **f**, A cross-sectional SEM image of 3D stacked Si memristor crossbars –100 nm X 70 nm, and 200 nm pitch. Scale bar, 200 nm. **g**, SEM image of 8×8 nm^2 memristors in a crossbar array. RRAM, resistive random-access memory. STTRAM, spin-transfer torque magnetic random-access memory. Panels adapted from: **a**, i-iii, ref. 5 ECS; iv, refs.14,[27,28] IEEE; **c**, ref.[29] American Chemical Society.; **d**, from information in ref. [30],

AAAS; **e**, ref.[34], Macmillan Publishers Ltd.; **f**, ref.[38], Macmillan Publishers Ltd.; **g**, ref.[32], IEEE.

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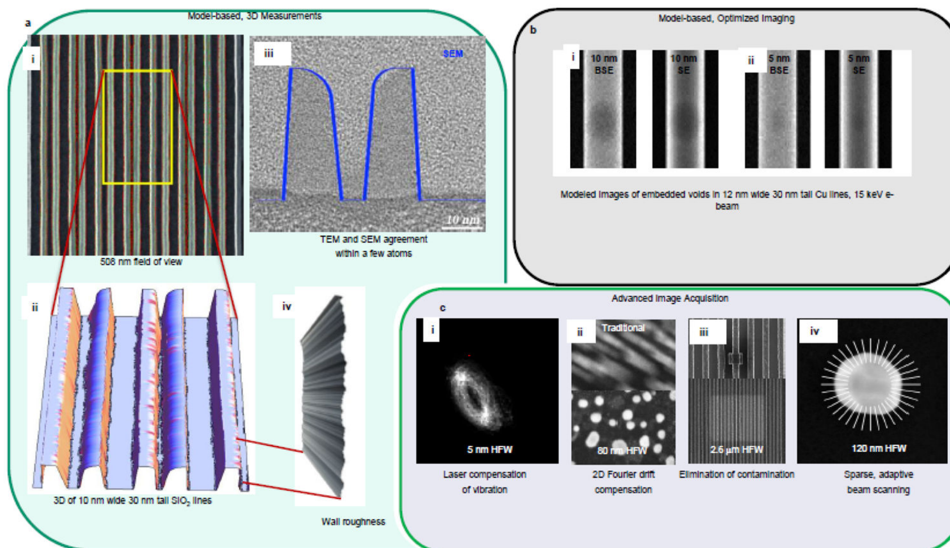

Figure 2 |. Advanced CD-SEM imaging.

a, Accurate, model-based 3D measurements of size, shape and roughness of 10 nm finFET structures. (i) top down CD-SEM image. (ii) model based 3D rendering from multiple angled beam images. (iii) profile of modelled SEM image overlaid with TEM cross-section shows good agreement, and is also a form of calibration as long as errors are accounted for. (iv) sidewall roughness of modelled 3D image. **b**, Optimized, model-based determination of best imaging/measurement conditions and signals. 12 nm lines with (i) 10 nm and (ii) 5 nm embedded voids simulated using a series of instrument settings. The setting(s) that yield the best image are used for actual measurement. **c**, Examples of advanced image acquisition techniques needed to obtain sub-nm resolution images; (i) laser-interferometry is used to monitor stage vibration and drift for fast image series, and (ii) 2D Fourier-transform is used to identify specific image location and align the series to correct vibration and drift effects. Uncompensated image (top) and 2D Fourier drift compensated image (bottom). (iii) plasma- and laser- based elimination of contamination to ensure ultra-high cleanliness; (iv) sparse, adaptive beam scanning strategy. This allows fast image acquisition, minimising the beam damage by limiting amount of time the beam is in contact with the sample. BSE, back scattered electron; SE, secondary electron; HFW, horizontal field width.

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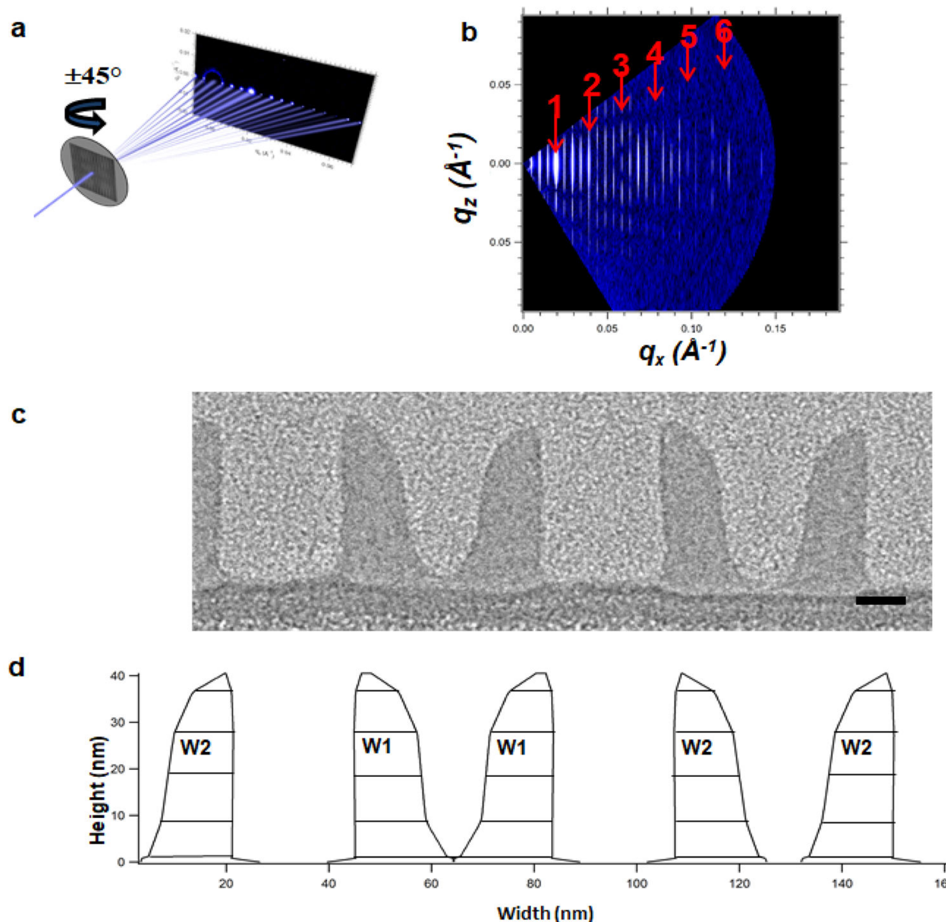

Figure 3 |. CD-SAXS operations and feature shape models.

– **a**, diagram illustrating variable angle transmission SAXS on a periodic nanostructure. **b**, Example of scattering pattern obtained from a pitch quartering sample. Red arrows mark the peaks from the nominal spacing. Other peaks are superlattice peaks from the pitch quartering. **c**, TEM cross-section of the pitch quartering nanostructure. Scale bar denotes 10 nm. **d,** Six trapezoid stack shape models for cross-sectional view obtained from fitting CDSAXS data. W1 and W2 denote that the width of the two sets of mirrored pairs is different. The number of parameters in a model is 3N+5 where N is the number of trapezoids in a stack. Defining the edges of the trapezoids with functions instead of allowing them to float reduces the number of parameters but could put constraints on the space sampling of the trapezoid edges and may create correlations between adjacent vertices. Panel adapted from: a, ref.[72], SPIE; b,c,d, ref.[74], International Union of Crystallography.

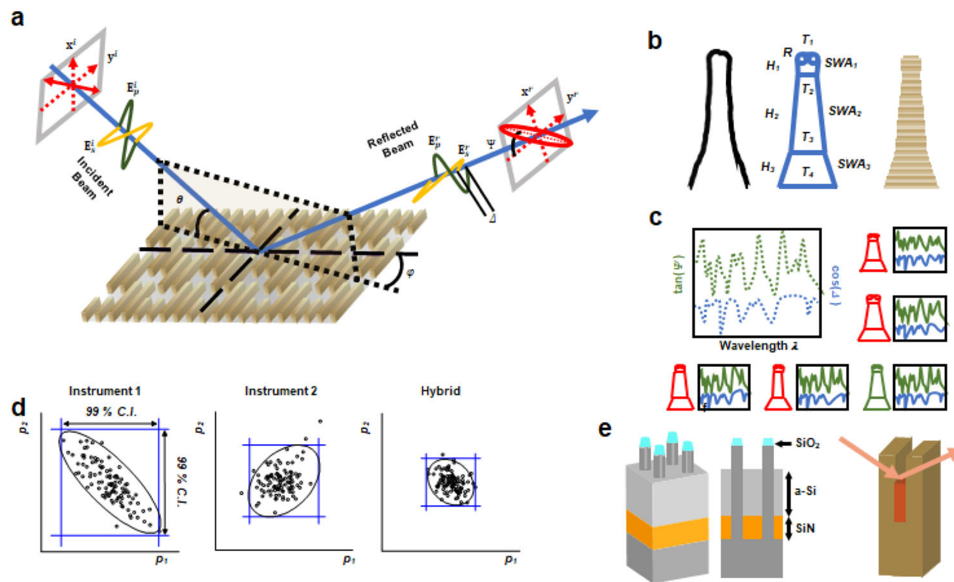

Figure 4 |. Principles of optical scatterometry with future challenges.

a, Schematic of light scattering off 3-D fin structures. Incident linearly polarized light with amplitude E^i is scattered and collected at angle $-\theta$. Two prominent quantities measured are the rotation of the now-elliptical polarization, ψ, and phase lag . Figure after information in refs. 86 and 91. **b**, Three schematics showing a cross-section of a fin, its geometric parameterization, and its segmenting for electromagnetic simulation; **c**, Schematic of experimental data and library fitting. Here, tan(ψ) and sin( ) are measured as functions of wavelength and also determined through simulation for a library of possible parametric values, with the best-fit parametric values corresponding to the green parameterization; **d**, For the parametric uncertainties, increased correlation also increases these uncertainties. To illustrate, assume a simple, two-parameter model for scatterometry Instrument 1. With a correlation between parameters p_1 and p_2 of c = −0.81, the 3σ uncertainty (shown by the 99 % confidence interval) is large. A better-optimized scatterometry Instrument 2 shows less uncertainty for c = 0.35. But, if these two instruments measured the same features and are combined using hybrid metrology, the uncertainty is greatly reduced. Additional information from multiple instruments is likely the necessary requirement for extensibility to future devices, such as VGAA. **e**, Scatterometry model proposed for upcoming VGAA structures featuring 16 parameters to be solved for the 3-D structure. A recent publication indicated c > 0.8. From Ref.[91]; **f**, Another example of a scatterometric vertical 3-D CD measurement envisioned for an ultrathin material exhibiting a strong anisotropy in its dielectric function ε thus disallowing current, simpler treatments of optical properties as $n(\lambda)$ & $k(\lambda)$ and requiring further parametrization and a *priori* information. Panels adapted from: e, ref.[91], American Institute of Physics;

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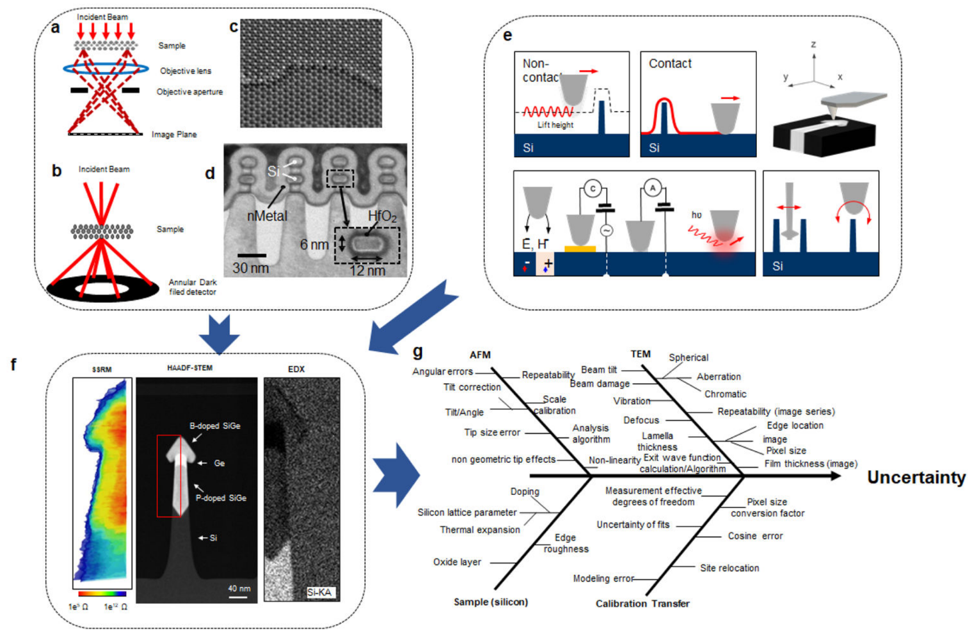

Figure 5 |. Combined TEM and AFM measurements.

Simplified schematic diagram of **a**, HR-TEM, (b) HAADF-TEM. **c**, exit wave phase image of double layer graphene reconstructed using a series of HRTEM through-focal lattice images., **d** TEM images of gate-all-around silicon nanosheets. At this length scale whole devices can be imaged, though not with atomic resolution. **e**, Schematic representations of the basic principles of operation for AFM modes. A nanosized tip is used to sense the surface by non-contact or contact tip-sample interaction. Long range forces including electric and magnetic fields can be measured by studying the frequency changes in an oscillating tip, while local electrical properties such as capacitance or resistance are measured when the tip is in direct contact with the biased sample. In addition, near-field optics techniques are used to explore chemical mapping and optical properties with nm-precision. Since the advent of fins, the conventional sensing scheme of AFM has been modified by dedicated tip-geometry (i.e. T-shaped apex) and tilting scan heads for advanced process monitoring of fins (e.g., sidewall and edge roughness). **f**, Site-specific structural, chemical and electrical information obtained by combination of TEM and SSRM on raised source/drain regions of a SiGe-based finFET (in the red rectangle area). **g**, A fishbone diagram showing possible calibration errors when TEM is used to calibrate other instruments or when measurements from two instruments are combined. Possible error sources include influence factors from TEM, sample, CD-AFM, and the calibration process itself. The uncertainty values of artifacts calibrated with TEM could be as low as 0.8 nm. SSRM, scanning spreading resistance microscopy; EDX, energy dispersive X-ray spectroscopy; Panels adapted from: **c**,ref.[99], Macmillan Publishers Ltd; **d**, ref.[100], IEEE.

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Table 1 |

Comparison of IC dimensional metrology methods

	Critical dimension-scanning electron microscopy	**Scatterometry**	**3D- Atomic force microscopy**	**Critical dimension –small angle X-ray scattering**	**Transmission electron microscopy**
Underlying Physics	Electron beams- matter interaction	Light scattering from periodic structures	Surface forces - tip interaction	X-ray scattering from electron density spatial variations	Electron beams-matter interaction
Resolution (lateral and vertical)	≈0.3 nm focusing capability	Model-dependent;≈ 1 nm, vertical and lateral	<0.01 nm vertical;<1 nm lateral	≈0.1 nm for average structures- depends on SNR	0.05 nm lateral
Range (field of view)	50 nm to 10 mm	10 μm and larger; dependent on spot size	10s of nm to > 500 um depending on scanner.	50 μm to 200 μm	10s of μm at low resolution
Advantages (for a hypothetical 5 nm patterned line)	Local and global information; sub-nm level measurement accuracy.	Non-scanning (i.e. fast); non-destructive; in-line* compatibility	Full 3D and limited sample preparation, in-line compatibility; nm level measurement accuracy.	Measures ensemble averages for large array; high resolution; larger angles as periodicity gets smaller; Fourier transform calculation is fast	Cross-section imaging capability for whole line imaged at atomic resolution, in-line# compatibility
Current instrument limitations (for a hypothetical 5 nm patterned line)	Drift; vibration; contamination; beam damage; lack of sub-nm beam placement accuracy; Information volume must be folded into size/shape determination	Inapplicable to isolated lines; spot size should underfill line arrays	Tip-size- (dense structures); relatively slow; Aspect-ratio (e.g., increased fins height reduced fins pitch)	Compact X-ray sources limit throughput;scattering interaction is weak Inapplicable to isolated lines;	Sample needs to be cross-sectioned – destructive; beam projection artefacts and noise. Relatively small high-resolution field of view.
Ultimate limitation due to underlying physics	Electron beam wavelength;	Non-uniqueness of solutions for inverse light scattering problem	Tip size; difficult to interpret tip/sample interaction in small confined spaces such as contact holes.	Interaction volume is small	Electron beam wavelength; beam steering errors.
SI length Traceability	Calibration samples;displacement interferometry.	Calibration results are non-transferable; uncertainty budget challenged due to geometry approximations	Calibration samples;displacement interferometry	Calibration samples; traceable translation of detector	Lattice information from x-ray diffraction (short traceability path)

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	Critical dimension-scanning electron microscopy	Scatterometry	3D- Atomic force microscopy	Critical dimension –small angle X-ray scattering	Transmission electron microscopy
Key error sources	Drift; vibration; contamination; EM fields	Parametric correlation; geometry parametrization; unfitted parameters (e.g., pitch)	Tip induced artefacts; tip/sample interaction interpretation.	SNR; shape models that cannot fit the correct solution; uniqueness of solution for noisy data or sample structure is unknown.	Lens aberration; sample preparation; beam damage (material dependant)
Potential improvements	Very low electron energy variation; displacement laser interferometry; elimination of e- beam-induced contamination; dose rate management	Spot size; target area reduction for more in-die placement; hybridization	Scanning speed; better modelling of tip/sample interaction	Higher brightness X-ray sources; higher coherence of X-ray source.	Electron dose management; improved sample preparation techniques

*In-line means that it could be used inside a semiconductor manufacturing fabrication (“fab”) environment.

#TEM is increasingly being optimized for use in the fab, see ref. [103]. SNR, signal to noise ratio; EM, electro-magnetic; Scatterometry information after ref.[95]