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Dual-mode Microelectrode Array Featuring 20k Electrodes and High SNR for Extracellular Recording of Neural Networks

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Abstract

In recent electrophysiological studies, CMOS-based high-density microelectrode arrays (HD-MEA) have been widely used for studies of both *in-vitro* and *in-vivo* neuronal signals and network behavior. Yet, an open issue in MEA design concerns the tradeoff between signal-to-noise ratio (SNR) and number of readout channels. Here we present a new HD-MEA design in 0.18 μm CMOS technology, consisting of 19,584 electrodes at a pitch of 18.0 μm. By combing two readout structures, namely active-pixel-sensor (APS) and switch-matrix (SM) on a single chip, the dual-mode HD-MEA is capable of recording simultaneously from the entire array and achieving high signal-to-noise-ratio recordings on a subset of electrodes. The APS readout circuits feature a noise level of 10.9 μV_{rms} for the action potential band (300 Hz - 5 kHz), while the noise level for the switch-matrix readout is 3.1 μV_{rms}.

Index Terms

Microelectrode array; active-pixel-sensor; switch-matrix; full-frame; signal-to-noise ratio

I Introduction

Recording and analyzing neuronal signals can provide insights into how neurons communicate with each other [1], [2]. CMOS-based HD-MEAs offer the important advantage of high spatiotemporal resolution recordings in comparison to traditional passive MEAs [1]. However, a major challenge in HD-MEA design includes the trade-off between noise performance, power consumption and electrode density. To mitigate these tradeoffs, two major types of readout schemes have been used. The first one is the active-pixel-sensor (APS) concept, a scheme also frequently used for in-vivo neural probes [3], [4]. This architecture consists of active circuits in each pixel, which, in most cases, include pixel amplifiers. APS-based HD-MEAs have the advantage that all electrodes of the array can be read out during every frame. However, due to the limitations in the total power consumption and the available area in each pixel, APS-based HD-MEAs tend to have a higher noise levels [5]–[7]. Moreover, the APS pixel size tends to be larger in order to accommodate all needed

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circuitry unit, which, in turn, entails a lower spatial resolution. The second HD-MEA type is switch-matrix (SM)-based, and the readout circuits are located outside the array, where no area restrictions apply. SM-based HD-MEAs feature a flexible routing scheme and higher signal-to-noise ratios (SNR) [8]–[10]. However, the improved SNR comes at the costs that only a fraction of the electrodes (typically < 10%) can be read out simultaneously, which may increase the complexity of experiments.

Here, we present a dual-mode HD-MEA (DM-MEA), which combines the advantages of SM and APS into a single MEA device. DM-MEAs can record from all the electrodes in the array and achieve high SNR at a selected subset of electrodes at the same time. Based on a previously developed prototype [11], the new DM-MEA presented here is targeted at studying both, single-neuron and network-level neuroscience phenomena. The new DM-MEA includes 19,584 pixels and APS readout channels, 246 SM readout channels, and 8 stimulation buffers. This enables to read out every electrode by using APS and SM techniques simultaneously, and to electrically stimulate through selected electrodes by using voltage-controlled or current-controlled stimuli.

II System overview

The DM-MEA consists of 108×192 pixels with a pixel size of 16.8×18.2 μm^2 in a hexagonal arrangement [10], resulting in 19,584 electrodes at an electrode pitch of 18.0 μm. Each pixel includes one pixel amplifier for APS readout and one SRAM cell for the connection to the SM readout or stimulation buffer. Additionally, there is direct access to every electrode for stimulation from an external signal source. The system includes 19,584 APS readout channels, 246 SM readout channels, and 8 stimulation buffers. The system details are summarized in Fig. 1.

A APS Readout Circuits

For APS readout circuits, there are three main parts: pixel amplifier, column amplifier and ADC (Fig 2).

The first stage of the readout circuit, the in-pixel amplifier is located underneath the electrode to drive the routing wires in time-multiplexed operation. A1 is a two-stage, AC coupled, inverter-based amplifier. C_{input} is the input MIM capacitor for AC coupling so as to remove the DC offset from the electrode. The input stage of A1 is an inverter-based amplifier consisting of M1/M2. VDD_1 is 0.8 V to reach a gain of 42 dB. R_1 can be operated as either a switch for resetting the operating point or a pseudo-resistor to build a high-pass filter to reject the low-frequency fluctuation from the electrode. After the input stage, there is an RC low-pass filter consisting of a voltage-controlled pseudo-resistor made from complementary NMOS/PMOS and a MOS-capacitor made from a PMOS transistor. The MOS-based structure was chosen due to the limited area in each pixel. To reduce the aliasing noise from the following sampling process, the cut-off frequency was set to 5 kHz. The sampling clock has been programmed to have a frame rate of 11.6 kHz.

The amplified signal from the pixel is buffered by A2 and further amplified by a switched-capacitor pseudo-differential amplifier A3 with a programmable gain of 6 – 18 dB. In order

to compensate for the DC offset, an auto-zeroing scheme was used and the single-ended signal is converted to differential signals for further processing. A 10-bit time-interleaved SAR ADC has been chosen for digitizing the amplified signal. Compared to traditional SAR ADCs, the time-interleaved ADC has two sets of capacitor arrays as DAC. This feature enables a longer sampling period and thus relieves the requirements for the ADC driver A4. The capacitor array uses a split-array structure, and the interleaving scheme is shown in Fig 2. While one capacitor array is connected to the input and samples the input signal, the other capacitor array is connected to the comparator and digitizes the previously sampled signal. The ADC clock is 50 MHz, and there are 48 ADCs for APS readout, which yields a total data rate of 2.4 Gb/s.

Since timing is critical for the readout chain, a central digital controller was used to control the timing of the APS readout circuit. It generates the clock signals for the row decoder, SC amplifier, multiplexer, and ADC. The row decoder generates the sampling clock (*EN*) for each row at the frequency of 11.6 kHz, and can be configured to skip rows to get higher temporal resolution. For the column readout, the sampling clock (*SH*) and mux clock (*MUX addr*) are generated for the timing of the column readout during each frame. For the ADC, signals are generated for the interleaving timing (Φ_0, Φ_1) as well as for SAR logics.

B Switch-matrix Readout Circuits

The SM readout circuit has the same topology as in [9]. There are 4 SM readout banks, and each includes 64 readout channels and one 10-bit SAR ADC. Every readout channel has three amplification stages and can achieve a max gain of 76.4 dB, and the high-pass corner can be tuned from less than 1 Hz up to 80 Hz to allow measurements of both action potential (AP) and local-field potential (LFP). The SM routing in the array is controlled by the WL decoder and BL registers [10].

III Measurement results

A Electrical characterization

The DM-MEA has been fabricated using 0.18 μm CMOS technology, and the chip micrograph and packaged chip picture are shown in Figure 3. The area of the chip is 6.0 × 8.9 mm^2, consisting of an array of 1.8 × 3.5 mm^2.

The gain and noise characterization results for APS and SM readout circuits are shown in Fig. 4. The APS readout circuit achieves a noise level of 10.9 μV_{rms} for the AP band (300 Hz - 5 kHz), whereas for SM the noise level is 3.1 μV_{rms}. Concerning the power consumption, the APS readout circuits consume 5.9 μW per channel, while the SM readout consumes 39.1 μW per channel. The system specifications and characterization results have been summarized and compared to the state-of-the-art in Table I.

B Bio measurements

Fig. 5 shows spontaneous action potentials from an acute brain slice preparation. Parasagittal cerebellar slices (300 μm, 3-week old wild-type C57BL/6 mouse) were prepared as described in [12]. The signals were measured using SM and APS mode. The figure shows

the activity map recorded by using the APS readout, and examples of recorded traces from APS and SM readout showing clear spikes.

IV Conclusion

Based on results obtained from brain slices, we found that the DM-MEA yielded high-quality recordings of neuronal action potentials. The DM-MEA could be used in the future for network-related studies, for which data from a large neuronal network are required. Future directions could also include to study the action potentials along the entire axonal arbor, which may cover the entire neural culture, and to study different regions of a whole-mounted retina.

In summary, the DM-MEA can reliably and efficiently record neuronal potentials and offers the possibility of full-frame recording of the entire array with high SNR.

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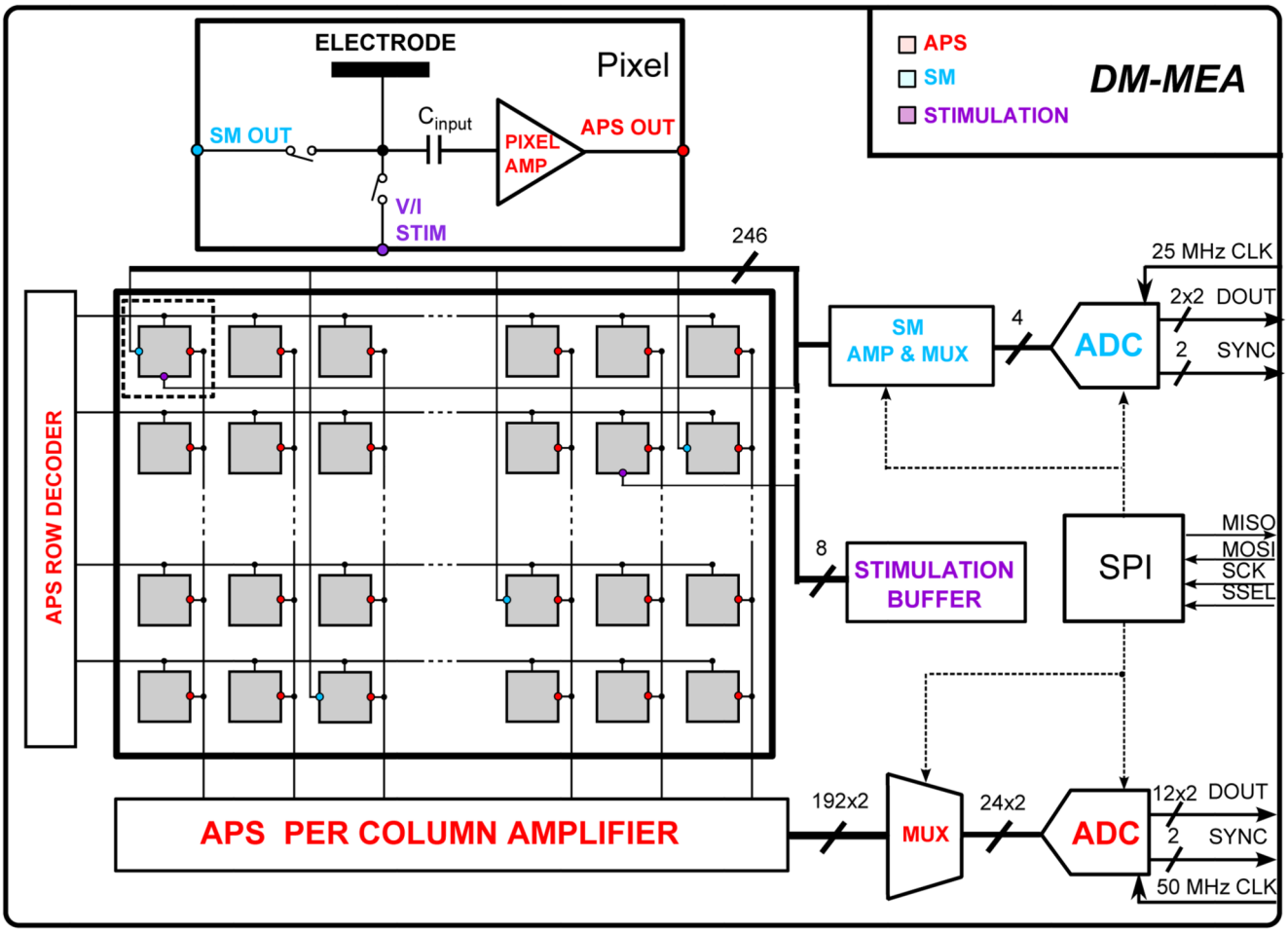

Fig. 1.

System diagram of the dual-mode HD-MEA, including electrode array, APS readouts, SM readouts and stimulation buffers.

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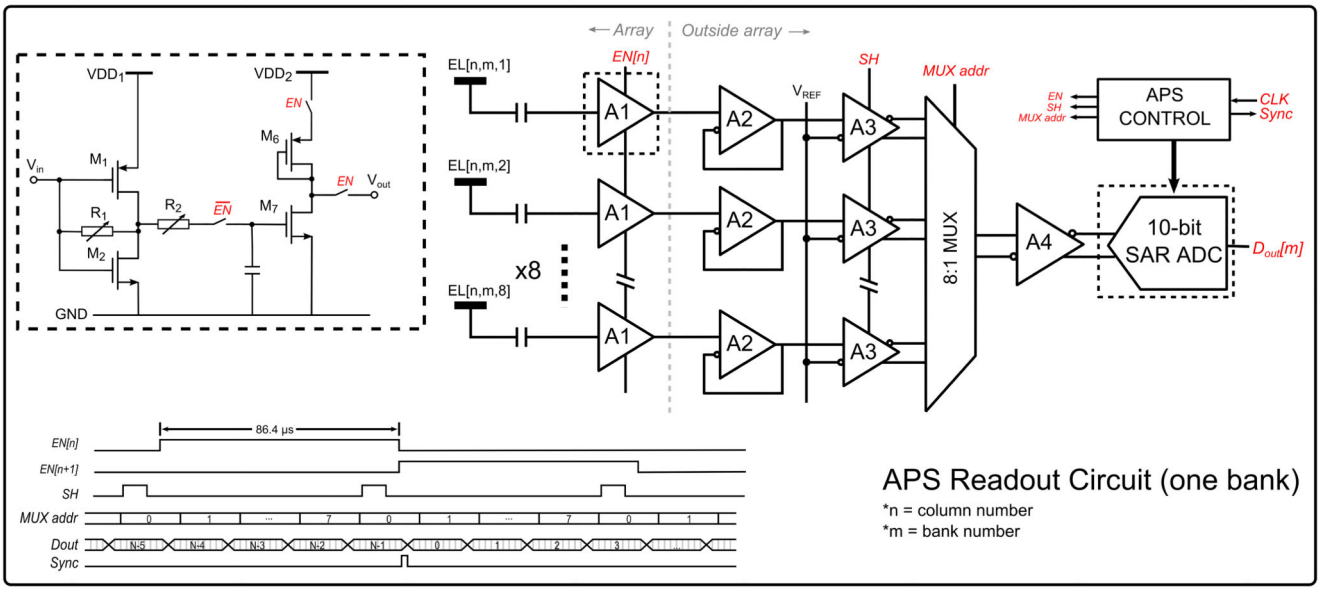

Fig. 2.

APS readout circuits including pixel amplifier, column readout circuits and timing information.

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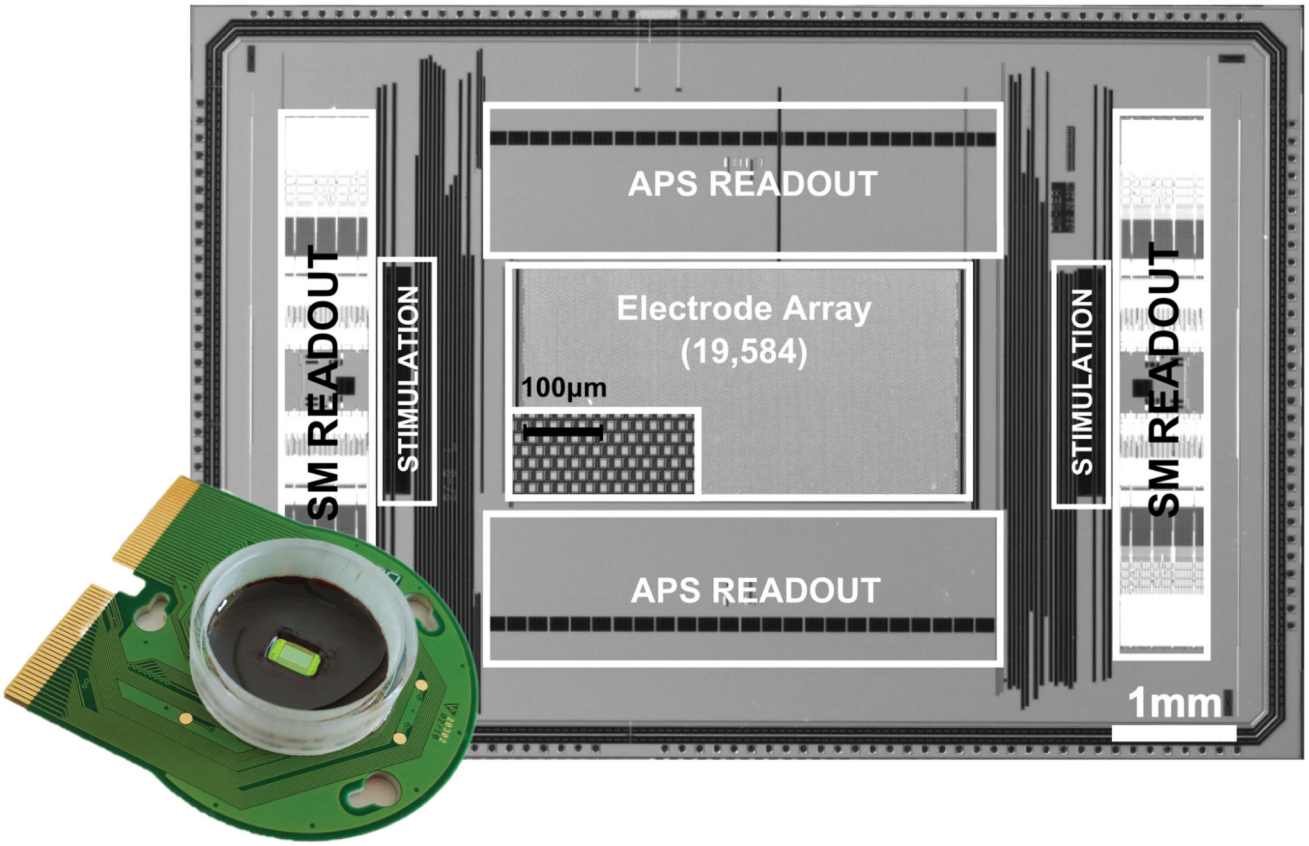

Fig. 3.
Chip micrograph and picture of the packaged chip.

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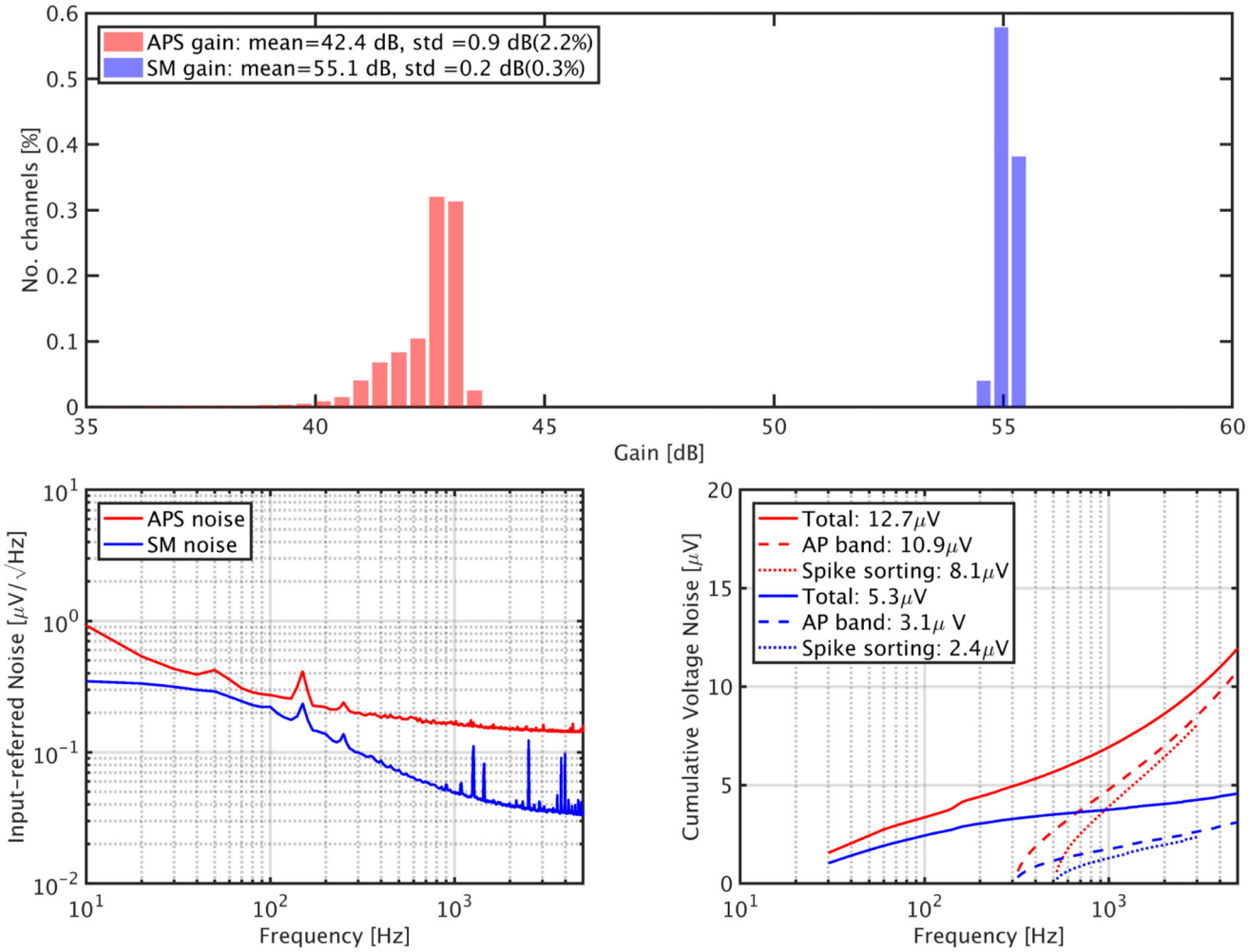

Fig. 4.

Gain and noise characterization results for APS and SM readout circuits.

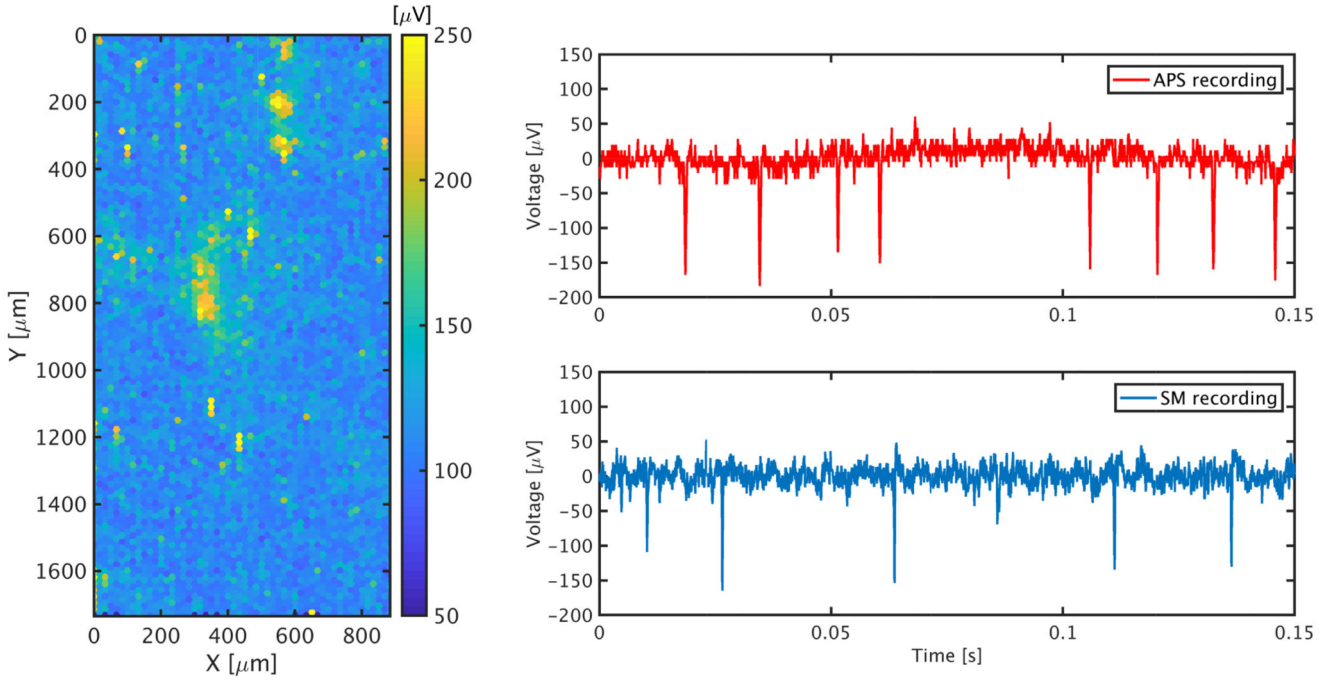

Fig. 5.

Bio measurement results using the DM-MEA. It shows the activity map recorded by using APS readout (left), and example spike traces from APS and SM readout (right).

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Table I

State-of-the-art comparison.

	[5]	[6]	[7]	[9]	This work	
Technology [nm]	140	180	180	180	180	
Readout structure	APS	APS	APS	SM	APS	SM
No. electrodes	27,684	4,225	512	59,760	19,584	
Pitch [μm]	24	16/32	25	13.5	18.0	
No. readout	6,912	4,225	512	2,048	19,584	246
Sampling rate [Hz]	12k	-	25k	20k	11.6k	24.4k
AP Noise [μV]	15.3	>44	-	2.4	10.9	3.1
Power/ch [μW]	-	-	3	16	5.9	39.1