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Study of Si Nanowires Produced by Metal-Assisted Chemical Etching as a Light-Trapping Material in n-type c-Si Solar Cells

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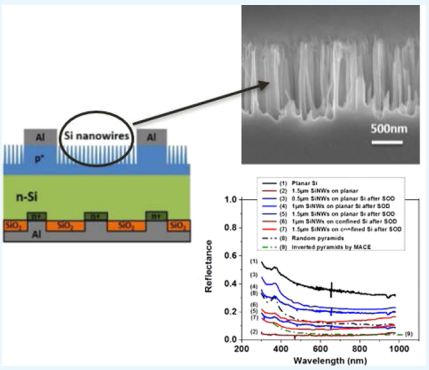
ABSTRACT: Si nanowires (SiNWs) produced by metal-assisted chemical etching on n-type Si were investigated for their use as a light-trapping material in c-Si solar cells. The nanowires were fabricated before junction formation (on a lightly doped Si substrate) so that their core was bulk and nonporous. The above fabrication process was implemented in solar cell fabrication. The SiNW reflectivity was tested at different steps of solar cell processing and found to be lower than that of conventional random pyramids used in c-Si solar cells. Contact formation on the front side of the cell was investigated by considering metal deposition either directly on the nanowires or on bulk areas in between the nanowire areas. The superiority of this second case was demonstrated. Three different Si nanowire lengths were investigated, namely, 0.5, 1, and 1.5 μm, the case of 1 μm giving better results in terms of solar cell characteristics and external quantum efficiency. The electronic quality of the Si nanowire surface was investigated using the corresponding metal-oxide-semiconductor capacitors with atomic-layer-deposited alumina dielectric. Successful reduction of surface recombination centers at the large Si nanowire surface was achieved by reducing structural defects at their surface through a specific chemical treatment. Finally, using the determined optimized conditions for Si nanowire formation, chemical cleaning, and process implementation in solar cell fabrication, we demonstrated ∼45% increase in solar cell efficiency with 1 μm SiNWs compared to that from a flat reference cell processed under similar conditions. The above study was made on test solar cells without surface passivation.



I. INTRODUCTION

High-performance c-Si solar cells require efficient light absorption within the absorber and efficient carrier collection of photoexcited carriers. Vertical silicon nanowires (SiNWs) on the Si surface can play a significant role in enhancing light trapping due to their strong broadband optical absorbance and antireflective properties in a broad range of incident angles.[1−3] There are different techniques to produce SiNW arrays on the Si surface, including lithography and etching,[4−8] vapor−liquid−solid growth,[9,10] and metal-assisted chemical etching (MACE).[11−17] MACE is a low-cost, fast, and easy method to produce Si nanowires on the c-Si surface with diameter in the 30−100 nm range. Their length, morphology, and structure depend on the etching time, the resistivity of the Si wafer, and the catalytic metal used in MACE.[18] On wafers with moderate resistivity (1−10 Ω cm), the nanowires are bulk, whereas on highly doped n- or p-type wafers, the resulting nanowires are porous.

The use of SiNWs by MACE in c-Si solar cells on p-type substrates has been studied by several groups,[19−24] including industrially processed solar cells with a cell size of 156 mm × 156 mm.[25] However, less work was devoted to SiNWs in c-Si solar cells on n-type substrates,[24] which gain increasing interest due to their demonstrated relative tolerance to common impurities like iron and oxygen and their immunity to boron−oxygen light-induced degradation reported in p-type crystalline Si solar cells.[26,27]

The low-reflectivity advantage of SiNWs by MACE as a light-trapping material in c-Si solar cells is counterbalanced by the increased surface recombination at the large Si nanowire surface.[1−3] The best method proposed so far to passivate the SiNW surface is by conformal atomic layer deposition (ALD) of alumina deposition.[3] However, further studies are needed to optimize the above passivation scheme.

In this work, we investigated the use of bulk Si nanowires by MACE as a light-trapping material on the front side of an n-type c-Si solar cell. SiNWs by MACE are bulk (nonporous) when they are formed on lightly doped Si. The same MACE process applied on highly doped Si results in porous Si nanowires. Consequently, for bulk SiNWs on the front side of c-Si solar cells, SiNW formation has to precede junction formation. This process sequence results in an emitter composed of the doped SiNWs and a doped continuous layer in bulk Si underneath the SiNWs. We studied the effect of SiNW length on solar cell characteristics by investigating three different lengths: 0.5, 1, and 1.5 μm. Reflectance spectra

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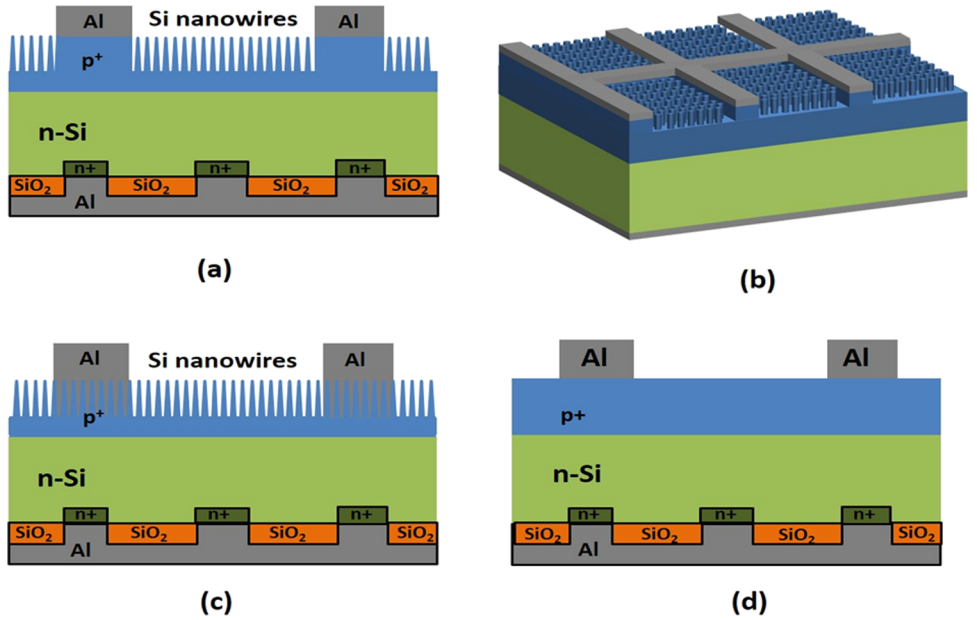

Figure 1. Schematic representation of a cross-sectional view of SiNW solar cell 3 described in the text in 2D (a) and 3D (b) representations. The schematics in (c) and (d) depict respectively the 2D representation of solar cell 2 and solar cell 1. In (c), the metal grid is directly on the SiNWs, whereas in (a), (b), and (d), the Al grid lies on bulk Si.

were recorded at different process steps of solar cell formation, and corresponding results will be discussed. Another challenge toward optimized solar cells with SiNWs at the front solar cell surface is the front metal contact. We investigated the use of an Al grid either deposited directly on the SiNWs or on bulk areas in between the SiNW areas. Finally, toward optimizing ALD alumina passivation of SiNWs, we investigated the use of a chemical treatment applied on the as-formed nanowires to remove structural defects from their surface and thus minimize interface states at the SiNW/ALD alumina interface. The electronic quality of the SiNW surface was tested by fabricating corresponding metal-oxide-semiconductor (MOS) test capacitors with ALD alumina dielectric and studying their electrical characteristics, from which the density of electronic states at the dielectric/SiNW surface was deduced.

II. EXPERIMENTAL RESULTS

The Si wafers used in this work were n-type single-face-polished, (100)-oriented Czochralski crystalline Si wafers with resistivity in the range of 1−2 Ω cm and thickness ∼400 μm.

II.I. SiNW Formation. SiNWs were fabricated using a single-step MACE process. Details on the process used are given in the experimental procedures, materials, and methods section. A two-step chemical cleaning was applied to remove structural defects from the SiNW surface, consisting of a sequence of piranha cleaning, followed by a dip in 2% per volume aqueous hydrogen fluoride (HF) solution at room temperature. Piranha cleaning is an oxidizing chemical process for Si, whereas the HF dip removes the formed oxide. By the subsequent use of the above, tiny structural defects at the SiNW surface are first surrounded by a silicon oxide during the piranha cleaning, whereas in the second step, these tiny defects are removed by liftoff, together with any other residues at the SiNW surface.

SiNWs with three different lengths, namely, 0.5, 1, and 1.5 μm, were fabricated and subjected to the above cleaning process. Corresponding solar cells were fabricated under the same experimental conditions.

II.II. Solar Cell Fabrication. Solar cells of a surface area of 1 cm^2 were fabricated on n-type Si wafers. Details of the process and materials used are given in the experimental procedures, materials, and methods section. Three different solar cell architectures were fabricated:

(a) Solar cell 1: reference cell without SiNWs.
(b) Solar cell 2: grid on SiNWs. In this cell, SiNWs were formed everywhere on the front solar cell surface area and the Al metal grid was in direct contact with the nanowires.
(c) Solar cell 3: grid on bulk Si. In this cell, SiNWs were formed on confined areas of 200 μm × 200 μm separated by a tetragonal mesh of bulk Si areas covered with the Al metal mesh of the gate.

The p^+ emitter was formed using spin-on doping (SOD), providing boron dopants. In the case of the SiNW solar cells 2 and 3, the p^+ emitter was formed after SiNW formation. The Al metal grid in all cases was covering a gate surface area of ∼15% of the total (same in all cells). In solar cell 3, the metal gate was aligned on the bulk Si areas and partly on SiNWs around the bulk, whereas in solar cell 2, the Al grid was in direct contact with the SiNWs. A back ohmic contact was formed on the backside of the wafer, its formation being implemented in the process flow in the corresponding order. A patterned SiO_2 layer was used as a passivation/reflector layer. Figure 1a,b shows a cross-sectional view in two-dimensional (2D) (a) and three-dimensional (3D) (b) representations of solar cell 3, whereas (c) and (d) show a 2D representation of solar cells 2 and 1, respectively. In all cases, the back ohmic contact was composed of Al on highly doped n^+ areas within SiO_2 windows, as depicted in Figure 1.

II.III. SiNW Structural and Morphological Characteristics. SiNWs by MACE fabricated under the conditions described above had a diameter in the range of 50−70 nm and interdistance in the range of 50−100 nm and were vertical to

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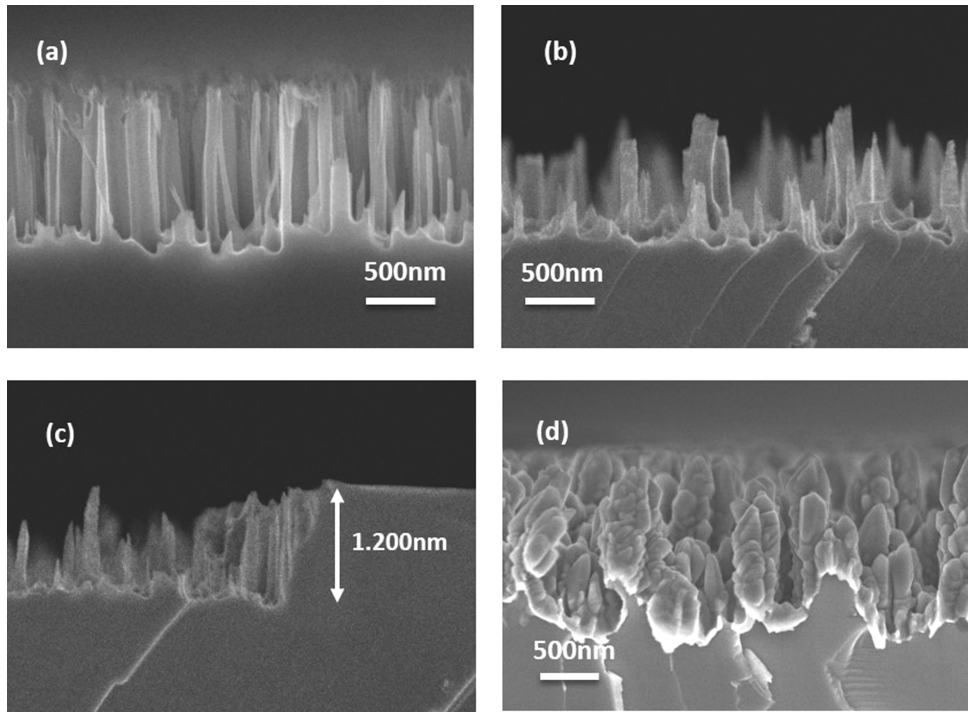

Figure 2. Cross-sectional SEM images of as-formed SiNWs (a), SiNWs in confined areas after the SOD process (b, c), and after Al deposition on SOD-processed nanowires (d).

the Si surface. Corresponding scanning electron microscopy (SEM) images are depicted in Figure 2. In confined areas (solar cell 3), the SiNW length was slightly higher than that on large surface areas (solar cell 2). This effect (etch rate higher in confined areas) was studied in detail in ref 14. Figure 2a shows an example of the cross-sectional SEM image of as-formed SiNWs by MACE, whereas Figure 2b,c depicts SiNWs imaged after the SOD process and showing some damage by this process, attributed to stress effects during the thermal cycle. Figure 2d shows the SiNWs in (b) after Al deposition. Conformal coverage of the SiNW surface is clearly seen, with Al crystals growing on the top of SiNWs after their full coverage, forming Al nanowires of increasing diameter and length with increasing deposition time. As mentioned above and illustrated in Figure 1, in solar cell 3, the Al grid was in direct contact with the patterned bulk crystalline Si areas, slightly exceeding those surface areas so as to partially cover SiNWs. In solar cell 2, the Al grid was directly deposited on the SiNW surface and had the same surface area as in solar cells 1 and 3. SOD was deposited after SiNW formation; however, after annealing, a p−n junction was formed underneath the SiNWs. Both the SiNWs and a c-Si layer underneath them were doped with boron. The presence of SiNWs during SOD resulted in a slightly shallower junction depth than in the reference solar cell without SiNWs. In the case of solar cell 3, bulk areas underneath the Al grid were also doped by SOD.

II.IV. Reflectivity Measurements. Reflectivity measurements were performed on samples with SiNWs at different stages of processing. The corresponding reflectance spectra are depicted in Figure 3 (spectra (1)−(8)) as follows: (1) n-type bulk crystalline Si (no SiNWs), (2) as-formed SiNWs on a planar Si surface area, ((3)−(5)) SiNWs of lengths 0.5, 1, and 1.5 μm, respectively, on a planar Si surface area after SOD processing, ((6) and (7)) similar reflectance spectra as in (4) and (5) but for SiNWs formed on confined areas. For

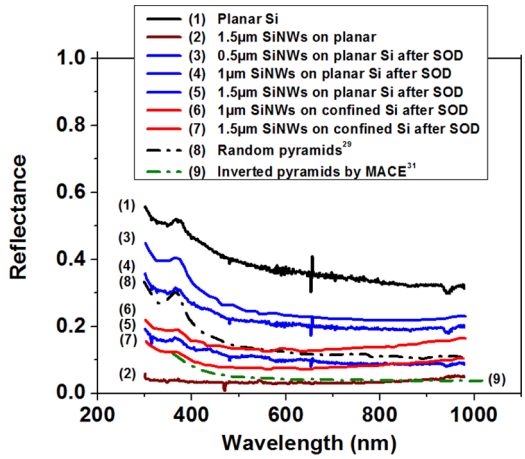

Figure 3. Reflectance spectra from five different samples as follows: (1) flat reference Si surface, (2) Si surface with as-grown 1 μm SiNWs everywhere, (3)−(5) as-grown SiNWs of lengths 0.5, 1, and 1.5 μm on a planar surface after the SOD process, and (6) and (7) 1 and 1.5 μm SiNWs on confined areas after SOD. For comparison, we show in (8) the reflectance spectrum from the literature (ref 29) for a Si surface with random pyramids without surface passivation, used in conventional c-Si solar cells. (9) Spectrum from inverted pyramids formed by MACE.[31]

comparison, spectrum (8) is the reflectance spectrum, from the literature,[28] of a Si surface with random pyramids used as an antireflective material in conventional c-Si solar cells. From Figure 3, we deduce that the reflectivity of our SiNWs is significantly lower than that of bulk crystalline Si and it decreases with the increasing SiNW length from 0.5 to 1.5 μm (see spectra (3)−(5)). If we now compare sample (3) with (6) and (4) with (7) with the only difference that in (3) and (4) the SiNWs were everywhere on the surface, whereas in (6) and (7), they were only in confined areas, we see that the

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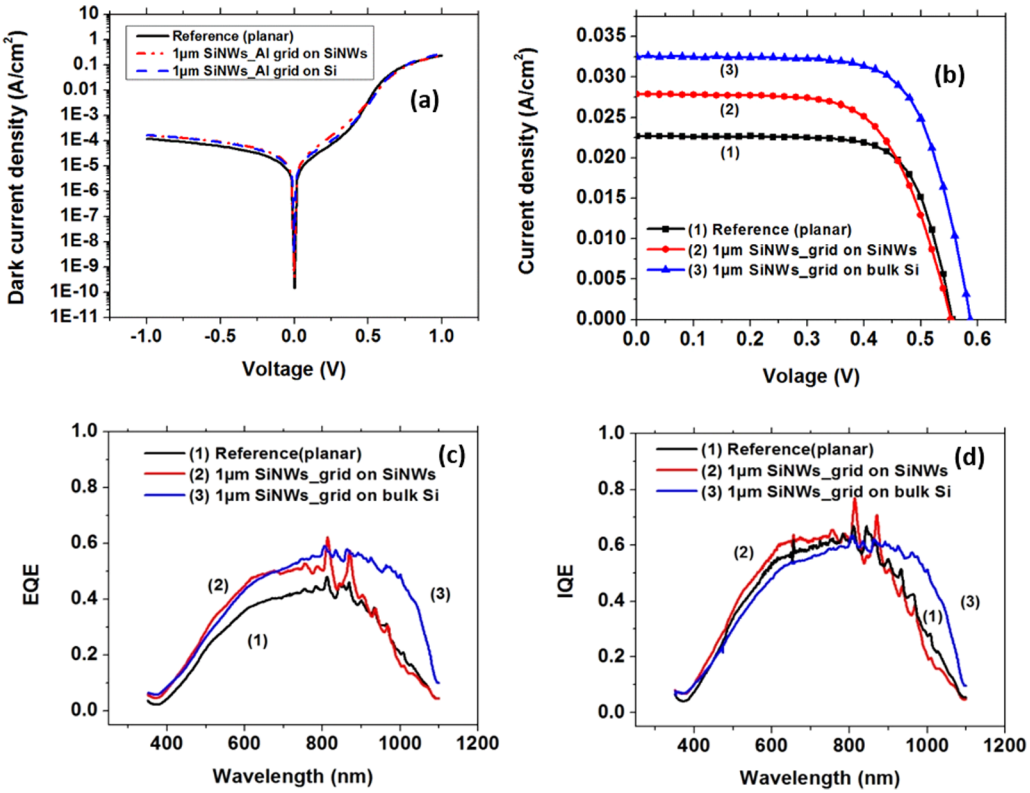

Figure 4. (a) Dark current density−voltage characteristics of the three different devices studied in this work (black curves: solar cell 1, reference cell; red curves: solar cell 2 with grid on SiNWs; blue curves: solar cell 3 with SiNWs and grid on bulk). (b) Photoelectric characteristics (current density−voltage) of the above three devices, (c, d) external (EQE) and internal (IQE) quantum efficiencies versus wavelength of the three different devices studied in this work.

reflectance spectra are significantly lower in the case of SiNWs in confined areas compared to those in the case of SiNWs on large Si areas, despite the fact that in the case of confined areas 15% of surface coverage is bulk Si. This is attributed to two different effects: (a) As stated above, we have observed that under the same experimental conditions SiNWs in confined areas are less damaged by the SOD process compared with SiNWs on a large Si area and (b) SiNWs in confined areas are slightly longer compared with SiNWs in nonconfined areas.[14] These two effects are at the origin of the observed differences in reflectivity. If we now compare the reflectance spectra of SiNWs with the spectrum of a nanostructured surface with random inverted pyramids used in conventional c-Si solar cells (green dotted line 9),[28] we see that the reflectance spectrum of SiNWs before SOD (spectrum (2)) and also the reflectance spectra of 1 and 1.5 μm SiNWs in confined areas even after SOD ((6) and (7)) are all below the reflectance spectrum of inverted pyramids. This is an interesting result toward improving Si solar cells by replacing the inverted pyramids with SiNWs. We have chosen the reflectance spectrum of ref 28 because this spectrum is directly comparable with the corresponding reflectance spectra of this work since there is no additional passivation/antireflection coating on the inverted pyramids, as is the case in most of the related papers in the literature. In optimized c-Si solar cells, the random pyramids are coated with a double-[29] or multilayer dielectric stack[30] with both passivation and antireflection properties, exhibiting reflectivity below 5% in the whole optical spectrum. It is thus important to note that a similar result is achieved using SiNWs without any antireflective coating on them. Furthermore, our reflectance spectrum of 1 μm SiNWs on a planar surface (curve (2) of Figure 3) is comparable with that of inverted pyramids obtained by MACE in ref 31 (reflectance also below 5%). However, in that second case, the shown SEM images depicted an additional rough porous Si layer on the surface of the inverted pyramids, which is expected to be fully detrimental for the solar cell efficiency, introducing important surface recombination due to an increased number of surface states. No results on fabricated solar cells were presented in that ref 31 to verify the above statement.

II.V. Electrical and Photoelectric Measurements of Solar Cells. The electrical and photoelectric characteristics of the three different devices studied in this work (solar cell 1 (reference), solar cell 2 (1 μm SiNWs, grid on SiNWs), and solar cell 3 (1 μm SiNWs, grid on bulk)) are depicted in Figure 4a−d. Figure 4a depicts the dark current density versus voltage curve for the above three cases, whereas (b) shows the photocurrent density versus voltage curve. The external and internal quantum efficiencies (EQE and IQE, respectively) versus wavelength are depicted in (c) and (d), respectively, for all three devices. IQE was calculated from EQE by taking into account the reflectance spectra of Figure 4; thus, their differences reflect the antireflective properties of the SiNWs. Short circuit current (J_{sc}) and open circuit voltage (V_{oc}) were determined from Figure 4b.

The electrical parameters of the solar cells in the dark (saturation current I_s, series resistance R_s, and ideality factor n of the diode) were calculated using the single-diode model, with the current−voltage (I−V) characteristics described by

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Table 1. Electrical and Photoelectric Parameters of the Three Different Solar Cells Studied in This Article[a]

device	J_s (A/cm^2)	n	R_s (Ω cm^2)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	PVE (%)
solar cell 1: reference cell, no SiNWs	1.16×10^{-4}	1.43	1.3	22.7	0.556	72.7	9.2
solar cell 2 (SiNW cell with grid on SiNWs)	1.62×10^{-4}	1.56	2.0	27.9	0.553	65.2	10.1
solar cell 3 (SiNW cell with grid on bulk)	1.61×10^{-4}	1.67	1.5	32.5	0.587	70.3	13.4

[a]The SiNW length for solar cells 2 and 3 was 1 μm.

$$I = I_s\left\{\exp\left[\frac{(V - IR_s)}{nKT}\right] - 1\right\}$$

where I_s is the saturation current, R_s is the series resistance, n is the ideality factor of the diode, K is the Boltzmann constant, and T is the absolute temperature. R_s was calculated from

$$\frac{dV}{d\ln I} = n\frac{kT}{q} + IR_s$$

The saturation current, I_s, was calculated by fitting the $I-V$ characteristics using the equation of the diode corrected to the series resistance.

Table 1 summarizes the electrical and photoelectric parameters of the three different solar cells studied in this work, including the saturation current density (J_s; I_s normalized to the solar cell surface area), the series resistance (R_s), the diode ideality factor (n), the short circuit current density (J_{sc}), open circuit voltage (V_{oc}), fill factor (FF), and photovoltaic efficiency (PVE). Table 2 shows a comparison of the photoelectric parameters of three SiNW solar cells with grid on bulk and different SiNW lengths.

Table 2. Electrical and Photoelectric Parameters of SiNW Solar Cells of Structure 3 with Grid on Bulk

device	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	PVE (%)
0.5 μm SiNWs	24.1	0.559	72.7	9.8
1 μm SiNWs	32.5	0.587	70.3	13.4
1.5 μm SiNWs	29.6	0.547	68.9	11.1

In Table 1, it is seen that the saturation current density, J_s, and the ideality factor, n, are quite similar for all three devices, being slightly lower in the case of the reference solar cell, as expected. The increased saturation current and thus the increased ideality factor above 1, which is the value of the ideal or Shockley diode, are attributed to carrier recombination in the emitter formed by SOD on the already existing SiNWs. In the case of the SiNW cells, the emitter is extended both in the core of the SiNWs and in a layer underneath them. It is thus expected that the roughness and structural defects at the SiNW surface affect the above carrier recombination. The fact that the obtained values for the SiNW cells and the reference cell are quite similar suggests that defects at the SiNW surface are minimized by the process used for their smoothing. The increased ideality factor reduces the fill factor, FF, of the cells; it could thus partly explain the better FF in the case of the reference cell.

The short circuit current (J_{sc}; see Figure 4b and Table 1) is much higher in the SiNW solar cells compared to that in the reference cell, the best case being that of the SiNWs in confined areas and grid on bulk. The factors that are expected to influence J_{sc} are the efficiency of light absorption in the cell, the defect-driven space charge recombination in the emitter as discussed above, and the existence of a high series resistance. Concerning the series resistance, the general comment in our study is that in all cases of our devices (see Table 1) R_s was relatively small; thus, it is not expected to seriously affect J_{sc}. The smallest R_s was obtained in the case of the reference cell, as expected. SiNWs introduce higher series resistance mainly resulting from their rough surface. It is thus understood why this is the highest in the case of SiNWs with the grid directly on the nanowires, partly explaining the smaller J_{sc} compared to that of the cell with SiNWs with grid on bulk. The main factor influencing the observed differences in J_{sc} is the antireflection properties of the SiNW solar cells. From Figure 3, we deduce that surface reflectivity on confined areas with the grid on bulk (spectrum 6) is lower than that of SiNWs everywhere on the Si surface and Al grid directly on the nanowires (spectrum 4). This may be attributed to differences in the damage produced by the SOD process (including an annealing step) when the SiNWs were everywhere on the Si surface area compared to the case of SiNWs in confined areas. This was confirmed by corresponding SEM images (not shown here).

Concerning the shunt resistance of our solar cells, the measured values were in the MΩ cm^2 range, being quite similar in all cases of the measured devices. Its effect on the open circuit voltage is thus expected to be negligible.

The external quantum efficiency, EQE, is much better in SiNW cells 2 and 3 compared to that in the reference cell in the optical region of the spectrum, attributed to the better antireflective properties of the SiNWs in the above cells. Furthermore, solar cell 3 shows better EQE and IQE than the other two solar cells in the red and IR regions of the spectrum. This could result from reduced recombination in the Si bulk in this specific cell; however, this cannot be the case since the substrate is the same for all studied devices. We could thus suggest that this is an effect of this specific cell architecture and its back contact, resulting in better light trapping of the red and IR light in the cell.

If we compare the open circuit voltage, V_{oc}, of the different cells of Tables 1 and 2, we see that the reference cell and the 0.5 μm SiNW cell have roughly similar V_{oc}. Between 0.5 and 1.5 μm SiNWs, V_{oc} is worse in the second case. The case of SiNWs everywhere on the solar cell surface and grid on them is slightly worse than the reference cell. The above differences could be attributed to increased surface recombination in the presence of SiNWs, increasing with the increase of the SiNW length; however, this is consistent only with the observed behavior of the 0.5 and 1.5 μm SiNW solar cells but not for the 1 μm SiNW solar cell with grid on bulk. The V_{oc} in this case is the highest compared with all other cases; however, the high V_{oc} is not consistent with an expected decreased saturation current and ideality factor of the diode (see Table 1). This point needs to be further elucidated.

Concerning the fill factor, FF, the best case was that of the reference cell compared to the other two cases. This is attributed partly to differences in the series resistance, which was lower in the case of the reference cell compared to that in the other two cases and lower in solar cell 3 compared to that

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in solar cell 2. When R_s decreases, FF increases. However, the most important parameter influencing the fill factor of our solar cells is the ideality factor, n, of the cell. When the ideality factor increases, FF decreases. In Table 1, it is clearly seen that changes in n are accordingly reflected to FF. Differences in the ideality factor may result from differences in the doping concentration of the emitter. In our SiNW solar cells, it is expected that the junction is mainly formed underneath the SiNWs, forming a continuous doped layer. The SiNWs themselves are also expected to be doped since their diameter is quite large, approximately 70 nm, and confinement effects making doping difficult are not expected to be present. Differences in the doping concentration of the emitter lead to differences in the width of the space charge region falling in the emitter. An increase in the doping concentration of the emitter can thus reduce space charge recombination and consequently the ideality factor, this being reflected to the fill factor.

A comparison was also made between solar cells with SiNWs of three different lengths, namely 0.5, 1, and 1.5 μm, and grid on bulk. The results are summarized in Table 2. The best performance was achieved with the 1 μm SiNWs. Compared to that in the case of the 0.5 μm SiNWs, the better performance of the 1 μm SiNW solar cell is mainly attributed to the higher reflectance of the 1 μm SiNWs compared to that of the 0.5 μm ones. The worse performance was achieved with the 1.5 μm SiNWs, in spite of the fact that these finally showed lower reflectance than that from the 1 μm SiNWs. This is attributed to an increased density of surface states in SiNWs fabricated by MACE when their length exceeds 1 μm.[32] Indeed, in this last case, the top part of the length of the SiNWs becomes porous, as demonstrated in ref 32. Thus, surface roughness and structural defects are introduced, which result in not only better light absorption (thus lower reflectivity) but also an increase of carrier recombination at the SiNW surface. The presence of these defects affects all three parameters of the cell, as explained above.

Overall, a 13.4% efficiency was obtained with our solar cell 3 without using any passivation layer on the solar cell surface. The above result was not optimized since the aim of this study was not solar cell optimization but the understanding of the effect on the different solar cell parameters of the use of SiNWs as antireflective material on the front solar cell surface.

II.VI. ALD Alumina/SiNW Interface Characterization by *C*−*V* Measurements on Test Metal-Oxide-Semiconductor (MOS) Capacitors. Structural defects at the SiNW surface induce surface states, which are a significant source of surface recombination of the solar cell. To test the effectiveness of the applied chemical treatment to reduce structural defects, we fabricated test capacitors and use them as test devices for the characterization of the electronic quality of the SiNW surface. The capacitors were metal-oxide-semiconductor (MOS) devices including the SiNWs on the gate, whereas atomic-layer-deposited (ALD) aluminum oxide (Al_2O_3) was used as the capacitor dielectric.[32] A schematic representation of a cross-sectional view of the test capacitor is depicted in Figure 5a.

To reduce structural defects or the presence of contaminants on the Si nanowire surface, we used a chemical treatment with a first step of piranha (mixture of H_2SO_4 and H_2O_2) cleaning, followed by an HF dip. This process was found to significantly reduce structural defects at the SiNW surface, thus reducing both the series resistance and the density of interface states at the Al_2O_3/SiNW interface.[32] Indeed, piranha cleaning oxidizes

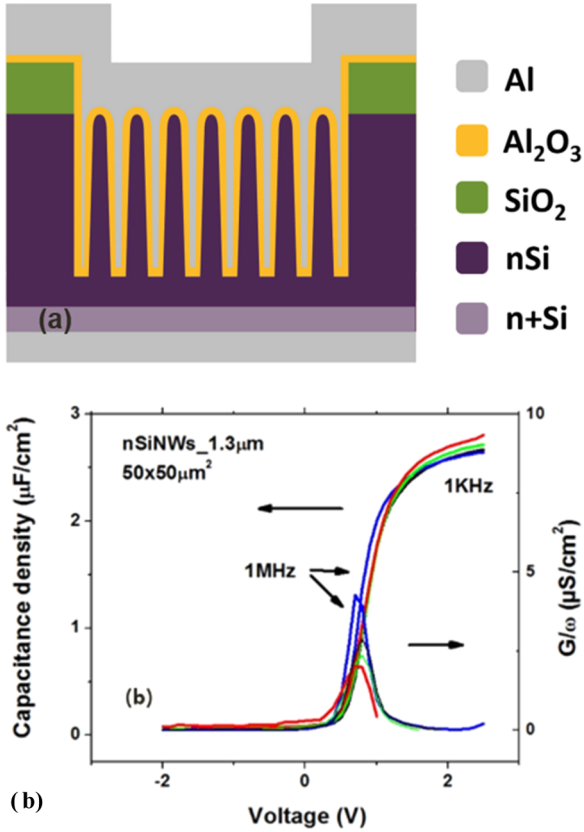

Figure 5. (a) Schematic representation of a SiNW test capacitor on n-type Si with ALD alumina dielectric. (b) $C-V$ and G/ω vs voltage characteristics (blue line, 1 MHz; red line, 1 kHz) of the SiNW capacitor on n-type Si. SiNWs were subjected to two cycles of piranha/HF chemical cleaning. There is almost no frequency dispersion at accumulation, indicative of the reduced series resistance. From the G/ω peak at depletion, the density of interface states can be calculated. The peak at 1 MHz (blue line) is higher than that at 1 kHz (red line), suggesting that fast responding traps are predominant.

the SiNW surface, whereas the HF dip removes the formed silicon oxide. At the same time, surface structural defects are partially removed, thus smoothing the SiNW surface. We investigated the electronic quality of the Si nanowire surface on n-type Si by characterizing the MIS capacitor of Figure 5a using capacitance−voltage ($C-V$) and conductance−voltage ($G/\omega-V$, where ω is the circular frequency) measurements in the frequency range 1 kHz to 1 MHz. Typical results are shown in Figure 5b, depicting $C-V$ characteristics on the left axis and the corresponding $G/\omega-$V characteristics on the right axis (blue line, 1 MHz; red line, 1 kHz). Detailed results are given in ref 32. From the curves of Figure 5, one can deduce that after the chemical treatment a high-quality alumina/SiNW interface is achieved. There is very limited frequency dispersion at accumulation in the studied frequency range, and only a small frequency dispersion is observed at depletion, attributed to charging of the structure after the first voltage sweep. The G/ω versus voltage curve (see the right axis of Figure 5b) shows a peak at depletion, attributed to interface states at the alumina/SiNW interface. The intensity of the peak at depletion is higher at 1 MHz than at 1 kHz, which implies that the corresponding interface states are fast. The density of interface states D_{it} was determined using the conductance method and was found to be 1.05×10^{13} cm^{-2} eV^{-2} for the capacitor with the as-grown SiNWs and 7×10^{11} cm^{-2} eV^{-2} in

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the case of the MOS capacitor with SiNWs after the applied chemical cleaning. This second value of D_{it} is quite low for the alumina dielectric, indicative of a good electronic quality of the SiNW surface after the applied chemical cleaning. This is attributed to the corresponding smoothing of the SiNW surface and removal of the tiny structural defects from their surface.[33]

III. DISCUSSION

We demonstrated that the use of SiNWs by MACE on the front Si surface of a c-Si solar cell on n-type Si can substantially improve the solar cell efficiency compared to that of a cell without nanowires. One restriction is that the SiNWs by MACE should be formed before junction formation (on moderately doped areas) to have bulk crystalline and not porous structure. This is because it is well known that SiNWs by MACE formed on highly doped areas (in this case, the solar cell emitter) are porous.[16] Furthermore, we have demonstrated (results to be published elsewhere) that junction formation by SOD applied after SiNW formation results in an almost planar junction on c-Si underneath the SiNWs. In this specific case, the main function of SiNWs is to act as an antireflective material to improve light absorption by the solar cell. The reflectance spectrum of as-formed SiNWs with length above 1 μm is far below that of the conventionally nanostructured surface with inverted pyramids (below 4% in the whole spectrum compared to above 10% in high wavelengths and above 20% in low wavelengths in the case of conventional inverted pyramids (see Figure 4)). The 1 μm SiNWs after the SOD process showed reflectance on the order of 8−12%, always below that of conventional inverted pyramids without surface passivation. An improvement of the above is expected if the SOD process is improved so as to avoid SiNW damage (for example by rapid thermal instead of furnace annealing).

When comparing the reflectance spectra of solar cell 2 and solar cell 3 after the SOD process (see curve 4 compared to curve 6 in Figure 3), we can clearly see that curve 6 is much below curve 4. This is attributed to the better mechanical stability of the SiNWs when they are formed in confined areas between the metal grids compared to that of the SiNWs formed everywhere on the solar cell surface. SiNWs are less damaged by the annealing process following SOD when they are confined in smaller areas. The differences in reflectance spectra are mainly at the origin of the differences in the photocurrent density and EQE in the above two cases.

Another factor to consider when comparing the reference cell without SiNWs with the two SiNW solar cells described above is the junction depth using SOD. We found that the junction depth was slightly smaller in the case of the SiNW cells compared to that in the reference cell. We studied the junction depth by introducing a novel method of junction cross section imaging based on the different contrast of MACE SiNWs formed on highly doped areas (porous SiNWs) compared to that of SiNWs on lightly doped Si (having bulk crystalline structure). This method is the subject of another paper submitted for publication. The junction depth of our cells was found to be 1.3 μm in the case of the planar junction compared to 1.1 μm in the presence of SiNWs of 1 μm.

The presence of SiNWs on the front solar cell surface (3D nanostructuring of the surface) introduces a difficulty in the metallization scheme to be used. The solution is the solar cell architecture with the grid on bulk Si and the SiNWs in confined areas within the grid openings, as the architecture used in solar cell 3.

Finally, using an n-type c-Si substrate for our solar cells in combination with SiNWs by MACE, we demonstrated high electronic quality of the SiNW/ALD alumina interface, better than that of the corresponding interface in the case of the p-type Si substrate studied in ref 28. The structural defects on the SiNW surface on n-type Si were more effectively removed by chemical cleaning than in the case of SiNWs on p-type Si.[28] No bulk traps were observed in the case of n-type Si, as demonstrated in this paper. This result is very promising toward incorporating ALD alumina as a passivation layer on SiNWs by MACE in c-Si solar cells on an n-type Si substrate.

IV. CONCLUSIONS

SiNWs by MACE with bulk structure on n-type Si were investigated for their use as a light-trapping material in c-Si solar cells. Their reflectivity at different stages of solar cell processing (e.g., emitter formation by SOD) was investigated and found to be lower than that of conventional random pyramids mainly used in c-Si solar cells. Front contact formation either directly on the SiNWs or on bulk areas in between SiNW areas was also investigated. We found that the above second case resulted in better solar cell characteristics of the cell. Three different SiNW lengths were investigated, namely, 0.5, 1, and 1.5 μm. The case of 1 μm SiNWs gave better results in terms of solar cell characteristics and external quantum efficiency. We also showed that the SOD process causes some damage of the SiNWs, which is reduced by fabricating them in confined areas within a grid of bulk Si areas. These bulk areas are also used as contact areas on which the Al grid is deposited. Solar cells with SiNWs of 1 μm were compared with reference flat area solar cells. A 45% increase in efficiency was measured with the use of SiNWs. Finally, we applied a chemical treatment to remove structural defects from the SiNW surface, which resulted in improving the electronic quality of the ALD alumina/SiNW interface. In a future work, the obtained results will be used to fabricate optimized c-Si solar cells on an n-type substrate with ALD-passivated SiNWs on their front surface.

V. EXPERIMENTAL PROCEDURES, MATERIALS, AND METHODS

V.I. Substrates. In this work, n-type single-face-polished, (100)-oriented Czochralski crystalline Si wafers were used with resistivity in the range of 1−2 Ω cm and thickness ∼400 μm.

V.II. Formation of SiNWs by MACE. SiNWs were fabricated using a single-step MACE process. The etching solution was composed of 4.8 M HF (50%) and 0.02 M $AgNO_3$, and the process temperature was 30 °C. After SiNW formation, the Ag dendrites formed on the SiNW surface, as well as Ag residues within the nanowires, were removed by dipping the samples in HNO_3 (50%) for a short time. A two-step chemical cleaning was then applied to remove structural defects from the SiNW surface, consisting of a sequence of piranha cleaning in 1:1 v/v H_2O_2/H_2SO_4 solution for 30 min followed by a dip in 2% per volume aqueous HF solution at room temperature for 1 min. Piranha cleaning is an oxidizing chemical process for Si, whereas the HF dip removes the formed oxide, resulting in liftoff of tiny nanostructures and other residues from the Si surface. SiNWs with three different lengths, namely, 0.5, 1, or 1.5 μm, were fabricated.

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V.III. Metal Deposition on SiNWs. Al deposited by electron gun evaporation was used as the metallization material. A Denton e-gun evaporator was used in this respect, and the base pressure in the system was $\sim 10^{-6}$ Torr. The deposited equivalent thickness on a flat surface was 300 μm. Confocal coverage of the SiNW surface was observed, as depicted in Figure 2d. The Al layer was patterned using optical lithography and chemical etching.

V.IV. Solar Cell Fabrication. Solar cells of a surface area of 1 cm^2 were fabricated on n-type Si wafers. Three different solar cell architectures were used: solar cell 1 was a reference cell, solar cell 2 was a solar cell with SiNWs everywhere on the front solar cell surface area and an Al metal grid in direct contact with the nanowires, and solar cell 3 had SiNWs on confined areas of 200 μm × 200 μm separated by a tetragonal bulk Si area covered with the Al metal grid as front electrode metal. The p^+ emitter was formed after SiNW formation by spin-on doping (SOD). The SOD material used was B154 of Filtronics, providing boron dopants. Spinning of the SOD material was followed by high-temperature annealing at 1050 °C for 30 min. The remaining conductive layer on the Si surface after the above process was chemically removed by dipping the samples in buffered hydrofluoric acid. The Al metal grid coverage of the device surface area was ∼15% of the total in all cases. In solar cell 3, the metal grid was aligned on the bulk Si areas, fully covering them and partly exceeding on the SiNW surface area around the bulk. An Al back ohmic contact was formed on the backside of the wafer at the beginning of the process. The process flow was carefully designed so as to use compatible process steps in the correct order. A spin-coated resist subsequently removed was used when needed to protect the already formed areas.

V.V. Test Capacitor Fabrication. MOS capacitors used as test structures for characterizing the electronic quality of the ALD alumina/SiNW interface were fabricated with the following process steps: A 500 nm thick silicon field oxide (thermal SiO_2) was formed on the Si wafer and patterned to define the capacitor area. Si nanowires were formed in the SiO_2 windows using MACE through a resist mask protecting the SiO_2. The two-step chemical cleaning was then applied to the samples, and a 10 nm thick alumina (Al_2O_3) layer by ALD was deposited on top of the SiNWs. The last step was Al gate metal deposition, followed by patterning using lithography and etching to define the gate area. An ohmic contact was formed on the backside of the wafer, implemented in the above process steps. The last step was furnace annealing in forming gas (mixture of H_2/N_2), performed at 430 °C for 30 min.

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The authors declare no competing financial interest.

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