HHS Public Access

Author manuscript

IEEE J Solid-State Circuits. Author manuscript; available in PMC 2020 October 01.

Published in final edited form as:

IEEE J Solid-State Circuits. 2019 October ; 54(10): 2867–2878. doi:10.1109/JSSC.2019.2930911.

Integrated Cold-Start of a Boost Converter at 57mV using Cross-Coupled Complementary Charge Pumps and Ultra-Low-Voltage Ring Oscillator

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Abstract

This paper demonstrates an on-chip electrical cold-start technique to achieve low-voltage and fast start up of a boost converter for autonomous thermal energy harvesting from human body heat. An improved charge transfer through high gate-boosted switches by means of cross-coupled complementary charge pumps enables voltage multiplication of the low input voltage during cold start. The start-up voltage multiplier operates with an on-chip clock generated by an ultra-low-voltage ring oscillator. The proposed cold-start scheme implemented in a general purpose 0.18μm CMOS process assists an inductive boost converter to start operation with a minimum input voltage of 57mV in 135 ms while consuming only 90 nJ of energy from the harvesting source, without using additional sources of energy or additional off-chip components.

Keywords

Thermoelectric energy harvesting; DC-DC converter; integrated cold-start; charge pump; ring oscillator

I. Introduction

THERMAL energy from human body heat is a ubiquitous source of energy, and unlike solar power, it can be harnessed irrespective of illumination conditions. As such, body heat is an ideal energy source for self-powered wearable devices [1]. Thermal energy can be converted to electrical energy using thermoelectric generators (TEG), solid-state devices that generate voltage from an applied temperature gradient (ΔT) using the Seebeck effect [2]. A wearable form factor requires small-area TEGs, which generate only tens of millivolts from the small ΔT (~ 1-2°C) between skin and the ambient environment. A DC-DC step-up converter is needed to boost this small voltage to power electronics. While low-voltage DC-DC converters have been demonstrated, initial start-up of the power converter at low input voltage is challenging without using additional energy sources such as batteries [3], mechanical vibrations [4], or RF sources [5].

Over the past decade, research efforts focused on low-voltage electrical cold-start of thermoelectric energy harvesters have demonstrated fully battery-less operation. Transformers are used in [6] and [7] to kick-start the boost converter at 21mV and 40mV,

respectively. Inductor-based LC oscillators [8] or Colpitts oscillators [9] have also demonstrated start-up from 50mV and 40mV input voltages. All these approaches accomplished low-voltage cold-start but require additional off-chip magnetic components that limit device miniaturization.

Fully-integrated electrical cold start at low input voltage is challenging due to the high threshold voltage of transistors in sub-micron CMOS processes. The integrated self-start in [10] requires an input voltage of at least 330mV to start the converter, and a capacitor pass-on scheme together with post-fabrication threshold-trimming of on-chip oscillator transistors in [11] achieves 95mV cold start. Alternatively, Schmitt trigger oscillators are used in [12] to achieve integrated cold-start at 70mV, but reliance on a conventional charge pump and large storage capacitor (1 nF) results in a slow start-up (1.5 s) and prevents further reduction of the cold-start voltage. An integrated oscillator reported in [13] successfully generates start-up clock at input voltage of 45mV, although converter cold-start is limited to 210mV.

In each of these implementations, a voltage multiplier boosts the low input voltage with the assistance of a start-up clock to power control circuits of an inductive converter during start-up. Although primarily limited by the minimum supply needed for the clock, cold-start voltage is also highly dependent on the boosting ability and output power of the start-up voltage multiplier.

In this work, we demonstrate an alternative integrated startup mechanism in which a one-shot pulse triggers the inductive converter to start operation. A start-up voltage multiplier is proposed that enables efficient voltage multiplication of the small input voltage by means of a high-gate-boosting scheme, implemented using cross-coupled complementary charge pumps. The multiplier operates with a start-up clock generated by an on-chip ring oscillator using a unique stacked-inverter delay element for ultra-low-voltage operation. The proposed start-up mechanism is implemented in a 0.18 μm CMOS process and achieves cold-start of an inductive boost converter at an input voltage as low as 57mV, which is the lowest cold-start voltage reported to date using a fully-integrated electrical circuit [14]. This paper describes detailed circuit architectures of key building blocks of the proposed start-up regime, including ultra-low-voltage clock generation, start-up voltage multiplier, and strobe generation, as well as low-voltage design challenges and extended block-level electrical characterization of the IC.

The rest of the paper is organized as follows: Section II describes the cold-start architecture; Section III elaborates design of the ultra-low-voltage ring oscillator; Section IV explains circuit details and operation of the proposed start-up voltage multiplier; generation of the strobe pulse is described in Section V; Section VI presents measured results from the fabricated IC; and, Section VII provides a brief conclusion.

II. Proposed One-Shot Cold Start Operation

Limited on-chip capacitance constrained by silicon area and low input voltage reduce charge transfer ($Q = CV$) through a charge-pump-based voltage multiplier. This is exacerbated by the low start-up clock frequency at low supply voltage, which results in a low output current.

As such, charging a large storage capacitor with the diminished output power of a charge pump is not prudent for low-voltage cold start. However, while a TEG provides low output voltage, it can provide a moderate amount of current due to its low source impedance (typically a few ohms); charging an inductor with this current can generate higher energy per cycle. To exploit this, rather than relying solely on a start-up charge pump, power transfer is quickly handed over to the inductive converter to achieve a low-voltage and fast cold-start operation.

The proposed cold-start architecture is shown in Fig. 1a. A start-up voltage multiplier initially boosts the input voltage to power a strobe generation unit (SGU). The voltage boosting ability of the multiplier is improved by using cross-coupled complementary charge pumps to enhance gate drive of the charge transfer switches. A low-voltage, on-chip ring oscillator generates the start-up clock for operation of the charge pumps. A strobe signal, V_{ST}, from the SGU turns on an auxiliary low-side (LS) switch, M_{LS1}, and charges the inductor with current from the TEG. As shown in Fig. 1b, a sharp falling edge of the one-shot pulse, V_{ST}, forces the voltage, V_S, to rise and forward-bias an active diode. The inductor current immediately charges a small on-chip storage capacitor, C_{INT} (350 pF), to a voltage $V_{INT} > 400$mV in the strobe-cycle itself.

A thyristor-based ring oscillator (TRO), designed to start oscillation with a low supply (400 mV) is powered immediately by V_{INT} and takes over control to operate the inductive converter. A wider LS switch, M_{LS2}, is now used to charge the inductor with higher current per cycle. V_{INT} is not connected to the output until it crosses a voltage threshold detected by the voltage detector D1. This ensures that all inductor energy is used to start the TRO during start-up. M_{LS1} is disabled during primary operation as V_{ST} goes low.

The proposed start-up scheme reduces the power burden on the voltage multiplier and achieves low-voltage start-up. In addition, the one-shot kick-start mechanism quickly hands over the power transfer process to a more efficient current-mode inductive boost converter and thereby speeds up the start-up process.

III. Ultra-low-voltage ring oscillator

An oscillator is required for operation of the start-up voltage multiplier. Ring oscillators, comprising a series of delay stages in closed loop are easy to integrate and have been used to generate start-up clocks [10]-[12]. To create sustained oscillation, required gain (A) of each delay stage and total number of stages (n) can be derived from Barkhausen criteria for oscillation as:

$$A \geq \sqrt{1+\left(\frac{\omega_o}{\omega_p}\right)^2} \text{ and } n = \pi/tan^{-1}\left(\frac{\omega_0}{\omega_p}\right) \quad (1)$$

where ω_0 is the frequency of oscillation and ω_p is the pole frequency contributed by each stage. As such, a smaller gain (A) requires a higher number of delay stages (n) for oscillation and results in a low output frequency (ω_o) of the ring oscillator.

A. Limitations of CMOS Inverter as delay element

At very low supply voltage, CMOS inverters suffer from low DC gain due to the significant deterioration of transconductance of the transistors. From Meindl's limit [15], minimum supply required for an inverter in a 0.18 μm bulk CMOS process to achieve DC gain greater than unity is 48mV at 300 °K [16]. Hence, this sets the theoretical limiting supply voltage for operation of a CMOS inverter-based ring oscillator.

Low supply voltage also degrades the output voltage rails of an inverter. As shown in Fig. 2, during an output transition, the difference current ($I_{ON} - I_{OFF}$) between active and inactive transistor charges or discharges the output. As V_{OUT} changes, $|V_{DS}|$ of the active transistor decreases and I_{ON} falls, whereas, $|V_{DS}|$ of the inactive transistor increases. Finally, V_{OUT} settles to V_H or V_L when $I_{ON} = I_{OFF}$. For a transistor in subthreshold operation with device width, W, and length, L, drain current, I_D, is given by

$$I_D = I_0 \cdot \frac{W}{L} \cdot e^{\left(\frac{|V_{GS}| - |V_{th}|}{\eta V_T}\right)} \cdot \left(1 - e^{-\frac{|V_{DS}|}{V_T}}\right) \quad (2)$$

where $I_0 (= \mu_0 \cdot C_{ox} \cdot (\eta - 1) \cdot V_T^2)$ is constant, η is the subthreshold swing factor, V_{th} is the threshold voltage, and V_T is the thermal voltage [17]. At very low supply, when $|V_{GS}| << |V_{th}|$ and $V_{DS} \sim V_T$, I_D strongly depends on $|V_{DS}|$. Thus, increase in $|V_{DS}|$ of the inactive transistor during V_{OUT} transition results in significant increase of I_{OFF}. Thereby, the difference current vanishes well before V_{OUT} reaches the supply rail (V_{DD} or GND) and reduces the output voltage rail ($V_H - V_L$) of the inverter (Fig. 2); simulated output rail is 20% lower than supply rail (50 mV) in 0.18 μm CMOS. As a consequence, the output clock of a CMOS inverter-based ring oscillator exhibits degraded voltage swing at low supply.

B. Proposed delay-element

Dynamic reduction of the leakage current, I_{OFF}, can improve output voltage swing at low supply. To achieve this, a delay element is proposed [18] comprising three inverters, arranged as shown in Fig. 3a. Outputs of INV1 and INV3 are connected to the sources of PMOS and NMOS transistors of INV2, respectively.

During the charging phase, a high-to-low transition of V_{IN} causes INV3 to pull node B to V_{DD}, as annotated in Fig. 3b. This reduces V_{DS} and V_{GS} across the NMOS transistor M4 of INV2 and suppresses the leakage current I_{OFF}. During the discharging phase, as V_{IN} transitions from low to high, INV1 pulls node A down to GND and suppresses I_{OFF} through the PMOS transistor M3 of INV2 by reducing both V_{SD} and V_{SG} across it. However, the $|V_{DS}|$ drop across M1 or M6 in the path of I_{ON} will reduce effective $|V_{GS}|$ across the active transistors, M3 and M4, respectively, in the corresponding phases. This would reduce effective I_{ON} and nullify the effect of lowering I_{OFF}. To alleviate, M1 and M6 are sized three times of the width of M3 and M4, respectively, while M2 and M5 are of same dimensions as M4 and M3.

Compared to other leakage suppression techniques, such as Schmitt trigger logic [19], the proposed stacked-inverter delay cell provides more effective leakage current bypassing at low supply by applying maximum $|V_{GS}|$ to M5 and M2 in the respective phases. It also yields faster pull up and pull down actions of M5 and M2; with the transition of V_{IN}, I_{OFF} is blocked at the onset of the V_{OUT} transition. A similar leakage bypassing technique adopted for designing a low-voltage ring oscillator in recent work [13] also demonstrates the effectiveness of the technique. It is important to note that, although leakage current, I_{OFF}, is suppressed from the output in both the phases, additional leakage currents through the bypass transistors, M2 and M5, increases total current consumption of the delay block as compared to a simple CMOS inverter. However, the increase in power consumption is negligible compared to other blocks when used in a complete energy harvester architecture.

Low-V_{th} transistors are used to increase conduction at the low supply voltage. Simulated VTC of the stacked-inverter delay block in a 0.18 μm CMOS process is shown in Fig. 4, which demonstrates a 13.3% improvement in output voltage rails and 32.5% higher DC gain compared to those of a CMOS inverter (INV2 alone) at a supply of 50 mV. The enhanced gain is due to the higher output impedance, R_o, at the final output of the delay element, which can be expressed as

$$R_o = \left[r_{o3} + (1 + g_{m3}r_{o3})R_{o1}\right] \parallel \left[r_{o4} + (1 + g_{m4}r_{o4})R_{o3}\right] \quad (3)$$

where R_{o1} and R_{o3} are the output impedances of INV1 and INV3, respectively, at the DC operating point. While the cascoding effects of M3 and M4 are small due to the small intrinsic gains, $g_{m3}r_{o3}$ and $g_{m4}r_{o4}$, at the low supply voltage, R_o of the stacked-inverter delay cell is still higher than the output impedance ($r_{o3} \| r_{o4}$) of INV2 alone. The g_m of M1-M6 together contribute to the delay cell transconductance.

A ring oscillator was implemented using 21 stages of the stacked inverter delay element to generate the start-up clock. At a supply of 50mV, the simulated frequency of the clock is 9.4 kHz at the typical corner; the frequency ranges between 2 kHz–38 kHz across process corners.

IV. Start-up voltage multiplier

A voltage multiplier is required during startup to boost the input voltage and power the cold-start control circuits. Low swing and low frequency of the pumping clock make designing such a multiplier especially challenging at low voltage.

A. Limitation of Conventional Charge Pumps

On-chip voltage multipliers such as the Dickson charge pump [20] can boost input voltage but incur a voltage drop across each stage diode. A cascaded dual-phase charge pump [21] mitigates this problem by providing a gate drive (V_{GS}) equal to the voltage swing of the clock (V_{CK}) to turn on the charge transfer switches (CTS). This works efficiently at nominal input voltage, but at low supply, V_{CK} ($< V_{DD}$) turns on the CTS only weakly. The resulting forward current in the *ON* phase is not much larger than the reverse leakage current in the *OFF* phase, causing inefficient charge transfer. Dynamic biasing of CTS [22], where boosted

voltages are borrowed from higher stages of the charge pump to generate a V_{GS} of $2 \cdot V_{CK}$ for the CTS can further improve charge transfer. However, at tens of millivolts of V_{DD}, the boosted V_{GS} still does not sufficiently improve on-conductance of the CTS. For instance, with V_{DD} = 50mV, more than $6 \cdot V_{CK}$ is needed to cross the threshold voltage of even low-V_{th} devices available in a 0.18 μm CMOS technology. In addition, overlapped phases of the pumping clock and the CTS gate clock in [22] result in reverse charge sharing, reducing pumping efficiency. Dynamic body biasing [23], [24] can also improve CTS on-conductance but is only effective for input voltages above 100mV.

For ultra-low-voltage operation, the high V_{GS} needed for each CTS can be generated by borrowing voltages from much later stages of the charge pump, as illustrated in Fig. 5. The gate boosters (GB) represent circuit blocks such as dynamically-biased inverters used to generate the gate clocks [22]. Additional diode-connected stages are needed to generate gate clocks for the final stages, which suffer from inefficient voltage boosting and will reduce CTS gate drive in the final stages. Also, loading of these stages (6 shown here) will result in a voltage drop of $6NI_{GB}R_o$ at the output, V_{OUT}, where N is the number of primary stages, I_{GB} is equivalent current consumption of each GB, and R_o is the equivalent resistance per stage. For 20-stage voltage multiplication, the voltage drop will be $120I_{GB}R_o$. As such, conventional gate-boosting techniques are insufficient at very low input voltage.

B. Proposed Cross-Coupled Complementary Gate Boosting

In this work, a high-gate-boosting technique is demonstrated using cross-coupled complementary charge pumps for ultra-low-voltage operation. As shown in Fig. 6, the first section of the proposed start-up charge pump comprises a six-stage positive charge pump (CP^+) and a six-stage negative charge pump (CP^-), each operating in dual phases. The supply voltage, V_{DD}, is applied to the CP^+ input, and input of the CP^- is connected to GND. PMOS switches are used as CTSs in CP^+, whereas isolated deep-n-well NMOS switches are used as CTSs in CP^-. The complementary charge pumps mutually boost the gate drive of their CTSs, as described below.

Dual-phase voltages from later stages of CP^- are borrowed to generate CTS gate clocks for earlier stages of CP^+. As illustrated in Fig. 7, negative dual-phase voltages $N5$ and $N5B$ from the 5th stage of CP^- and positive dual-phase voltages $P2$ and $P2B$ from the 2nd stage of CP^+ are used to generate gate clocks $G2$ and $G2B$ that swing between a higher voltage level of $P2 - P2B$ and a lower voltage level of $N5 - N5B$ for the PMOS switches of the 2nd stage of CP^+ using a gate booster circuit. The high negative voltage swing of the gate clock will boost the gate drive, V_{SG}, of the PMOS switch to $V_{DD} + 6V_{CK}$ in the charge transfer phase, while ensuring $V_{SG} = 0$ in the non-conduction phase. However, as CP^- also exhibits poor CTS conductance at low voltage, negative voltage rail of the gate clocks will be affected, thereby lowering the effective V_{SG} of the CTSs in CP^+. A fully-complementary structure of the charge pumps addresses this problem, where dual-phase voltage outputs of the complementary charge pump CP^+ are utilized to improve CTS conductance of CP^-. With the drain and source of the NMOS switch of CP^- connected to boosted negative voltages, the positive voltage of gate clocks $T5$ and $T5B$ utilizing a higher voltage level $P2 - P2B$ from CP^+ will increase the gate drive, V_{GS}, of NMOS switches of the 5th stage of CP^- to V_{DD}

+ 6 V_{CK} during the charge transfer phase, enhancing conduction. In a similar fashion, complementary outputs of the 1st CP^+ stage and 6th CP^- stage, 3rd CP^+ stage and 4th CP^- stage, and so on, generate CTS gate clocks of respective stages with the help of gate boosters, as shown in Fig. 6. This complementary gate boosting action improves the pumping efficiency of both charge pumps.

As shown in Fig. 6, the final 14 stages of the start-up charge pump further boost the output of CP^+ using PMOS switches whose gate clocks are generated borrowing lower voltages from earlier stages. The final stage of the charge pump uses diode-connected deep-*n*-well NMOS devices to prevent reverse charge flow during output voltage droop due to load transients. It is important to note that, although gate boosting of the negative charge pump causes additional loading, voltage drop in the load path from this effect is small (I_{GB}.[1+2+ …+6]R_o = 21$I_{GB}R_o$), as voltages are borrowed from the initial 6 stages. Compared to a conventional gate-boosting technique, which borrows voltage from later stages, the proposed technique borrows voltages from earlier stages to boost the gate clock of CTSs of CP^+. As such, no stage needs to wait for an increase in voltage at later stages for enhanced charge transfer, which makes the gate boosting action faster. Nonetheless, during initial cold-start state, the charge pump boosts the voltage using leakage current of the CTS with the available low-voltage swing (~ V_{DD}) of the intrinsic gate clocks; however, the regenerative action of the cross-coupled $CP^+ - CP^-$ assists the voltage multiplier to emerge quickly from this slow initial state.

Low-V_{th} devices are used for CTSs to improve charge transfer. While these exhibit higher leakage current compared to regular-V_{th} devices, enhanced conductivity with boosted gate drive makes reverse leakage negligible. The deep-*n*-well of the isolated NMOS devices in CP^- are shorted to *GND*, whereas the local body is shorted to the source and connected to the nearest minimum voltage terminal. This allows the NMOS switches to handle negative voltages without forward biasing the deep-*n*-well junction and without V_{th} degradation due to body bias. High-density MOS capacitors, each 20 pF, are used as pumping capacitors, optimizing switching resistance, 1 /(Cf_{CK}), while ensuring slow switching limit operation by keeping charging time constant ($CR_{on} \ll 1/f_{CK}$) [25]. A 120 pF decoupling capacitor, C_{OUT}, is added to the final output, V_{CP}, using MOS capacitors.

C. Non-Overlapping Boosting of Gate Clocks

Gate clocks of the CTSs are generated using the gate-booster circuit illustrated in Fig. 8a. The boosted gate clocks must be non-overlapping with the pumping clocks to avoid reverse charge flow in the non-charge-transfer phase. The level shifters L1-L2 and L3-L4 take dual-phase outputs of the charge pump ($P - PB$ and $N - NB$) and generate corresponding non-overlapped phases using clocks $CK_{NOV\,A}$, $CK_{NOV\,B}$, $CKB_{NOV\,A}$, and $CKB_{NOV\,B}$, as shown in the timing diagram in Fig. 8b. These clock phases are generated using low-voltage NAND logic, implemented with a similar leakage suppression technique as discussed in Section II. As shown in Fig. 8a, *INV*1 and *INV*2 suppress leakage currents of the pull-up transistors; *INV*3,M_{BN}, and M_{BP} suppress leakage currents of the pull-down transistors. MOS capacitors, each 2 pF, are used in the non-overlapping level-shifters.

Outputs of the level-shifters, $P_{NOV\,B}$, $PB_{NOV\,B}$, $N_{NOV\,B}$ and $NB_{NOV\,B}$, are fed to the dynamic inverter X1 to generate gate clock TB that swings between the higher positive voltage levels of $P-PB$ and lower negative voltage levels of $N-NB$ as shown in Fig. 8b. Similarly, gate clocks G, GB, and T are generated using X2-X4. For the final 14 stages of the voltage multiplier, the same gate booster circuit is used, where $N-NB$ are replaced by positive voltage outputs of lower stages.

Poor gate drive of transistors in X1-X4 causes slow transition of the boosted gate clocks; to ensure non-overlap of the final gate clocks with the pumping clocks, the delay between falling edges of $CK_{NOV\,A}$ and CK is designed to be larger than the delay between their rising edges. Timing of other phases are set accordingly. The clocks are driven by higher strength stacked-inverter cells to drive long routing paths. Routing is laid out symmetrically to ensure correct phases and minimal skew at the final destinations.

V. Strobe generation and one-shot start-up

A strobe generation unit (SGU) is powered by the output of the start-up voltage multiplier, V_{CP}, to generate the control pulse, V_{ST}, required to kick-start the inductive boost converter. The SGU consists of a voltage detector, delay generator, and strobe logic circuit. As the output power of the charge pump is low, the SGU must operate with very small quiescent current.

The voltage detector output, V_{DET}, asserts V_{ST} once V_{CP} crosses a threshold sufficiently higher than the V_{th} of M_{LS1} to energize the inductor with required start-up current. A low-power reference generator is implemented using low-V_{th} and high-V_{th} transistors, M1 and M2, respectively [26]. Static current is minimized by using long-channel (10μm) devices for M1 and M2; settling of V_{REF} is still fast compared to the slow rise of V_{CP}, as shown in Fig. 9b. The detector comprises high-V_{th} PMOS transistors M3 and M4. Current through M3 is compared against leakage current through M4 (gate-source shorted); with the rise of V_{CP}, V_{SG} of M3 increases, and as current through M3 goes above the leakage current of M4, the output V_{DET} starts rising and follows V_{CP}. The width of M4 is set 10 times the width of M3 for higher effective threshold, $V_{REF}+V_{SG,M3}$. M_{LS1} is sized to energize the inductor with required start-up current without substantially slowing the falling-edge transition of V_{ST} due to larger gate capacitance.

V_{DET} is delayed to generate V_A using a thyristor-based latch formed by transistors M6-M7 [27]. The capacitor C_{DEL} is precharged to V_{CP} by M5 before V_{DET} rises. Once M5 turns off, the latch is enabled by turning M8 on and M9 off using V_{DET}. As C_{DEL} is discharged by leakage current while V_{CP} rises, V_{SG} of M6 increases, which charges the gate of M7; the M6-M7 regenerative feedback quickly discharges C_{DEL}. The thyristor latch avoids crowbar current during voltage transitions and minimize power consumption.

V_{ST} is finally generated from V_A and V_B using NOR logic (M10-M13) and buffered to the gate of M_{LS1}. All internal buffers ($I1-I3$) are designed with high-V_{th} transistors to reduce leakage current. Simulated current consumption of the sub-blocks of the SGU is shown in Fig. 9a.

An active diode with low static current consumption [28] is used to reduce voltage drop in the current path from the inductor to the capacitor, C_{INT}. An energy-efficient thyristor-based oscillator (TRO) [29] is designed to oscillate at a supply voltage as low as 400mV. This enables the clock, *CK*, immediately following the strobe cycle and it takes over control of the inductive boost converter. As the TRO takes the control, the inductor is energized using a wider LS switch M_{LS2}. Following cold start, the inductive boost converter is operated in discontinuous conduction mode (DCM), favorable for the low power level of the application.

In order to kick-start the inductive boost converter successfully with the one-shot strobe pulse, the energy stored in the inductor during the strobe cycle must be sufficient to power the TRO, which can be expressed as:

$$\frac{1}{2}\cdot L\left(\frac{V_{TEG}}{R_{LS1}}\right)^2 > \frac{1}{2}\cdot C_{INT}V_{INT}^2 + \frac{V_{INT}I_{TRO}}{f_s} \tag{4}$$

where R_{LS1} is the on-resistance of M_{LS1} during the strobe cycle, f_s is the frequency of *CK*, and I_{TRO} is the current drawn by the TRO. Conduction loss and leakage current through the active diode are negligible and are not included in the above condition for simplicity. R_{LS1} is dependent on the voltage drive (V_{ST}) and size of M_{LS1} during the strobe period, whose upper limits are bounded by the available output power of the start-up voltage multiplier at the cold-start voltage.

The inductor value, *L* gives another degree of freedom to meet this condition, as expressed in (4). While higher f_s seems favorable to reduce the start-up energy requirement in (4), this increases I_{TRO} and minimum value of V_{INT} to start the TRO. Based on the available output power of the voltage multiplier and on setting gate drive and size of M_{LS1} accordingly, it is calculated that an inductance value of higher than 100 μH is enough to meet the condition expressed in (4).

A frequency of 25 kHz is chosen for *CK* to optimize the conduction and switching losses of the converter, along with meeting the requirement of starting up the TRO with a small supply of 400mV. Although *CK* has a duty cycle of 66.67%, it still ensures DCM operation of the boost converter due to the high conversion ratio ($t_{OFF} >> t_{ON}$). This creates a t_{ON} of 26.8 μs, and the peak inductor current is kept much below the saturation current limit of the inductor for the whole input voltage range.

VI. Measurements

The proposed cold-start architecture was fabricated in a 0.18 μm CMOS process. Fig. 10a shows the die photograph of the implemented chip, where the cold-start block occupies 0.6 mm × 1.6 mm silicon area.

The start-up clock, CK_{STUP}, generated from the ultra-low-voltage ring oscillator is buffered to an output pin for measurements; buffers are powered using a separate test-only supply rail. Output transient of the start-up clock in Fig. 11 shows that oscillation starts at an input supply voltage as low as 40 mV, which demonstrates effective leakage suppression using the proposed stacked-inverter delay cells. The measured voltage swing of the clock is lower than

the internal clock swing due to the loading of the low-voltage test buffers by pad and probe parasitics.

A test output of the start-up voltage multiplier is buffered using an off-chip buffer to minimize probe loading during characterization. Measured output transient in Fig. 12 shows that an input voltage of 55mV is boosted by the multiplier to an output of 840mV, with an estimated load current of hundreds of picoamps due to the finite input impedance of the off-chip buffer. Boosted gate clocks cannot be measured at minimum input supply due to low drivability. As such, boosted gate clocks of the 7th stage of CP^{+} and the 3rd stage of CP^{-} are shown in Fig. 13 using an input supply of 120mV.

Pumping efficiency of the charge-pump-based voltage multiplier was measured across varying input voltage using a digital multimeter with an input impedance > 1 GΩ to measure output voltage. The output power was measured using a source meter (Keithley 2450) as a current sink. The measurement was done for an input voltage range relevant for the target application, body-heat energy harvesting, where the cold-start block will be exposed mostly to sub-100mV TEG voltages due to the small ΔT between skin and ambient.

As shown in Fig. 14, the proposed start-up voltage multiplier achieves a pumping efficiency higher than 78% across an input voltage range of 50mV - 100mV, with a peak value of 93% at an input voltage of 65mV. Pumping efficiency of the voltage multiplier is maximized at low input voltages to reduce the minimum cold-start voltage. At higher input voltages, large swing of the boosted gate clocks causes the gate boosters to draw more current driving CTS gates and increases internal loading. Additionally, low pumping-clock frequency due to large number of delay stages in the ring oscillator reduces-pumping effciency of the voltage multiplier at higher input voltages. Nevertheless, boosted output of the voltage multiplier at higher input voltages can easily power the SGU to generate the start-up strobe.

The start-up performance of the proposed architecture is characterized using a bench-top power supply with added 5 Ω series resistance to imitate a typical TEG source. A 220 μH off-chip inductor is used for the primary boost converter. The value of the inductor is chosen a higher than the minimum required value derived in Section V to mitigate additional conduction losses due to inefficient routing. As shown in Fig. 15, the primary converter starts with a minimum source voltage of 57mV. Although the standalone voltage multiplier operates at lower input voltage, leakage current of the SGU loads the multiplier output and prevents start-up at lower voltage. The minimum operational voltage of the key blocks are summarized in Table I.

Due to the fast one-shot start-up mechanism, it takes only 135 ms for cold-start. The zoomed waveform in Fig. 15 shows inductive overshoot at V_S with the falling edge of V_{ST}. A rise in V_{INT} above 400mV following the strobe-cycle starts the TRO immediately, and CK takes control of the inductive boost converter. Once started, the output voltage rises to an unregulated 1.8 V with no load.

The measured efficiency of the boost converter is 20% at the 57mV cold-start voltage, and the efficiency increases to 47% at input voltage of 100mV. As observed, the efficiency of the converter is relatively low due to comparatively high conduction losses, including the on-

resistance of the low-side switch, M_{LS2}, that charges the inductor following the cold-start, as well as parasitic routing resistance that can be improved in future implementations.

While the cold-start block draws current from the source during the normal operation of the boost converter, this small input current (Fig. 16) is drawn from the low-side input voltage, and power consumed by the cold-start block is negligible compared to the input power of the boost converter and does not affect overall efficiency. As such, the cold-start block is not functionally de-activated during normal operation. Nevertheless, disabling the cold-start block with the start of the inductive converter will increase the maximum input voltage range of the boost converter, ensuring that devices in the startup voltage multiplier remain within voltage stress tolerance at higher input voltages (>100 mV).

Cold start was also demonstrated using a commercial TEG (Marlow TG12-6-01L); the experimental setup is shown in Fig. 10b. The measured input and output transient waveforms in Fig. 17 show that the boost converter starts at an input voltage of 57mV, as expected, which corresponds to a ternperature gradient of ΔT=1.6° C, and sustains operation until input voltage falls below 25mV (ΔT = 0.8°C). The total energy used from the TEG for cold start is 90 nJ.

Prior to the operation of the inductive converter, the cold-start block is the only active block and draws less than 6 μA of current from the source, as shown in Fig. 16. Once started, the inductive converter draws an input power of 20 μW at the cold-start voltage and sustains operation with a minimum input power of 2.5 μW. The minimum input voltage for cold-start of the converter was checked across 5 chips and varies from 57mV to 61mV.

Performance of the proposed cold-start architecture is compared against state-of-the-art in Table II While [4] achieved low-voltage cold start with the aid of mechanical vibrations, [8] and [9] used additional off-chip inductors. The cold-start time, defined as the time required from power-on to starting the primary boost converter, is determined by the ability of the low-power start-up voltage multiplier to power start-up control circuits of the inductive boost converter. While the rise time of the final output depends on the inductor current and the output load cap, a majority of the start-up time is consumed by the slow, low-voltage cold-start. The proposed fully-integrated cold-start architecture achieves cold-start of the boost converter at 18% lower input voltage and in 48% less time, even at 1.6× lower input voltage, compared to previously demonstrated on-chip implementations [11], [12].

VII. Conclusion

An integrated cold-start architecture was presented to start inductive boost converters at very low input voltage toward realizing autonomous body heat energy harvesting using thermoelectric generators. Challenges of on-chip voltage multiplication at small input voltage have been addressed by applying a unique cross-coupled gate boosting technique using complementary charge pumps. An efficient leakage suppression technique was also demonstrated using stacked inverters to generate a start-up clock using an integrated ring oscillator at 40mV input supply voltage. The one-shot start-up mechanism achieves

integrated cold-start of the boost converter an input voltage as low at 57mV, and it takes only 135 ms to start an inductive boost converter.

In general, the proposed architecture and described design efforts were focused on implementation and optimization of the cold-start architecture, demonstrating a fast and low-voltage one-shot cold-start technique with the aid of the proposed voltage multiplier. once started, additional features can be added to further enhance the primary inductive boost converter efficiency, including maximum power transfer and zero-current sensing.

Cold-start and handover to a primary boost converter were also demonstrated using a commercial TEG as input with a temperature gradient <2°C, illustrating the utility of the proposed architecture for realizing fully-autonomous thermal energy harvesting from human body heat.

Acknowledgment

Research reported in this publication was supported in part by the National Institutes of Health under award number R21DE027170. The content is solely the responsibility of the authors and does not necessarily represent the official views of the National Institutes of Health.

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References

[1]. Leonov V, Torfs T, Fiorini P, and Hoof CV, "Thermoelectric converters of human warmth for self-powered wireless sensor nodes," IEEE Sensors Journal, vol. 7, no. 5, pp. 650–657, 5 2007.

[2]. Snyder GJ and Toberer ES, "Complex thermoelectric materials," Nature Materials, vol. 7, pp. 105 EP –, 2 2008, review Article. [Online]. Available: 10.1038/nmat2090 [PubMed: 18219332]

[3]. Carlson EJ, Strunz K, and Otis BP, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," IEEE Journal of Solid-State Circuits, vol. 45, no. 4, pp. 741–750, 4 2010.

[4]. Ramadass YK and Chandrakasan AP, "A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage," IEEE Journal of Solid-State Circuits, vol. 46, no. 1, pp. 333–341, 1 2011.

[5]. Shrivastava A, Roberts NE, Khan OU, Wentzloff DD, and Calhoun BH, "A 10 mV-input boost converter with inductor peak current control and zero detection for thermoelectric and solar energy harvesting with 220 mV cold-start and–14.5 dBm, 915 MHz RF kick-start," IEEE Journal of Solid-State Circuits, vol. 50, no. 8, pp. 1820–1832, 8 2015.

[6]. Teh Y and Mok PKT, "Design of transformer-based boost converter for high internal resistance energy harvesting sources with 21 mV self-startup voltage and 74% power efficiency," IEEE Journal of Solid-State Circuits, vol. 49, no. 11, pp. 2694–2704, 11 2014.

[7]. Im J, Wang S, Ryu S, and Cho G, "A 40 mV transformer-reuse self-startup boost converter with MPPT control for thermoelectric energy harvesting," IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 3055–3067, 12 2012.

[8]. Weng P, Tang H, Ku P, and Lu L, "50 mV-input batteryless boost converter for thermal energy harvesting," IEEE Journal of Solid-State Circuits, vol. 48, no. 4, pp. 1031–1041, 4 2013.

[9]. Lim B, Seo J, and Lee S, "A colpitts oscillator-based self-starting boost converter for thermoelectric energy harvesting with 40-mV startup voltage and 75% maximum efficiency," IEEE Journal of Solid-State Circuits, pp. 1–10, 2018.

[10]. Kadirvel K, Ramadass Y, Lyles U, Carpenter J, Ivanov V, McNeil V, Chandrakasan A, and Lum-Shue-Chan B, "A 330 nA energy-harvesting charger with battery management for solar and thermoelectric energy harvesting," in *2012* IEEE International Solid-State Circuits Conference, 2 2012, pp. 106–108.

[11]. Chen P, Ishida K, Ikeuchi K, Zhang X, Honda K, Okuma Y, Ryu Y, Takamiya M, and Sakurai T, "Startup techniques for 95 mV step-up converter by capacitor pass-on scheme and V_{th}-tuned oscillator with fixed charge programming," IEEE Journal of Solid-State Circuits, vol. 47, no. 5, pp. 1252–1260, 5 2012.

[12]. Goeppert J and Manoli Y, "Fully integrated startup at 70 mV of boost converters for thermoelectric energy harvesting," IEEE Journal of Solid-State Circuits, vol. 51, no. 7, pp. 1716–1726, 7 2016.

[13]. Luo Z, Zeng L, Lau B, Lian Y, and Heng C, "A sub-10 mV power converter with fully integrated self-start, MPPT, and ZCS control for thermoelectric energy harvesting," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 5, pp. 1744–1757, 5 2018.

[14]. Bose S, Anand T, and Johnston ML, "Fully-integrated 57 mV cold start of a thermoelectric energy harvester using a cross-coupled complementary charge pump," in *2018* IEEE Custom Integrated Circuits Conference (CICC), 4 2018, pp. 1–4.

[15]. Meindl JD and Davis JA, "The fundamental limit on binary switching energy for terascale integration (TSI)," IEEE Journal of Solid-State Circuits, vol. 35, no. 10, pp. 1515–1516, 10 2000.

[16]. Zhai B, Blaauw D, Sylvester D, and Flautner K, "The limit of dynamic voltage scaling and insomniac dynamic voltage scaling," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 11, pp. 1239–1252, 11 2005.

[17]. Roy K, Mukhopadhyay S, and Mahmoodi-Meimand H, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," Proceedings of the IEEE, vol. 91, no. 2, pp. 305–327, 2 2003.

[18]. Bose S and Johnston ML, “A stacked-inverter ring oscillator for 50 mV fully-integrated cold-start of energy harvesters,” in *2018* IEEE International Symposium on Circuits and Systems (ISCAS), 5 2018, pp. 1–5.

[19]. Lotze N and Manoli Y, “A 62 mV 0.13μm CMOS standard-cell-based design technique using schmitt-trigger logic,” IEEE Journal of Solid-State Circuits, vol. 47, no. 1, pp. 47–60, 1 2012.

[20]. Dickson JF, “On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique,” IEEE Journal of Solid-State Circuits, vol. 11, no. 3, pp. 374–378, 6 1976.

[21]. Pelliconi R, Iezzi D, Baroni A, Pasotti M, and Rolandi PL, “Power efficient charge pump in deep submicron standard CMOS technology,” IEEE Journal of Solid-State Circuits, vol. 38, no. 6, pp. 1068–1071, 6 2003.

[22]. Wu J-T and Chang K-L, “MOS charge pumps for low-voltage operation,” IEEE Journal of Solid-State Circuits, vol. 33, no. 4, pp. 592–597, 4 1998.

[23]. Chen P-H, Ishida K, Zhang X, Okuma Y, Ryu Y, Takamiya M, and Sakurai T, “0.18 V input charge pump with forward body biasing in startup circuit using 65nm CMOS,” in IEEE Custom Integrated Circuits Conference 2010, 9 2010, pp. 1–4.

[24]. Kim J, Mok PKT, and Kim C, “A 0.15 V input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement,” IEEE Journal of Solid-State Circuits, vol. 50, no. 2, pp. 414–425, 2 2015.

[25]. Seeman MD and Sanders SR, “Analysis and optimization of switched-capacitor DC-DC converters,” IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 841–851, 3 2008.

[26]. Seok M, Kim G, Blaauw D, and Sylvester D, “A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V,” IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2534–2545, 10 2012.

[27]. Kim G, Kim M-K, Chang B-S, and Kim W, “A low-voltage, low-power CMOS delay element,” IEEE Journal of Solid-State Circuits, vol. 31, no. 7, pp. 966–971, 7 1996.

[28]. Rozgić D and Marković D, “A miniaturized 0.78-mW/cm^2 autonomous thermoelectric energy-harvesting platform for biomedical sensors,” IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 773–783, 8 2017. [PubMed: 28541912]

[29]. Liu X and Sanchez-Sinencio E, “A single-cycle MPPT charge-pump energy harvester using a thyristor-based VCO without storage capacitor,” in 2016 IEEE International Solid-State Circuits Conference (ISSCC), 1 2016, pp. 364–365.

[30]. Cao P, Qian Y, Xue P, Lu D, He J, and Hong Z, “27.1 An 84% peak efficiency bipolar-input boost/flyback hybrid converter with MPPT and on-chip cold starter for thermoelectric energy harvesting,” in 2019 IEEE International Solid- State Circuits Conference - (ISSCC), 2 2019, pp. 420–422.

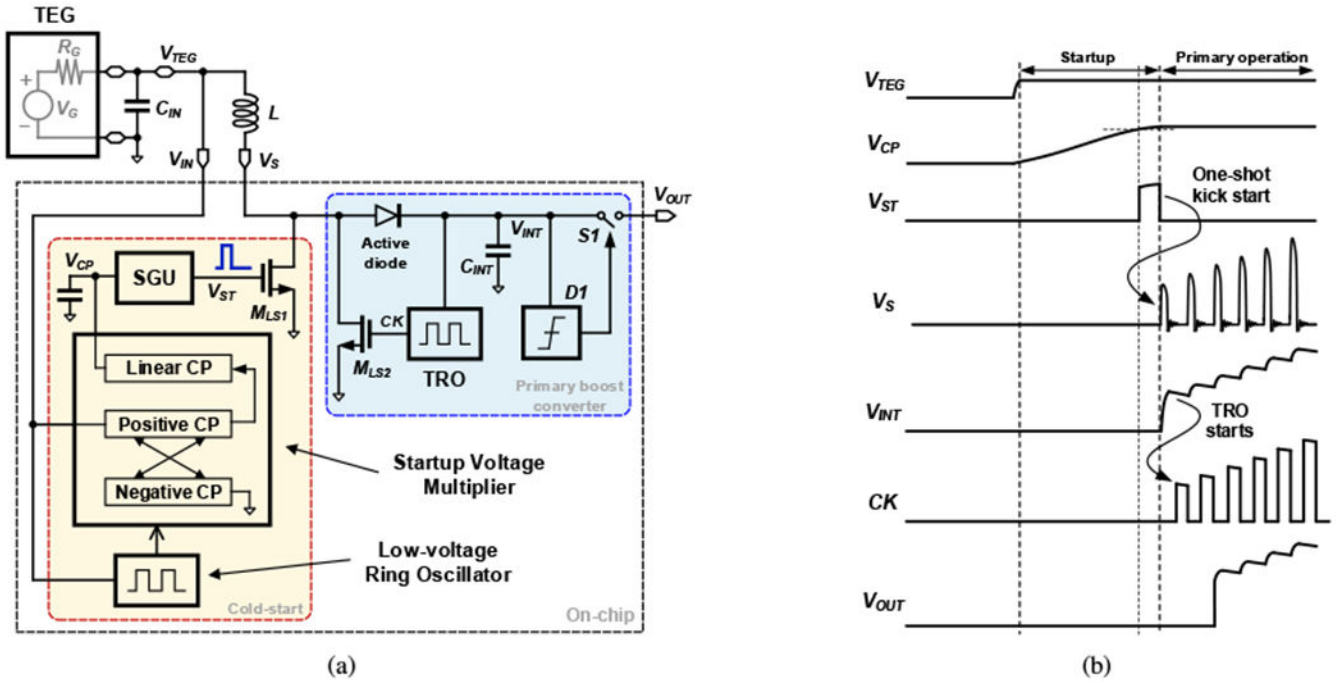

Fig. 1.

(a) Proposed integrated cold-start architecture, (b) timing diagram of the cold-start sequence utilizing a fast-falling edge of a strobe pulse for quick triggering of the primary inductive boost converter.

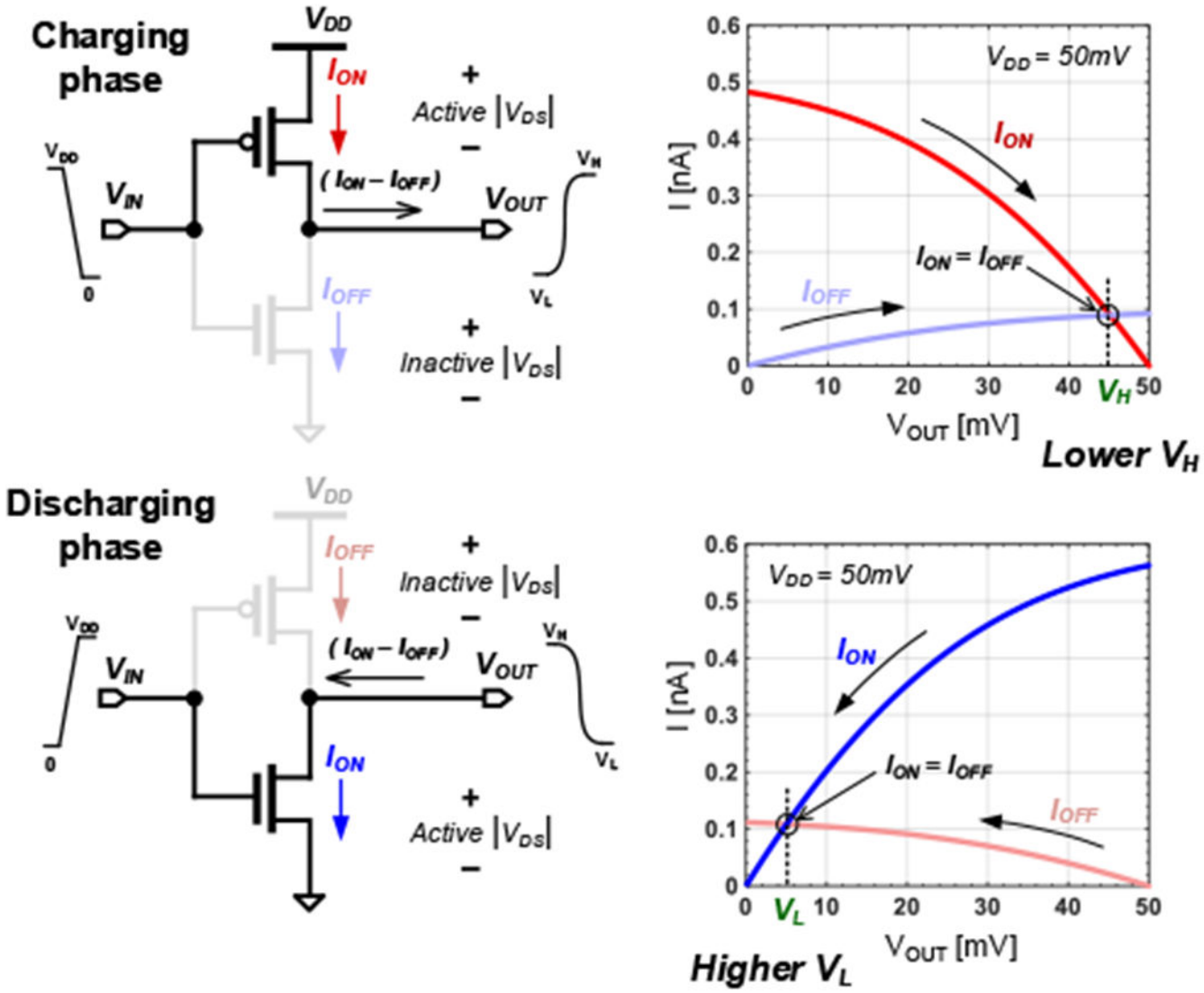

Fig. 2.
Low output voltage rail of a CMOS inverter at low supply

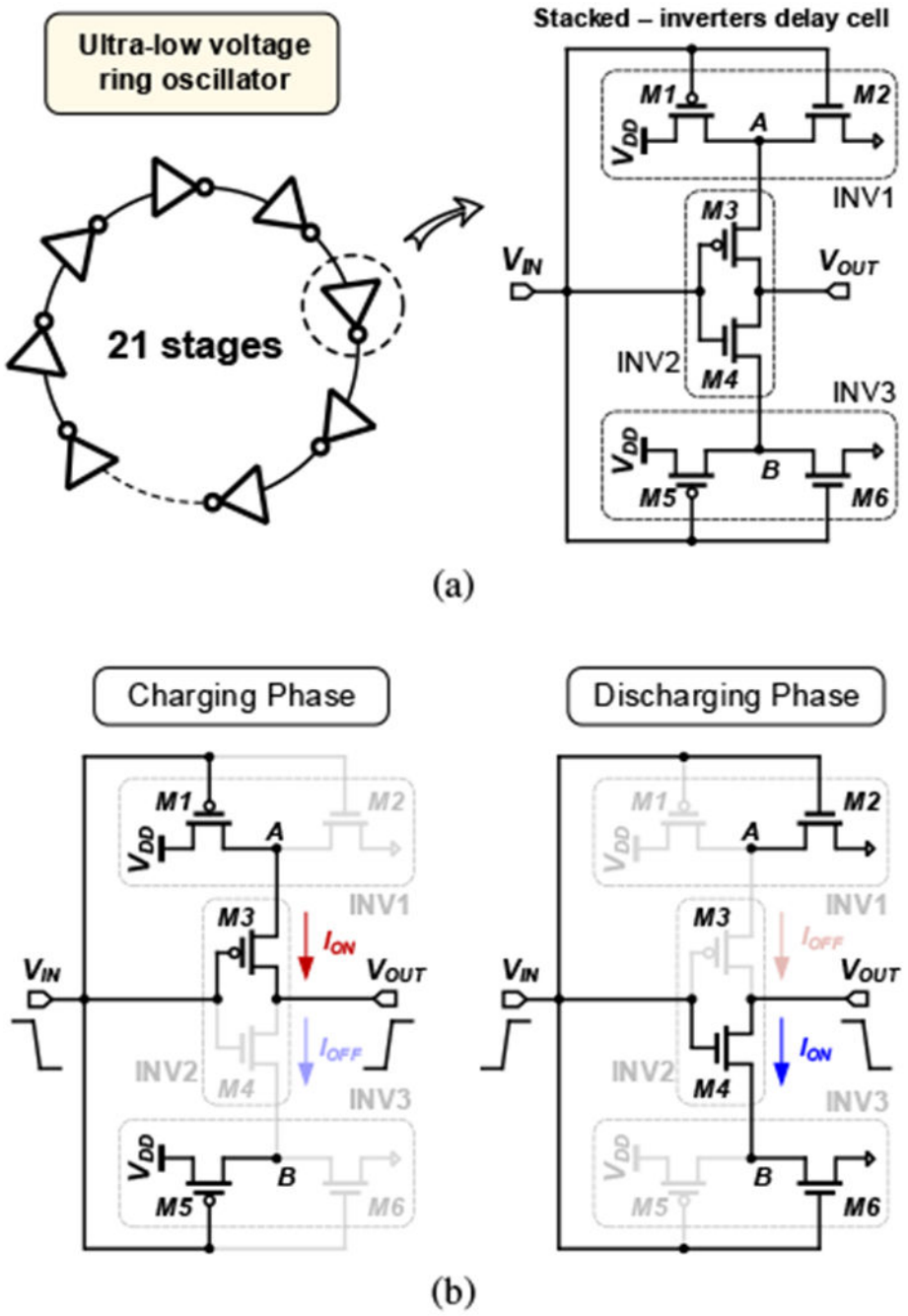

Fig. 3.

(a) Ultra Low-voltage ring oscillator comprising the proposed stacked-inverters based delay cells, (b) Leakage current suppression in the delay cell in charging and discharging phases.

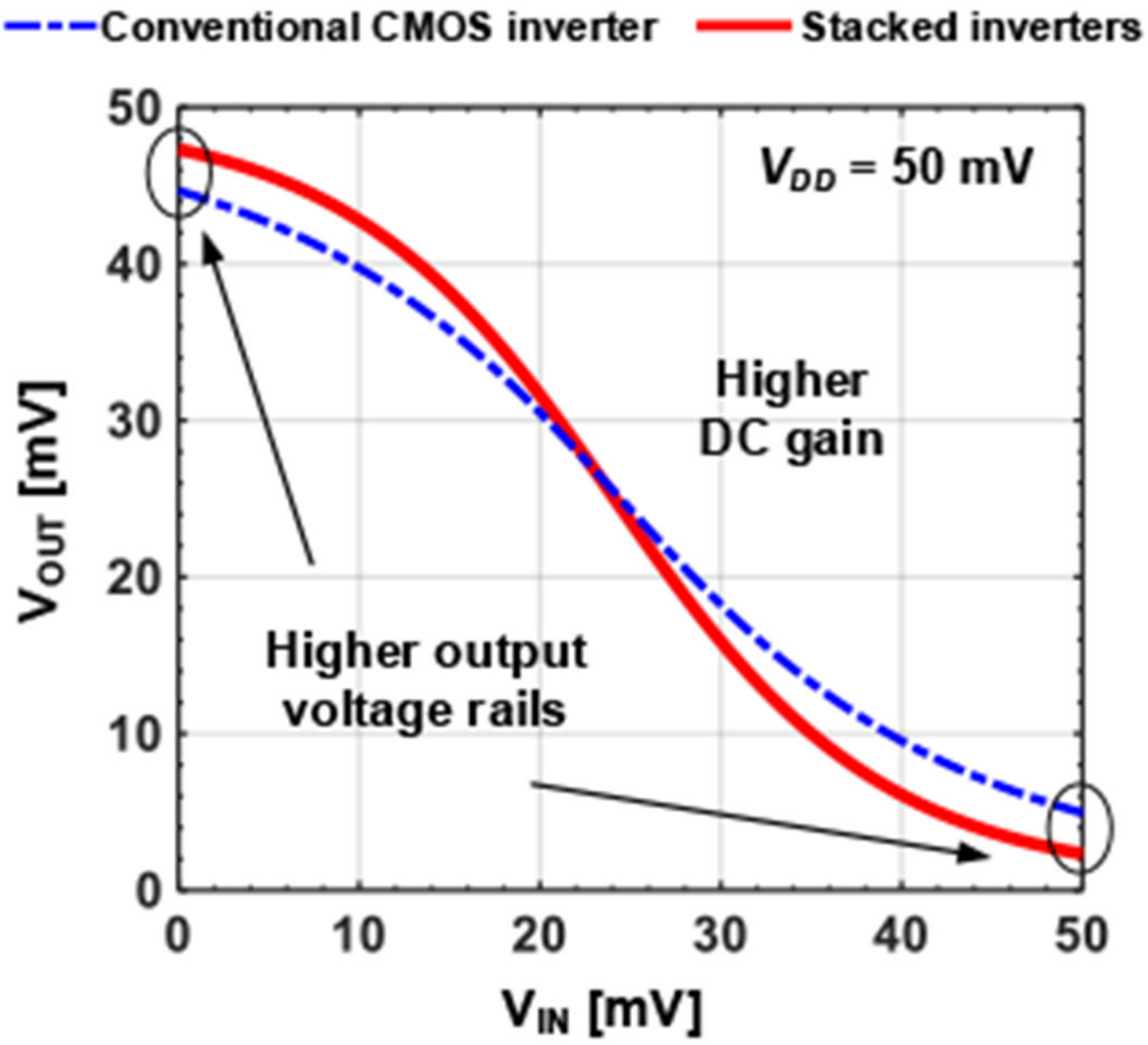

Fig. 4.
Simulated VTC of the proposed delay cell shows improvement of DC gain and output voltage rails over conventional CMOS inverter.

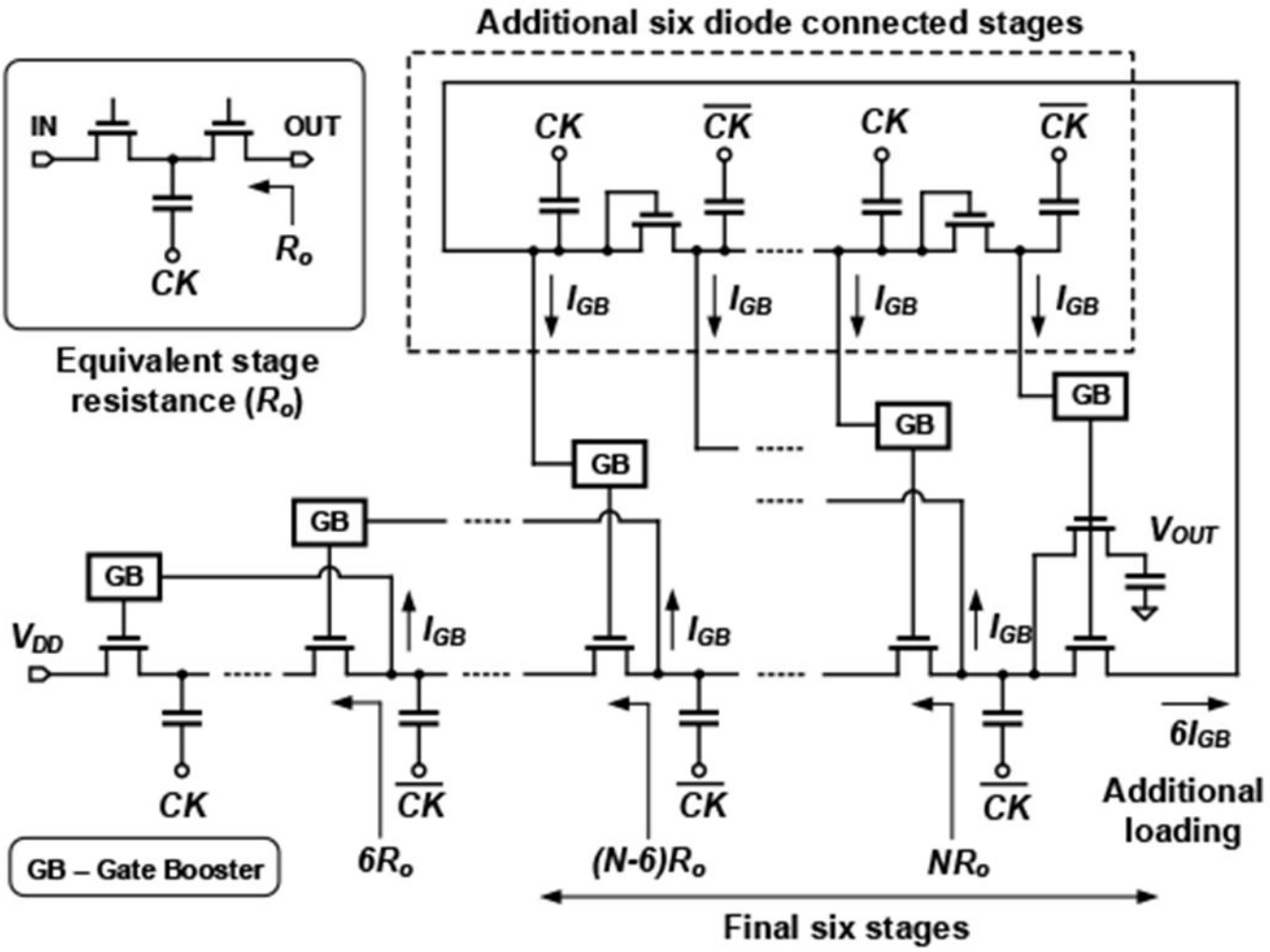

Fig. 5.
Loading effect in high gate boosting by borrowing voltages from much later stages.

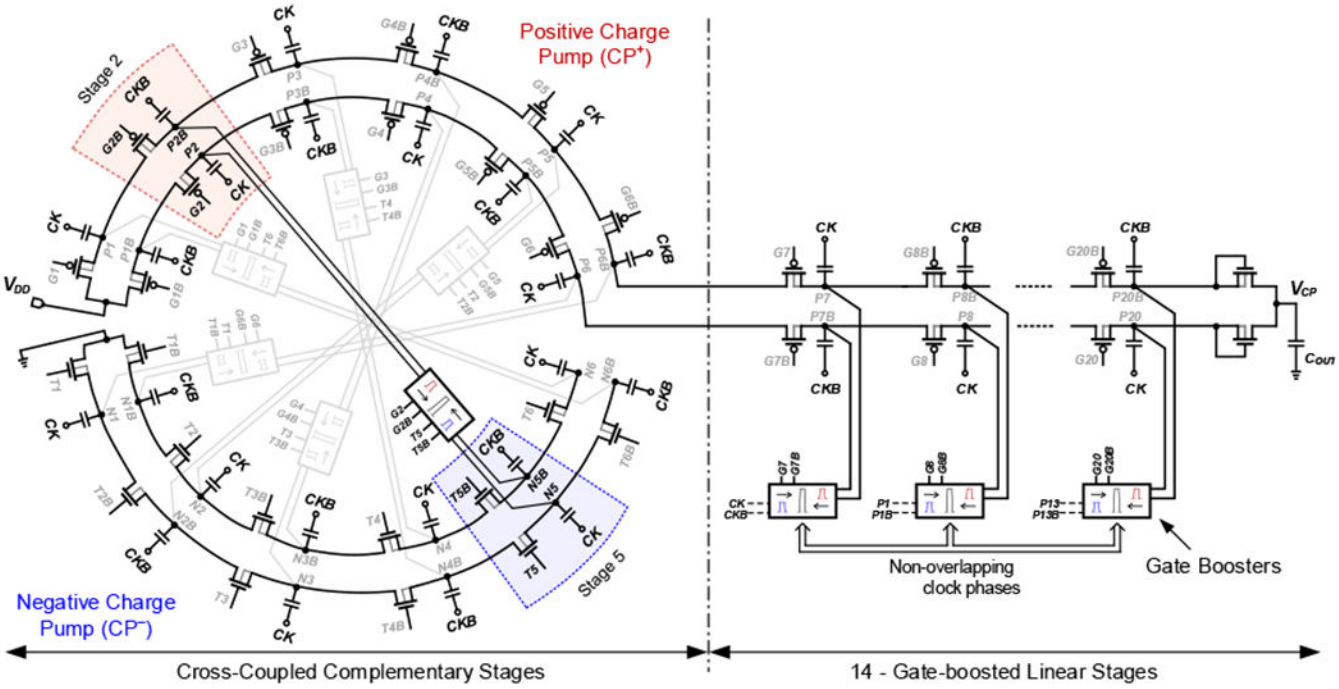

Fig. 6.

Proposed start-up voltage multiplier, using cross-coupled complementary charge pumps for high gate-boosting and low voltage operation.

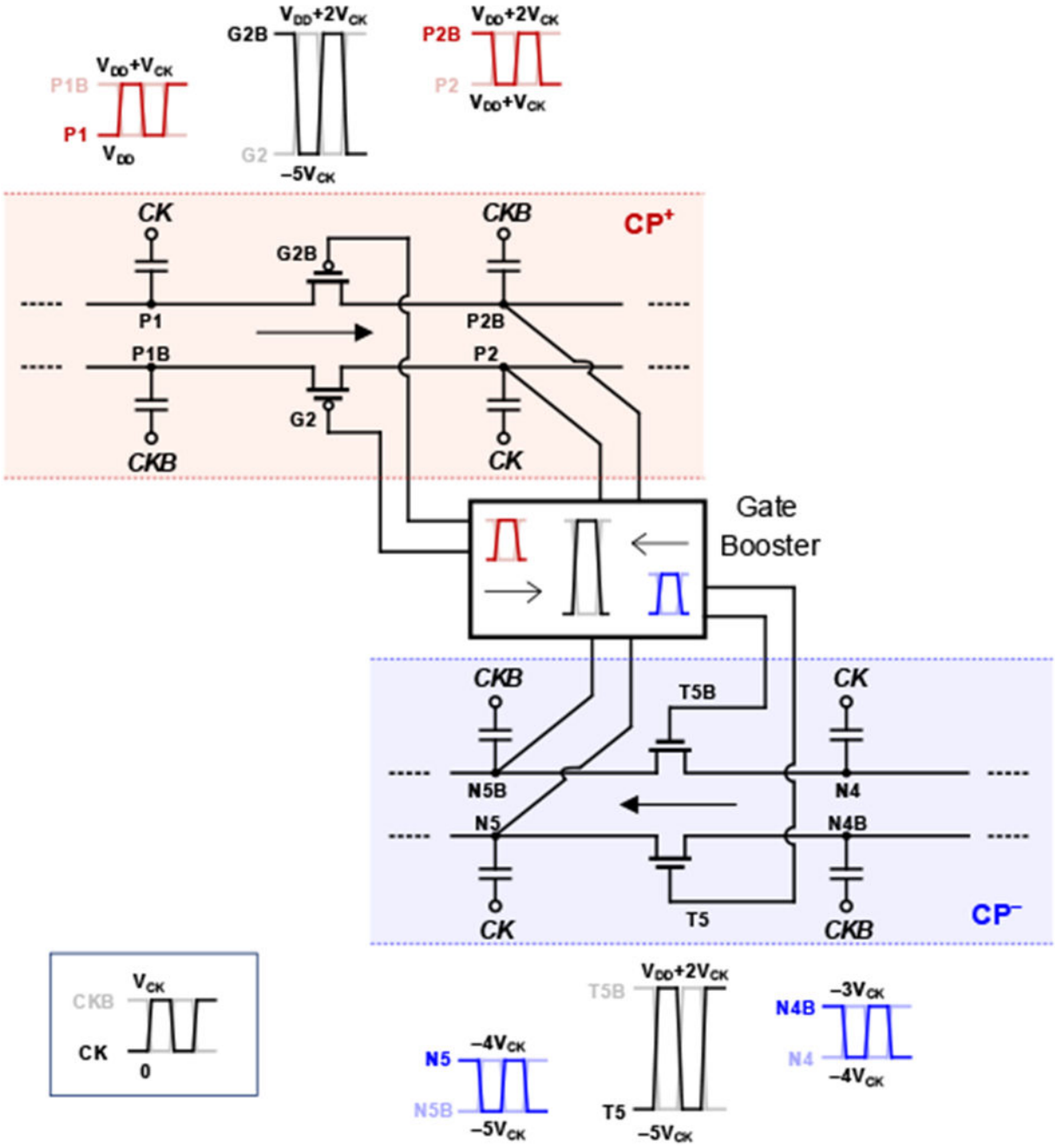

Fig. 7.

Mutual voltage boosting of gate clocks borrowing dual phased outputs of complementary charge pumps.

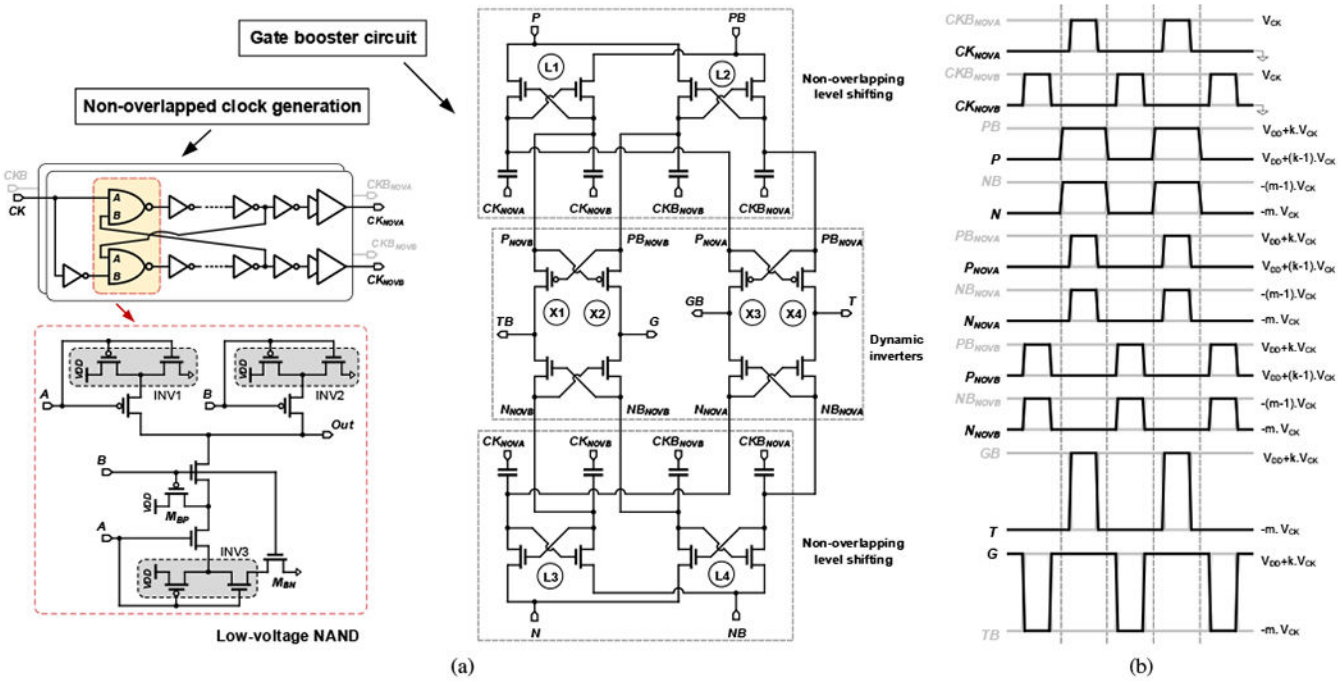

Fig. 8.

(a) Generation of non-overlapping gate clocks with boosted voltage swing, and (b) timing diagram for gate clock generation.

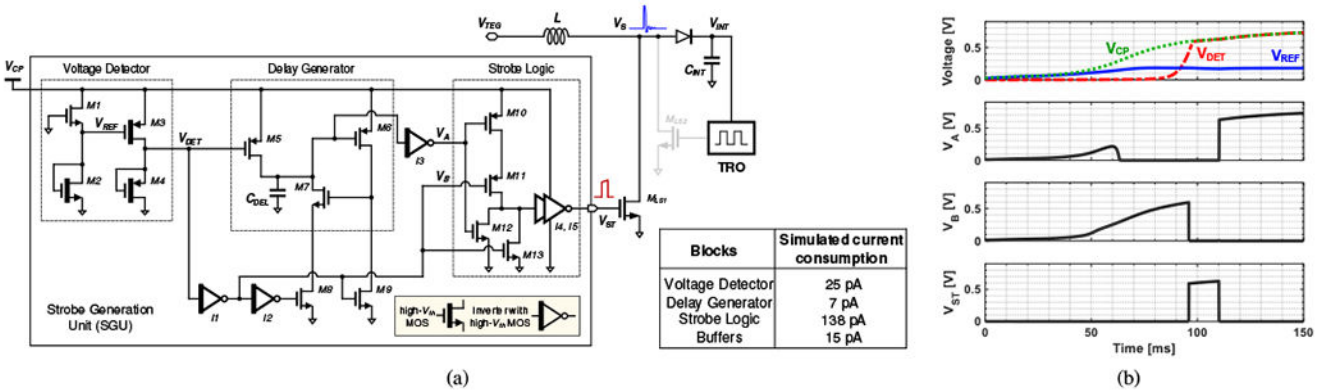

Fig. 9.

(a) Circuit schematics of the strobe generation unit (SGU) with simulated current consumption of each functional blocks, (b) simulated waveforms showing functionality of the SGU.

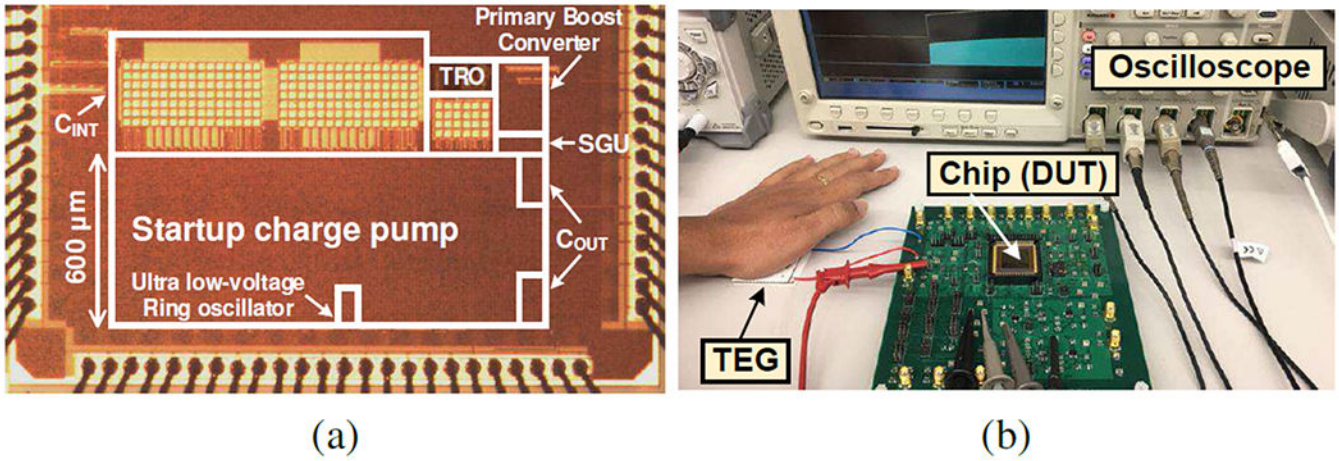

Fig. 10.

(a) Die photo of the chip fabricated in 0.18 μm CMOS technology, (b) experimental set up for measurements with commercial TEG attached to human body.

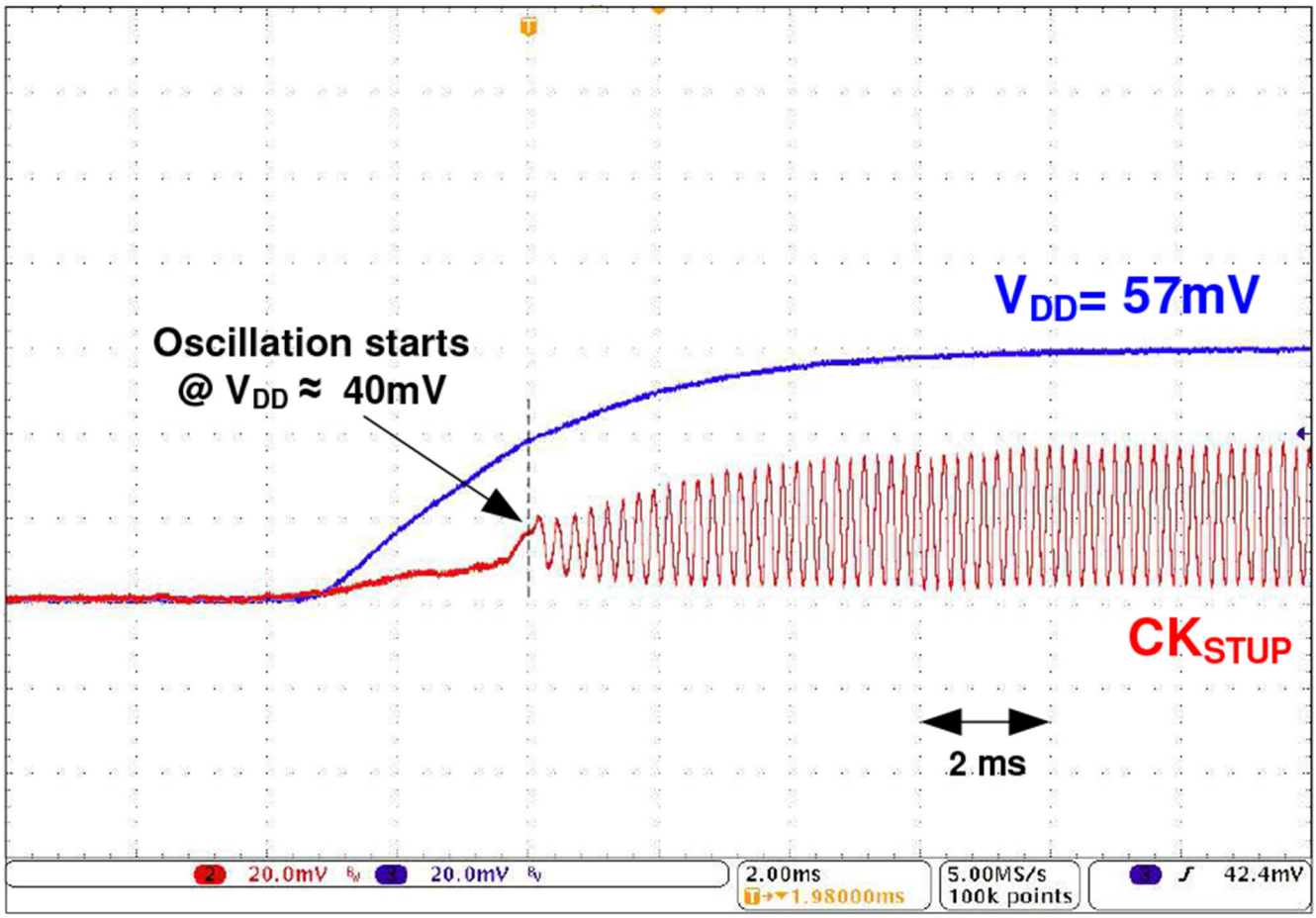

Fig. 11.
Measured start-up clock generated by the ultra-low-voltage ring oscillator.

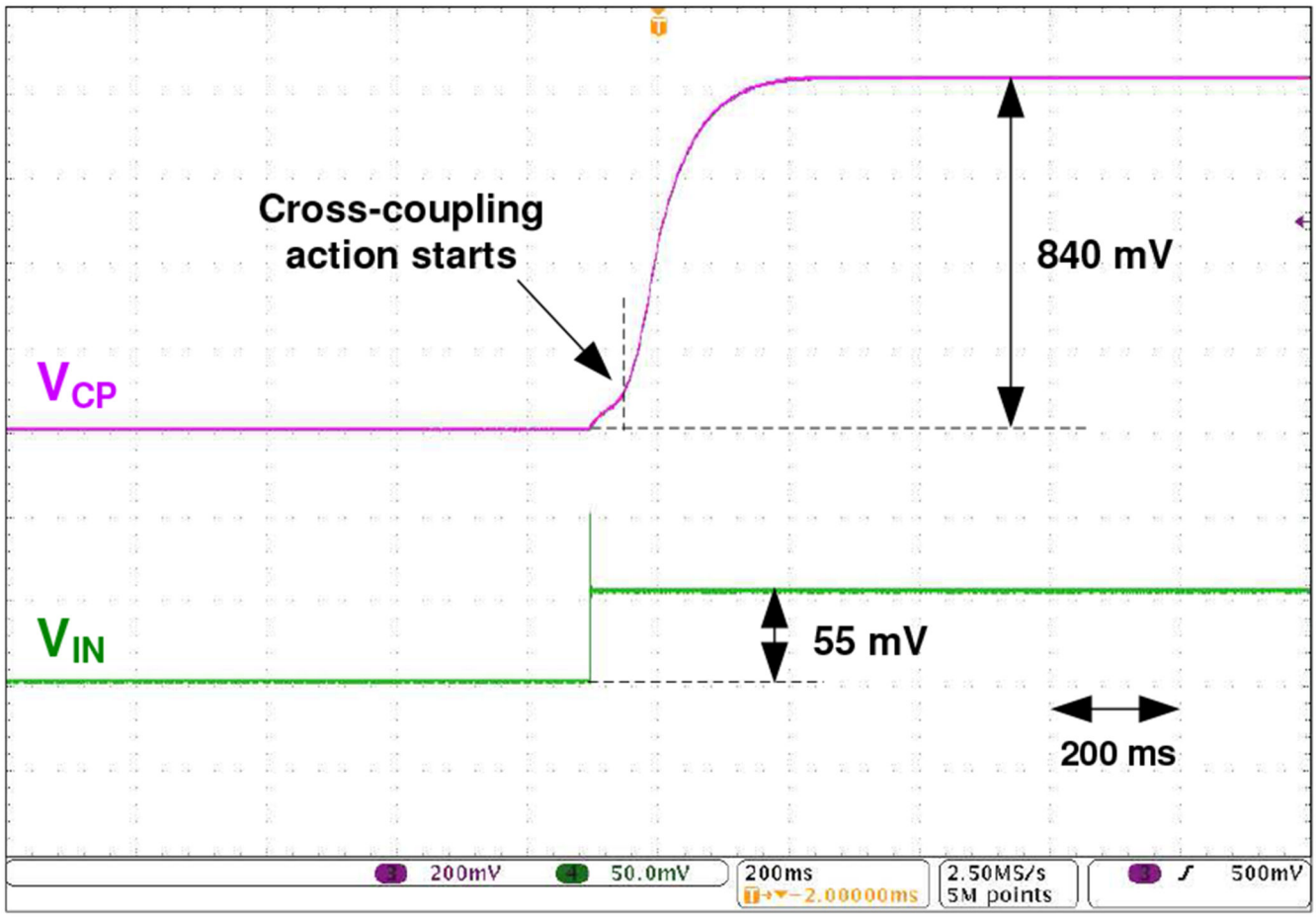

Fig. 12.

Measured transient waveform of V_{CP} (buffered off-chip) with an input supply of 55 mV.

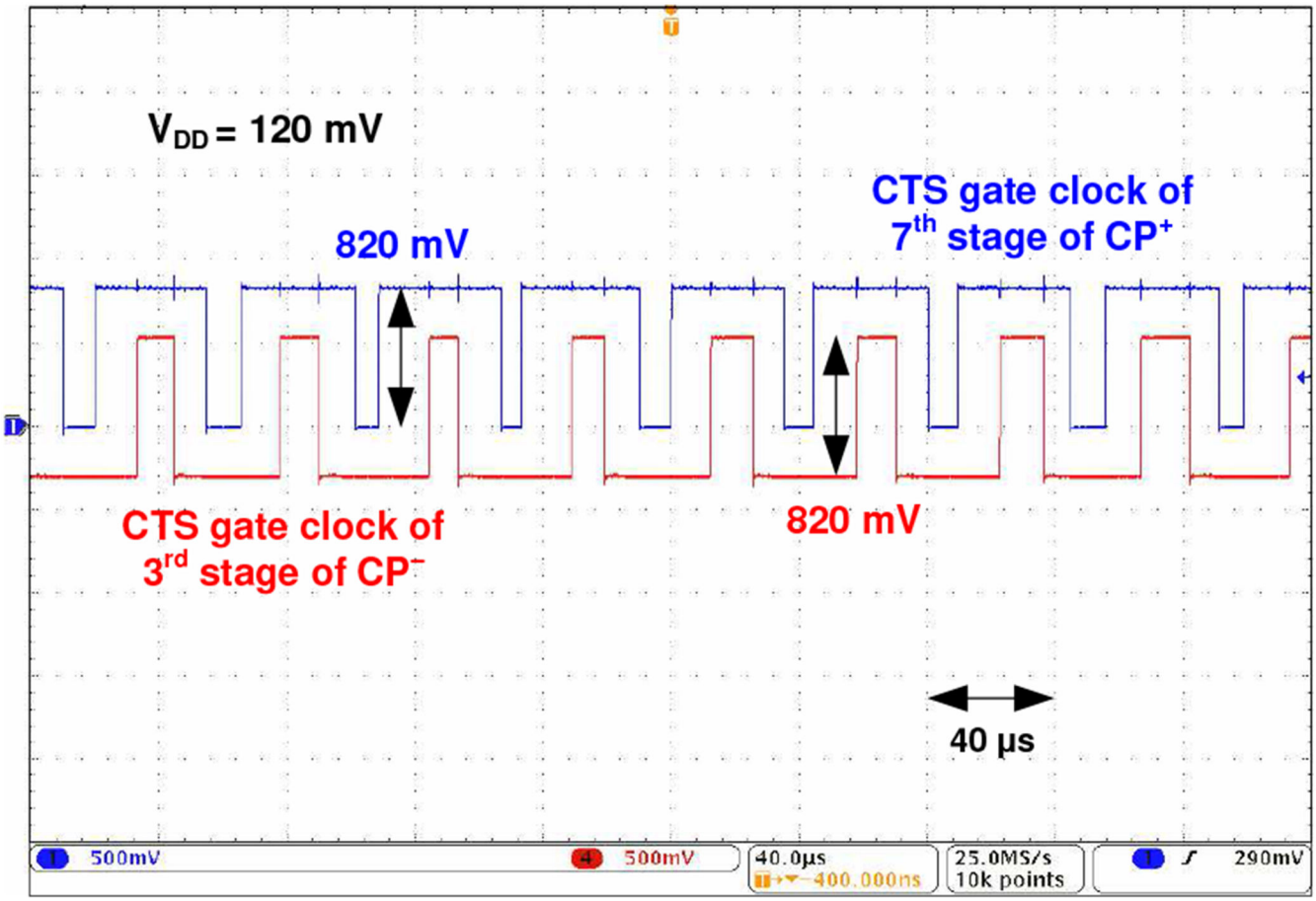

Fig. 13.
Measured non-overlapping gate clocks with boosted voltage swing.

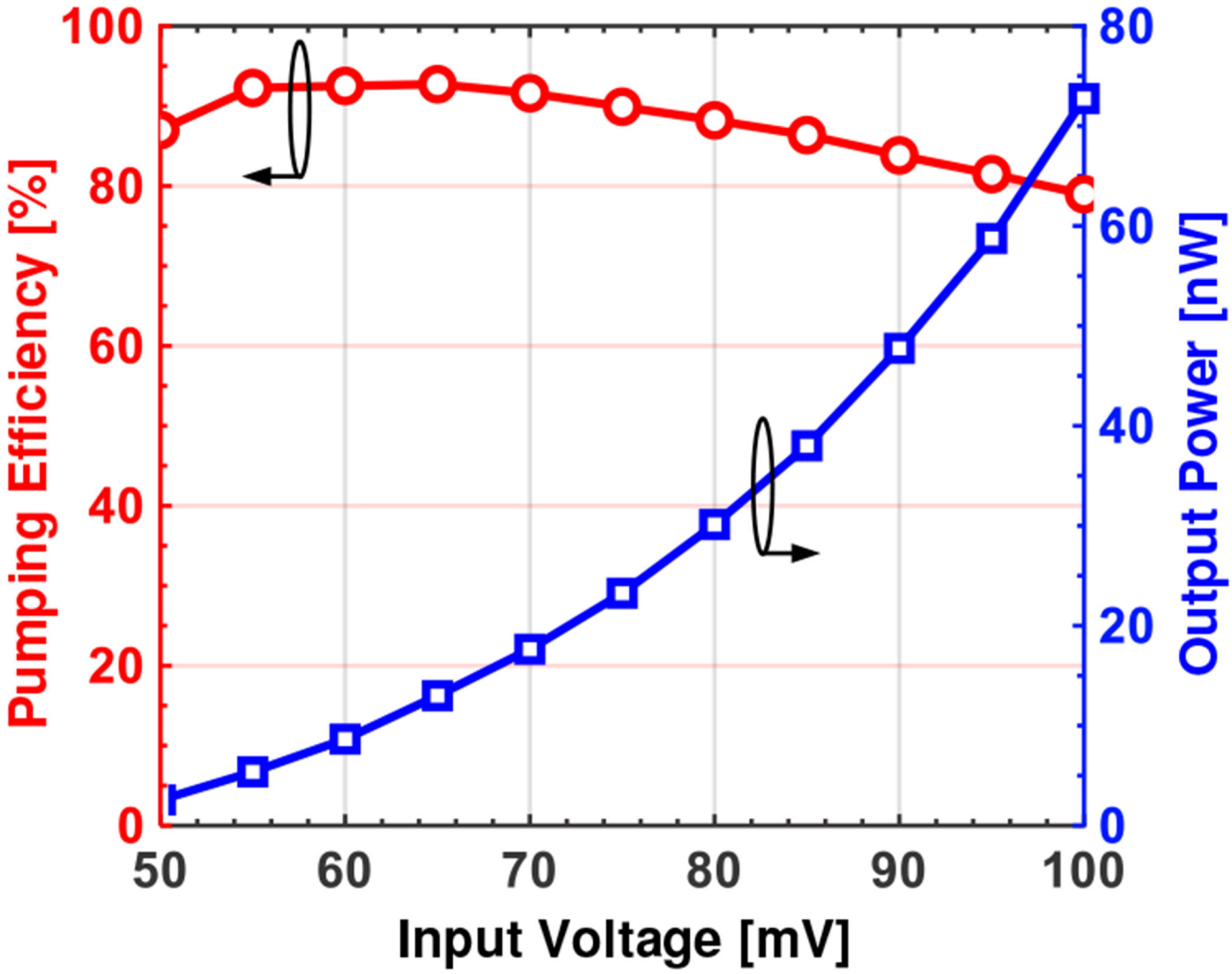

Fig. 14.
Measured pumping efficiency and output power of the charge-pump-based voltage multiplier across input voltages.

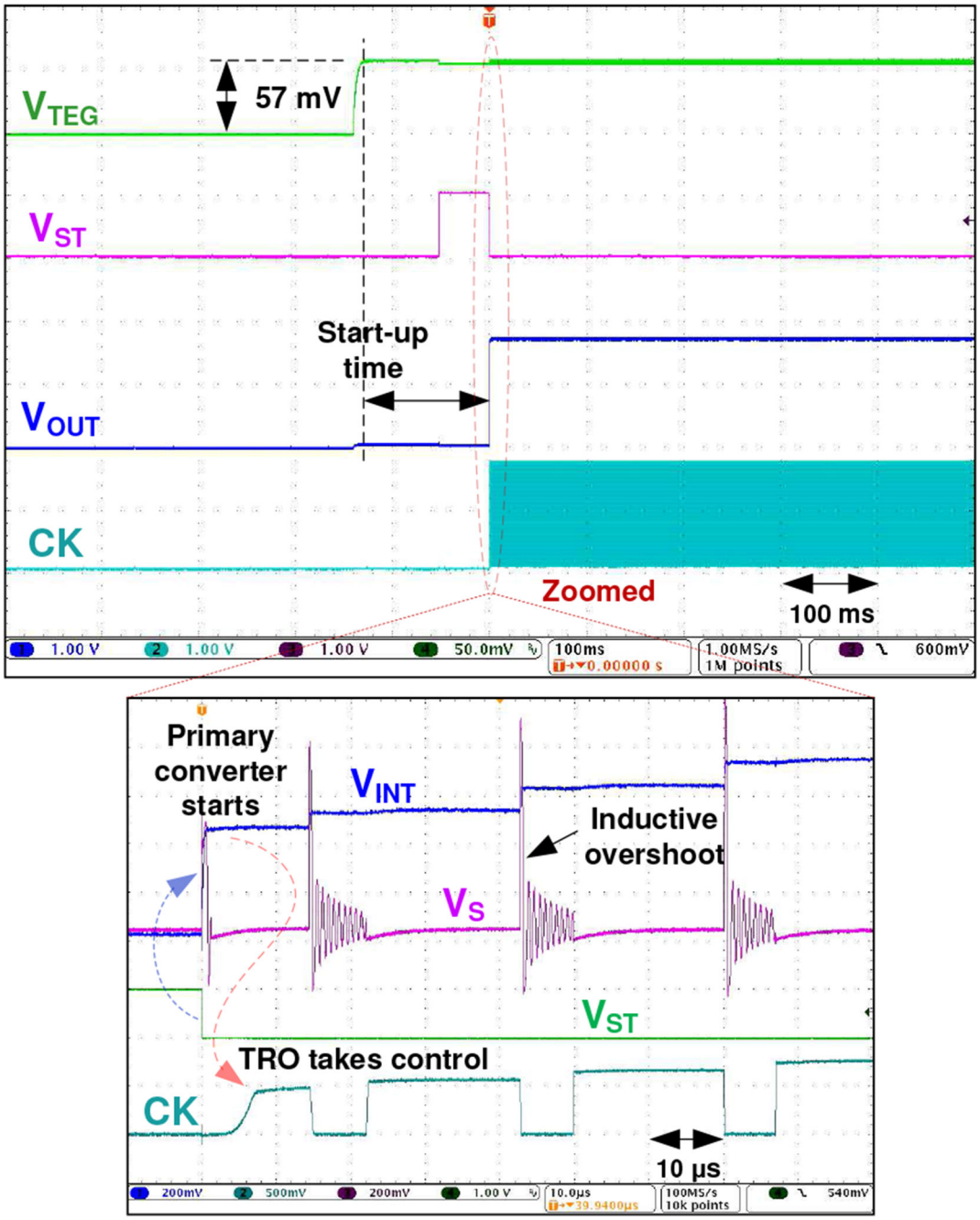

Fig. 15.

Measured start-up transient of the proposed cold-start architecture. Zoomed waveform showing triggering of the primary converter with the fast falling edge of strobe pulse, V_{ST}.

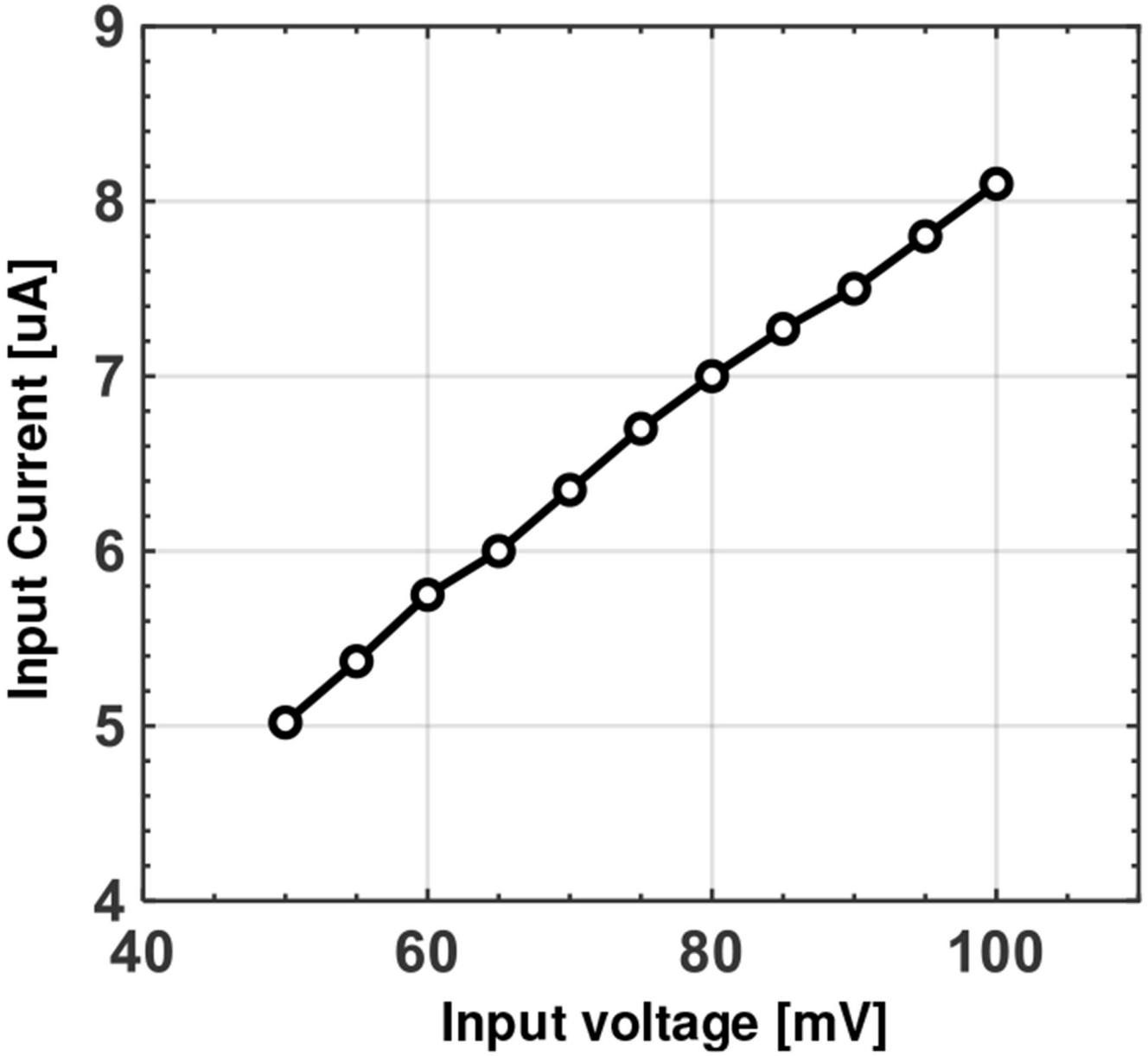

Fig. 16.
Current drawn from source by the cold-start block at various input voltages

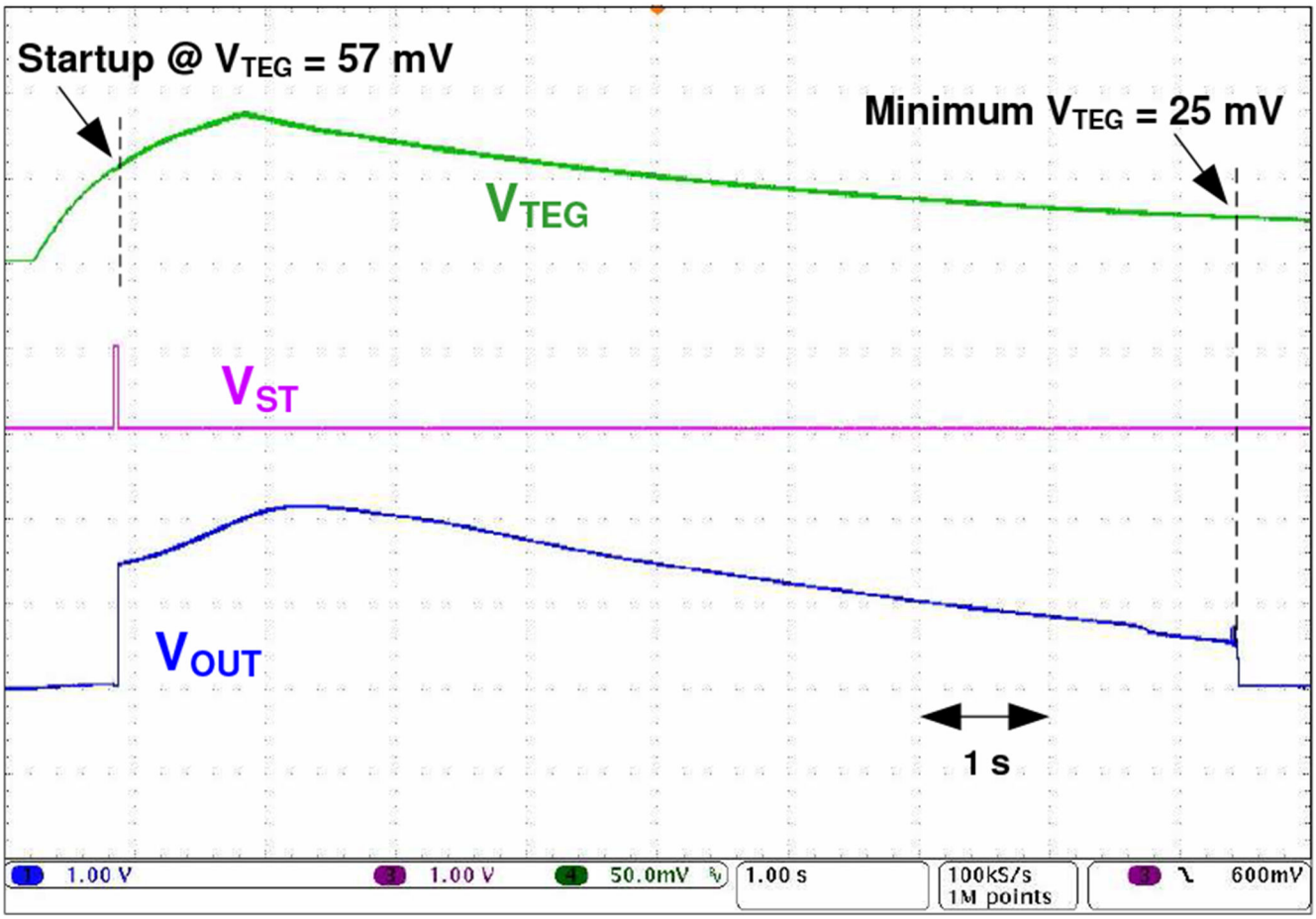

Fig. 17.
Measured transient of the boost converter with a commercial TEG.

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TABLE I

SUMMARY OF MINIMUM OPERATIONAL VOLTAGE

Block	Min. operational voltage
Start-up ring oscillator	40mV
Start-up voltage multiplier	50mV
Cold-start	57mV
Inductive boost converter	25mV (once started)

TABLE II

COMPARISON WITH STATE-OF-THE-ART COLD-START VOLTAGES

Cold-start Integration	**Off-chip**			**On-chip**				
References	JSSC'11 [4]	JSSC'13 [8]	JSSC '18 [9]	JSSC'12 [11]	JSSC '15 [5]	JSSC'16 [12]	ISSCC '19 [30]	**This work**
Process	0.35 µm	65 nm	65 nm	65 nm	0.13 µm	0.13 µm	0.18 µm	**0.18 µm**
Start-up mechanism	Mechanical vibration	LC oscillator & charge pump	Colpitts oscillator & charge pump	Ring-oscillator[(1)] & charge pump	Ring-oscillator & charge pump	Ring-oscillator & charge pump	Ring-oscillator & charge pump	**Ring-oscillator & charge pump**
Cold-start voltage	35 mV	50 mV	40 mV	95 mV	220 mV	70 mV	129 mV	**57 mV**
Start-up time	18 ms	30 ms [(2)]	22 ms [(2)]	262 ms	3.5 s [(2)]	1.5 s	150 s [(2)]	**135 ms**
Intermediate storage capacitor[(4)]	470 pF (On-chip)	– (On-chip)	4.7 nF (Off-chip)	10 nF (Off-chip)	100 uF (Off-chip)	1 nF (On-chip)	– (Off-chip)	**350 pF (On-chip)**
Boost Inductor	22 µH	4.7 µH + 100 µH	3.3 µH	6.8 µH	22 µH	>200 µH	–	**220 µH**
Additional element[(3)]	MEMS	Inductor	Inductor	None	None	None	None	**None**

[(1)] Post fabrication V_{th} trimming.

[(2)] Estimated from transient plots.

[(3)] For cold-start purpose only.

[(4)] Used during cold-start.