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# A superconducting thermal switch with ultrahigh impedance for interfacing superconductors to semiconductors

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## Abstract

A number of current approaches to quantum and neuromorphic computing use superconductors as the basis of their platform or as a measurement component, and will need to operate at cryogenic temperatures. Semiconductor systems are typically proposed as a top-level control in these architectures, with low-temperature passive components and intermediary superconducting electronics acting as the direct interface to the lowest-temperature stages. The architectures, therefore, require a low-power superconductor-semiconductor interface, which is not currently available. Here we report a superconducting switch that is capable of translating low-voltage superconducting inputs directly into semiconductor-compatible (above 1,000 mV) outputs at kelvin-scale temperatures (1K or 4 K). To illustrate the capabilities in interfacing superconductors and semiconductors, we use it to drive a light-emitting diode (LED) in a photonic integrated circuit, generating photons at 1K from a low-voltage input and detecting them with an on-chip superconducting single-photon detector. We also characterize our device's timing response (less than 300 ps turn-on, 15 ns turn-off), output impedance (greater than 1MΩ), and energy requirements (0.18fJ/$\mu$m$^2$,3.24mV/nW).

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At present, a number of quantum and neuromorphic computing architectures plan to operate at cryogenic temperatures, using superconductors as the basis of their platform [1,2] or as a measurement component[3–6]. In these architectures, semiconductor systems are often proposed as a top-level control with low-temperature passive components and intermediary superconducting electronics acting as the direct interface to the lowest-temperature stages [7]- this stratification is required because semiconductor-based amplification of small superconducting signals consumes too much power for extensive use at kelvin-scale temperatures[8–10]. As a result, the architectures require a low-power superconductor-semiconductor interface to, for example, leverage complementary metal-oxide-

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**Author contributions** A.N.M., V.V., S.M.B., and J.M.S. conceived and designed the experiments. A.N.M. performed the experiments. J.P.A. and A.G.K. analyzed and modeled the thermal properties of the device. A.N.M. and V.V. fabricated the devices. A.N.M., A.T, and S.W.N. analyzed the data.

**Competing Interests** The authors declare U.S. Patent US10236433B1

**Data availability** The data that support the findings of this study are available within the paper. Additional data are available from the corresponding authors upon reasonable request.

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semiconductor (CMOS) coprocessors for classical control of superconducting qubits[11], or as a means to drive optoelectronics from superconducting detectors. However, the ability to interface superconductors with semiconductors is a missing component in these advanced computing ecosystems.

The primary issue with interfacing superconductor electronics with semiconductor electronics is one of bandgap and impedance mismatch. The average superconductor has a bandgap almost a thousand times smaller than that of a semiconductor (e.g. 2.8 meV for Nb versus 1,100 meV for Si). Similarly, the impedances of these systems differ greatly: a typical transistor element has an effective input impedance in the $10^4$-$10^9$ range, whereas a typical superconducting logic element will have an output impedance in the 0–$10^1$ range. Due to these mismatches, it is extremely difficult to drive the high-impedance inputs of a semiconductor element to ~ 1,000 mV using ~1 mV superconductor outputs. At present, there are only two known ways to generate 1,000 mV directly from a superconducting output: connect many few-millivolt devices (such as Josephson junctions) in series[12], or allow a superconducting nanowire to latch[13].

The most successful previous attempts at creating a superconductor-to-semiconductor interface consist of a superconducting preamplifier stage combined with a semiconductor amplifier stage[9,14,15]. This approach is effective at translating signal levels, but is power-constrained. In particular, using semiconductor transistors in an amplifier configuration necessarily draws significant static power (~1 mW each), which limits scalability on a cryogenic stage. In related work, a CMOS-latch input was used after the preamplifier to limit static power[16], but this introduced the need for per-channel threshold calibration. Alternatively, it has been shown that a > 1 V output can be created from a nanowire device such as the nanocryotron[13], but using the nanocryotron as a means for semiconductor-logic interfacing has drawbacks: creation of the high-impedance state is a relatively slow hotspot-growth process along the length of the nanowire (0.25 nm/ps in NbN[17]); it is hysteretic and not able to self-reset without external circuitry; and output-input feedback is a concern, as the input and output terminals are galvanically connected[18].

In this Article, we report a monolithic switch device that can translate low-voltage superconducting inputs directly into semiconductor-compatible (>1,000 mV) outputs. The switch combines a low-impedance resistor input (1–50 Ω) with a high-impedance (>1 MΩ) superconducting nanowire-meander switch element. The input element and switching element are isolated galvanically but coupled thermally by a thin dielectric spacer (25 nm $SiO_2$). When input current is applied to the resistor, the state of the entire nanowire-meander is switched from superconducting to normal. The input induces an extremely large impedance change in the output: from 0 Ω to >1 MΩ (Fig. 1). The power cost of inducing this change is surprisingly small when compared to existing methods, and crucially it can be operated in a non-hysteric (that is, self-resetting) regime. As a demonstration of a superconductor-semiconductor interface, we have used the switch to drive an LED in a photonic integrated circuit, generating photons at 1 K from a low-voltage input and detecting them with an on-chip superconducting single-photon detector.

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## High-impedance superconducting switch

Our device consists of a 3-layer stack (Fig. 1b). On the top of the stack is a resistor made from a thin film of normal metal with a small resistance (1–50 Ω). On the bottom of the stack is a meandered nanowire patterned from a superconducting thin film. The nanowire layer acts as a high-impedance, phonon-sensitive switch, while the resistor layer is used to convert electrical energy into Cooper-pair-breaking phonons. Like related low-impedance thermal devices[19,20], between these two layers is a dielectric thermal spacer that has two purposes: thermally coupling the resistor layer to the nanowire layer, and electrically disconnecting the input (resistor) from the output (nanowire switch). The device has four terminals total, with two of the terminals connected to the resistor and two of the terminals connected to the nanowire (Fig. 1). Fabrication details are available in the Methods section.

The device begins in the “off” state where there is no electrical input to the resistor and the nanowire has a small current-bias. To transition to the “on” state, a voltage or current is applied to the input terminals of the resistor and thermal phonons are generated. The thin dielectric carries phonons generated from the resistor to the nanowire. Phonons with energy >2Δ break Cooper pairs within the nanowire, destroying the superconducting state of the nanowire. Once the superconducting state has been completely destroyed in the entire nanowire, the device is in the on state.

Analogously, this process can be described in terms of an effective temperature: the dielectric layer is thin enough that the phonon systems between the nanowire and the resistor are tightly coupled, meaning the phonon temperature in the nanowire is closely tied to the temperature of the resistor. When enough electrical power is delivered to the resistor, the nanowire is driven above its critical temperature and becomes normal, jumping from 0 Ω to >1 MΩ. Once the device has switched, current is then driven into the high-impedance output load and a large voltage can be generated.

When characterizing a switch, of primary importance is its on and off resistance. We measured the steady-state behavior of the switch by applying power to the resistor inputs of several devices and measuring the nanowire resistance with an AC resistance bridge. As can be seen in Fig. 1, each device remained at zero resistance until a critical surface power $P_c$ was reached. When more than $P_c$ was applied to the resistor, the resistance of the underlying nanowire increased rapidly, ultimately saturating at the normal-state resistance of the device. One potential concern was that phonons from the resistor could escape in-plane (e.g. out through the thick gold leads), resulting in wasted power. This type of edge power loss would scale with the length of the edge, and so we measured $P_c$ for devices of several sizes. However, by dividing each device’s $P_c$ by its active area $A$, we found that the devices had critical surface power densities $D_c = P_c/A$ of 21.0 ± 0.6nW/μm$^2$. This means power loss through edge effects (e.g. along the substrate plane or into the gold contacts) did not play a role at the scale of device measured here. Additionally, through thermal modeling, we also found that worst-case thermal crosstalk between adjacent devices would be negligible if the devices were separated by a few micrometers (further details on lateral heat transport and crosstalk are available in the Supplementary Information). As shown in Fig. 1c, the resistance of each device continues to increase beyond $P_c$-this was likely due to non-uniform

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dissipation within the resistor element creating local temperature variation. Note that performing this measurement with a low-power measurement technique (such as an AC resistance bridge) was critical in order to limit Joule heating from current passing through the nanowire element. In this experiment, we applied a maximum of 10 nA (~100 pW) in order to guarantee that the nanowire was not heated by the measurement process. The 4.5-nm-thick tungsten silicide (WSi) film used for the nanowires had a $T_c$ of 3.4 K, and all measurements were taken at a base temperature of 0.86 K.

## Driving a cryogenic LED

As a means of demonstrating the superconductor-semiconductor interface, we used the switch to dynamically enable a cryogenic LED in a photonic integrated circuit (PIC) using only a low-level input voltage. Shown in Fig. 2, the output from the switch was wirebonded to a PIC that had an LED which was waveguide-coupled to a superconducting nanowire single-photon detector (SNSPD). The switch translated the 50 mV input (Fig. 2b) signal into 1.12 V at the output, enabling and disabling the LED in a free-running mode. Photons produced by the LED were coupled via waveguide into the detector, producing clicks on the detector output (Fig. 2c). The switch was driven with 94.0 μW of input power (55.9 nW/μm$^2$, well above $D_c$), generating an on-state resistance of approximately 400 kΩ. We note these particular LEDs had a low overall efficiency (~$10^{-6}$ as characterized in Ref. [21]), and so a large LED input power was necessary to generate the handful of photons per period. The large LED power requirement necessitated wide nanowires (1 μm wide for this experiment) to carry the requisite current, and so the device area and input power scaled proportionally. Steady-state behavior of the circuit is shown in Fig. 2d, which characterizes the detector response with the switch input power above and below the $D_c$ threshold. We additionally verified that the counts measured on the detector were in fact photons generated by the LED-not false counts due to sample heating or other spurious effects-by reducing the LED bias below threshold and observing no clicks on the detector output, and also by quadrupling the switching input power and observing no heating-induced change in count rate.

## Transient and sub-threshold response

We also characterized the transient properties of the device when driving high-impedance loads by placing a 8.7 kΩ on-chip resistor at the output of the device. In this experiment, we applied voltage pulses to the resistor input with a pulse generator and measured the device output, while applying a current bias to the nanowire either below the retrapping current (Fig. 3, red data), or near the critical current (Fig. 3, cyan data). As seen in the circuit diagram of Fig. 3, an output voltage could only be generated when the switch reached a significant resistance ($\ll$1kΩ) allowing us to probe the impedance transition of the device. The results from this experiment, shown in Fig. 3, showed that the device could turn-on from its low-impedance state to its high-impedance state below 300 ps, characterized by a power-delay product on the order of ~100 aJ per square micrometer of device area.

Crucially, the impulse-response also demonstrates that this device can self-reset. As highlighted in Fig. 3a, when the nanowire is biased below the retrapping current, it becomes non-hysteretic and returns to the zero-voltage (superconducting) state after the input is

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turned off. The logic follows simply: below the retrapping current, the self-heating caused by the nanowire bias current does not generate enough power to keep the wire above $T_c$. Thus, when the additional heating from the resistor is removed, the nanowire is forced back into the superconducting state-it does not get stuck in the on-state or "latch." This non-latching property is in contrast to existing thin-film nanowire devices previously developed, and is critical to guarantee device reset in unclocked systems where the input bias to the devices is not periodically turned off. We note that even in this regime, there is still a thermal recovery time constant for the device to transition from the normal (on) to superconducting (off) state. We found that fall time was on the order 10 ns, which is consistent with the thermal recovery time constants previously reported for WSi. Additionally, it should be noted that although the nanowire fabricated here has a very high kinetic inductance, the L/R time constant of the switch-that could potentially limit the rise time of the current output-is not a limiting factor. When the device transitions from low-to high-impedance, the expected $L_k/R_s$ is equal to 0.39 ps.

To better understand the response of the device below the critical surface power density $D_c$, we measured the nanowire critical current as a function of power applied to the resistor. The result of this characterization is shown in Fig. 4. For each datapoint, we applied a fixed amount of electrical power to the input resistor and measured the critical current of the nanowire several hundred times, taking the median value as $I_c(P)$. We then extracted an effective temperature for the nanowire by numerically inverting the Ginzburg-Landau relation $I_c(t) = I_{c0}( 1 - t^2)^{3/2}(1 + t^2)^{1/2}$ where $I_{c0}$ was the critical current at zero applied power and t was the normalized temperature of the device $T/T_c$ (for this material, the $T_c$ was measured to be 3.4 K). Note the non-uniform heating causes the critical current to reach zero at 8 nW/μm$^2$-well before the jump in resistivity shown in Fig. 1c at $D_c$ (21 nW/μm$^2$)-because localized heat can suppress $I_c$ but the resistivity measurement accounts for the state of every part of the nanowire. The data in Fig. 4 show that there is a nonlinear relationship between the nanowire temperature and the applied heating power. We note that these nanowires are likely constricted due to current crowding[22] at the bends, and as a result may obfuscate changes in Ic at low powers in Fig. 4.

## Thermal transport modeling

A complete model of the dynamics of the device requires an investigation of the nonequilibrium dynamics of the electron and phonon systems of the heater, dielectric spacer, and nanowires. While a full description is beyond the scope of this paper, we find that an approximation using ballistic phonon transport is sufficient for describing the main experimental results. Given that the bulk mean-free-path of phonons in $SiO_2$ is on the order of 1 μm at 2.5 K, we assume that phonons escaping from the heater travel through the dielectric without scattering and either interact with the nanowire or continue unimpeded to the substrate[23]. Within this model and under the simplifying assumption of equilibrated electron and phonon systems in the nanowire at temperature $T_{WSi}$, the energy balance equation of the nanowire is given by

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$$\left(C_e(T_{WSi}) + C_{ph}(T_{WSi})\right)d\ f\frac{\partial T_{WSi}}{\partial t} = f\chi_{abs}P_h - \Sigma\left({T_{WSi}}^4 - {T_{sub}}^4\right) \quad (1)$$

where $C_e(T_{WSi})$ is the BCS electron heat capacity, $C_{ph}(T_{WSi})$ is the lattice heat capacity, $d$ is the nanowire thickness, $f$ is the nanowire fill factor, $\chi_{abs}$ is the fraction of energy incident on the nanowire which is absorbed, Σ describes the magnitude of phonon energy flux from the nanowire to the substrate per unit area, and $P_h$ is the power dissipated by the heater per unit area. For a WSi device with $d$ = 4.5 nm, $f$ = 0.5, sheet resistance $\rho_{sq}$ = 590Ω/sq, $T_c$ = 3.4 K, and using values from the literature [24,25] for the diffusion coefficient $D$ =0.74 $cm^2/s$ and specific heat ratio $C_e(T_c)/C_{ph}(T_c) \sim 1$, the parameters $\chi_{abs}$ and Σ are chosen to fit the turn-on delay vs dissipated power results of Fig. 3b. The calculated curves show the turn-on delay for temperature thresholds of 2.5 K and 3K, where temperature threshold refers to the minimum temperature required at a given bias current to switch the device. The two remaining free parameters were fitted to be $\chi_{abs}$ = 0.02, and Σ = 0.7 $W/m^2K^4$. This value of Σ corresponds to nonbolometric phonon bottlenecking at the $WSi/SiO_2$ interface with a conversion time from the non-escaping to escaping group of phonons with a magnitude over 1 ns, which is consistent with experiment [24]. For comparison, the estimation of the parameter $\chi_{abs}$ based on the solution of ballistic phonon transport in the nanowire is provided in the Supplementary Information.

While the basic principle of operation is applicable to materials with higher critical temperatures, the details of the heat transfer between heater and superconductor would change. The heat capacity of materials increases with temperature, so more energy will be required to heat the superconductor to its current dependent critical temperature. With a larger superconducting gap Δ, higher-energy phonons are required to break Cooper pairs. At the same time, higher temperature operation means that phonons from the heater will have higher energies, and shorter mean-free-paths in the dielectric, which will lead to additional scattering and absorption. It is currently unclear if this will make heat transfer less efficient due to the additional scattering, or more efficient by keeping energy trapped in the local area of the nanowire.

A useful figure of merit for these devices is $P_V$, the output voltage generated per unit input power while the switch is on. Due to proportionalities between the device resistance and area, and also between nanowire width and $I_c$, this figure of merit is area-and shape-independent-it depends only on the materials used and the nanowire configuration. We calculated $P_V$ by first noting that the power required to heat the full area $A$ of a given device was $D_cA$. For a device with nanowires of width $w$, thickness t, and fill-factor $f$, the amount of switching resistance generated in that area is $R_sfA/w^2$, where $R_s$ is the nanowire normal-state sheet resistance. For the WSi material used here, the bias current density $J$ was $1.6\times10^9$ $A/m^2$ (non-latching) or $7.2\times10^9$ $A/m^2$ (latching), and $R_s$ was 590 Ω/sq. The resulting voltage generated per unit power is then $R_sfJ/w^2D_c$ (thus, independent of device area), and so for the devices characterized in Fig. 1, $P_V$ was 0.72 mV/nW (non-latching) or 3.24 mV/nW (latching).

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One potential area of concern when using this device as a switch is the power usage from current-biasing the device. Typically, a current-bias capable of driving high voltages require a large amount static energy dissipation: when using a resistor or MOSFET-based current source as a current bias, to achieve a maximum voltage of $V_{max}$ will generally require $I_b V_{max}$ of static power. However, for these devices a better approach will be to use inductive biasing to generate the high-impedance current bias. Superconducting thin films such as the one used here lend themselves particularly well to the generation of large inductances in compact areas, due to their large kinetic inductance. For instance, to generate a 200 mV swing on a CMOS input capacitance of 5 fF requires a bias current of 50 μA being carried by an 160 nH inductor-a trivial amount of inductance to generate with a superconducting nanowire. More importantly, the inductor can be charged only when needed, using a low-voltage superconducting element such as a Josephson junction.

## Conclusions

Our superconducting thermal switch has a number of favourable features as a communications device between superconducting and semiconducting elements: it provides switch impedances of more than 1MQ, input-output isolation, low turn-on time, and low-power operation with zero passive power required. Even with the reset-time limitations presented by thermal recovery, this switch has particular applicability for driving optoelectronics on a cryogenic stage such as LEDs or modulators. In applications such as quantum photonic feed-forward experiments or low-power neuromorphic hardware[26], clicks from efficient superconducting detectors need to be converted to optoelectronic-compatible signals, and a nanosecond-scale thermal recovery is acceptable as long as the initial response is fast. We note for these types of applications, it may be best to configure the device geometry to minimize propagation delay-the propagation delay for powering an LED to 1 V will be much smaller if 1 mA is driven across a switch of 1 kΩ, rather than driving 1 μA across 1 MΩ. It may also be helpful to drive the device with another superconducting three-terminal device[27], as this can provide a purely non-resistive superconducting input and be fabricated in the same step as the nanowire meander.

Looking forward, there are a number of practical methods to enhance the operation of this device, depending on what tradeoffs are acceptable in a given application. The simplest would be to use multiple layers of nanowire: the on-resistance could, for example, be effectively doubled by adding an additional nanowire meander underneath the first (at some minor turn-on energy cost). If power usage is a concern, the on-state power requirements could be decreased by placing the device on a membrane. This would greatly increase the thermal resistance, reducing overall energy cost at the cost of increasing the thermal turn-off time. For higher operational frequencies, a different nanowire material could be used (for example, NbN for a ~1 ns thermal reset time [28]). Finally, this device does not fundamentally need to be a thermal device: any method of inducing a phase change in a superconducting film – for instance, using an electric-field induced superconductor-to-insulator transition [29] – could be operated equivalently.

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## Methods

### * Fabrication details

Fabrication began with a clean thermal oxide wafer (150 nm $SiO_2$ on Si). WSi was sputtered uniformly over the entire wafer to a thickness of 4.5 nm, and afterwards-but before breaking vacuum-a thin capping layer (1–2 nm) of amorphous Si was also sputtered on top. (WSi was chosen primarily for its high practical fabrication yield in our lab-other highly-resistive thin-film superconductors should work equivalently, although with potential power/thermal tradeoffs discussed in the thermal modeling section.) Next, contact pads for the superconducting layer were patterned using a liftoff process and deposited by evaporating 5 nm Ti / 100 nm Au / 5 nm Ti. We then patterned and etched the WSi layer to form the nanowires. Afterwards, we sputtered the whole wafer with 25 nm of $SiO_2$. $SiO_2$ was chosen because of its compatibility with WSi – in past experiments we had found that SiO2 deposition did not negatively impact the superconducting parameters of the WSi layer ($T_c$, $I_c$, etc.). Using a liftoff process, we then fabricated the resistor layer by evaporating 15 nm of PdAu. Lastly, the low-resistance contact pads were deposited using another liftoff process, evaporating 5 nm Ti followed by 100 nm of Au.

## Supplementary Material

Refer to Web version on PubMed Central for supplementary material.

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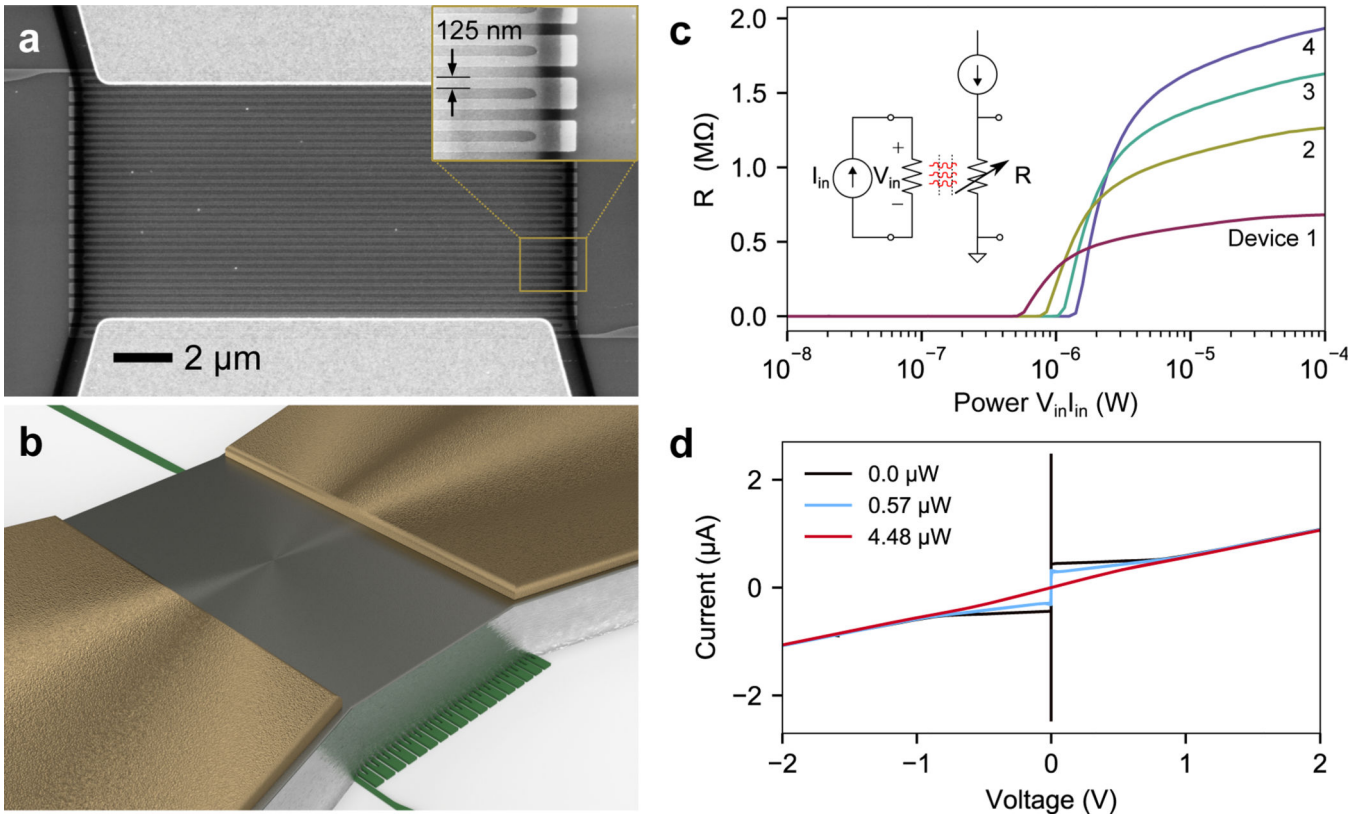


**Figure 1.**

High-impedance superconducting switch overview. (a) Scanning electron micrograph of one device (inset) closeup of the nanowire meander. (b) Schematic illustration of the device, showing the three primary layers (resistor, dielectric, and nanowire) as well as contact pad geometry. (c) Resistance data versus input power for several devices and circuit schematic for resistance measurement. Maximum resistance is proportional to device area, with devices 1–4 having areas 44, 68, 92, and 116 $\mu m^2$. (d) I-V curve of one device for three different input powers.

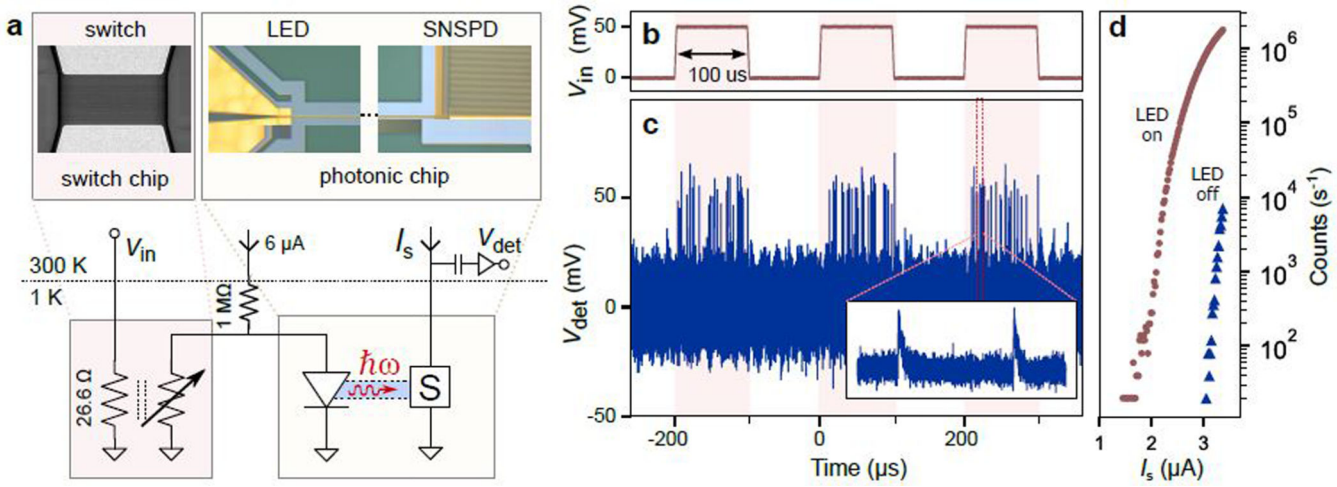


**Figure 2.**

Driving a photonic integrated circuit at 1 K. (a) Schematic and circuit setup for powering a cryogenic LED with the switch and reading out the generated light using a waveguide-coupled single-photon detector. (b,c) Switch input and detector output versus time. When $v_{in}$ is high, photons generated by the LED are transmitted via waveguide to a superconducting nanowire single-photon detector, producing detection pulses. (inset) Zoom-in of the detector output pulses. (d) Detector count rates for the experiment with the LED on (red) and off (blue).



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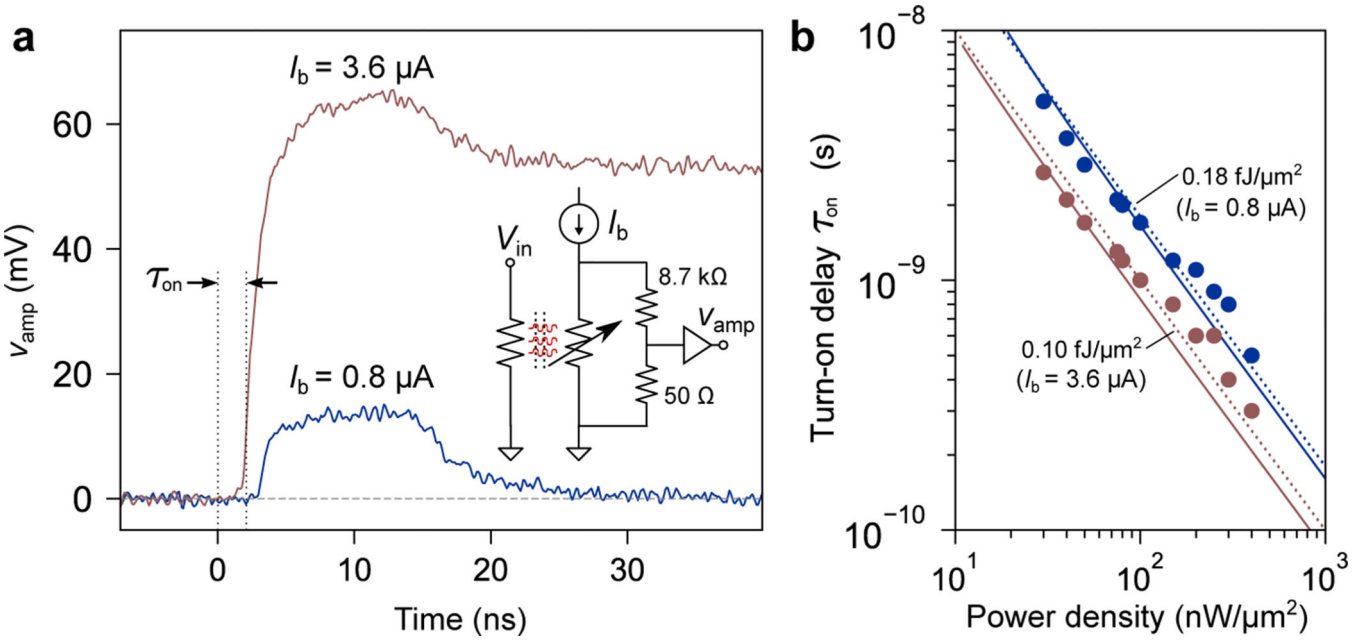


**Figure 3.**

Driving an 8.7 kΩ load using the switch. (a) Output produced by a 10-ns-wide square pulse to the heater with input surface power density $D = 50$ nW/μm$^2$, highlighting the latching and non-latching regimes. Trace data taken with a 1 GHz bandwidth-limited amplifiers and oscilloscope. (b) Turn-on delay $\tau_{on}$ versus applied input power when the nanowire is biased below the retrapping current (blue) and near $I_c$ (red). The solid lines are fits generated by the ballistic phonon transport modeling, and the dotted lines are constant-energy per unit area curves corresponding to 0.18 fJ/μm$^2$ (blue) and 0.10 fJ/μm$^2$ (red).

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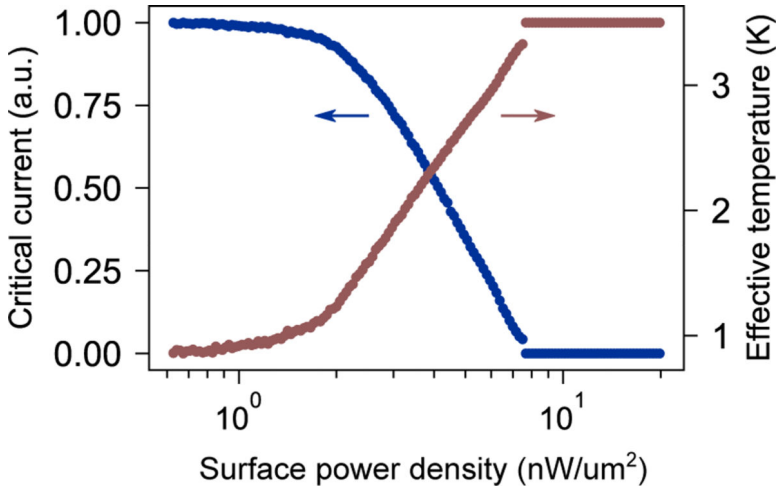


**Figure 4.**

Critical current and inferred temperature versus input power density. As the input power density is increased, the effective temperature of the meander rises, and its critical current is reduced. The small discontinuity is an experimental artifact from measuring very small critical current values.