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ZrO_2 Ferroelectric Field-Effect Transistors Enabled by the Switchable Oxygen Vacancy Dipoles

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Abstract

This paper investigates the impacts of post-rapid thermal anneal (RTA) and thickness of ZrO_2 on the polarization *P* and electrical characteristics of TaN/ZrO_2/Ge capacitors and FeFETs, respectively. After the RTA ranging from 350 to 500 °C, TaN/ZrO_2/Ge capacitors with 2.5 and 4 nm-thick amorphous ZrO_2 film exhibit the stable *P*. It is proposed that the ferroelectric behavior originates from the migration of the voltage-driven dipoles formed by the oxygen vacancies and negative charges. FeFETs with 2.5 nm, 4 nm, and 9 nm ZrO_2 demonstrate the decent memory window (MW) with 100 ns program/erase pulses. A 4-nm-thick ZrO_2 FeFET has significantly improved fatigue and retention characteristics compared to devices with 2.5 nm and 9 nm ZrO_2. The retention performance of the ZrO_2 FeFET can be improved with the increase of the RTA temperature. An MW of ~ 0.46 V is extrapolated to be maintained over 10 years for the device with 4 nm ZrO_2.

Keywords: FeFET, ZrO_2, Memory, Germanium, Amorphous

Background

Doped poly-HfO_2 ferroelectric field-effect transistors (FeFETs) have attracted considerable interest in the non-volatile memory (NVM) applications due to their CMOS process compatibility [1]. Although the decent electrical performance has been demonstrated in doped HfO_2-based FeFETs [2], some fundamental limitations still plague their practical applications, including the high thermal budget of 500 °C annealing required to form orthorhombic crystal phases and the undesired leakage current along the grain boundaries with the scaling down of ferroelectric thickness. Ferroelectricity has been widely observed in a variety of different materials, e.g., Sb_2S_3 nanowires [3], $GaFeO_3$ film [4], $LaAlO_3$-$SrTiO_3$ film [5], and amorphous Al_2O_3 containing nanocrystals [6, 7]. Recently, we reported the FeFETs with partially crystallized ZrO_2 gate insulator functioning as NVM and analog synapse [8]. Although the ZrO_2 transistors exhibited decent electrical performance with the thinner thickness compared to the reported doped HfO_2, the underlying mechanism for the ferroelectricity in ZrO_2 film remains unclear. It is critical and important to elucidate the origin of the switchable polarization *P* for evaluating the performance limit of ZrO_2 FeFETs.

In this work, TaN/ZrO_2/Ge FeFETs with 2.5 nm, 4 nm, and 9 nm-thick insulators are fabricated. The switchable *P* in TaN/ZrO_2/Ge capacitor is proposed to originate from the migration of voltage-driven oxygen vacancies and negative charges. The impacts of ZrO_2 thickness and the post-rapid thermal annealing (RTA) on the *P* of TaN/ZrO_2/Ge and the memory window (MW), endurance, and retention characteristics of FeFETs are investigated.

Methods

FeFETs with ZrO_2 gate insulator were fabricated on 4-in. n-Ge(001) substrate using a similar process in [8, 9].

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After the pre-gate cleaning in the diluted HF (1:50) solution, Ge wafers were loaded into an atomic layer deposition (ALD) chamber. ZrO_2 films with thicknesses of 2.5 nm, 4 nm, and 9 nm were deposited at 250 °C using TDMAZr and H_2O as precursors of Zr and O, respectively. A 100-nm-thick TaN gate electrode was deposited by reactive sputtering. After the gate electrode formation, the source/drain (S/D) regions were implanted by BF_2^+ at a dose of 1×10^{15} cm^{-2} and an energy of 20 keV. A total of 15 nm nickel (Ni) S/D contacts were formed by a lift-off process. Finally, the RTA at 350, 450, and 500 °C for 30 s was carried out.

Figure 1 a shows the schematic of the fabricated transistor. Figure 1b–d shows the transmission electron microscope (TEM) images of the TaN/ZrO_2/Ge samples with 2.5, 4, and 9 nm-thick ZrO_2, respectively. All the samples underwent an RTA at 500 °C for 30 s. The 2.5 nm ZrO_2 sample remains an insulator film after the annealing. For the 4 nm sample, although some nanocrystals are observed, ZrO_2 maintains to be an amorphous layer. While full crystallization occurs for the 9 nm ZrO_2 film. Notably, an interfacial layer (IL) of GeO_x exists between the ZrO_2 and Ge channel region, although it is too thin to be observed in the TEM images.

Results and Discussion

Figure 2 shows the P vs. voltage (V) curves for the TaN/ZrO_2/Ge capacitors with different ZrO_2 thicknesses and different annealing temperatures. The solid lines with different colors represent the minor loops with various sweeping voltage range (V_{range}). The measurement frequency is 1 kHz. The 2.5 nm and 4 nm ZrO_2 devices can exhibit stable ferroelectricity after an RTA at 350 °C. Figure 3 plots the remnant P (P_r) as a function of the sweeping V range curves for the capacitors annealed at various temperatures.

Figure 3 shows the comparison of P_{max} as a function of V_{range} for the TaN/ZrO_2/Ge capacitors with the different ZrO_2 thicknesses and the various RTA temperatures. For the 4 nm ZrO_2 devices, as the annealing temperature increases from 350 to 450 °C, a larger V_{range} is required to obtain a fixed P_{max}. This is attributed to the fact that the higher annealing temperature produces the thicker interfacial layers (ILs) between at Ge/ZrO_2 and ZrO_2/TaN interfaces, leading to a larger unified capacitance equivalent thickness (CET). For the 2.5 nm ZrO_2 capacitors, the sample with 500 °C annealing has a lower V_{range} than does the 350 °C annealing sample with the same P_{max}. Although the ILs get thicker with the increased RTA temperature, some ZrO_2 was consumed by the oxygen scavenging and interdiffusion at the interface. For the very thin ZrO_2 device, the latter is dominant. Compared to the 2.5 nm ZrO_2 capacitor, a much larger V_{range} is required to achieve a similar P_{max}. However, the 9 nm ZrO_2 capacitor does not exhibit the higher V_{range} in comparison with the 4 nm device. This is due to the crystal ZrO_2 that has a much higher κ value than does the amorphous film, which significantly reduces the CET of the 9 nm device.

Figure 4a shows the extracted evolution of the positive and negative P_r, denoted by P_r^+ and P_r^-, respectively, for the 4 nm-thick ZrO_2 capacitors with RTA at different temperatures over 10^6 sweeping cycles measured at 1

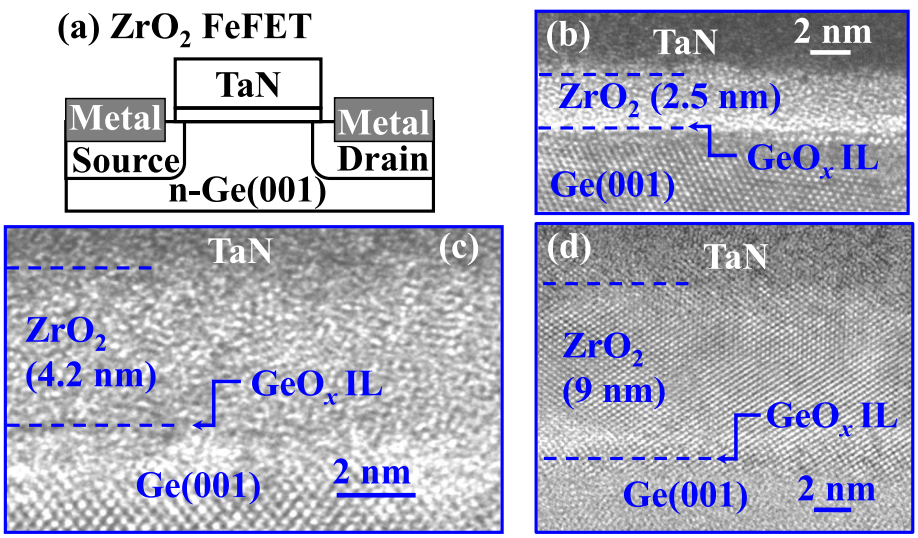

Fig. 1 **a** Schematic of the fabricated TaN/ZrO_2/Ge FeFET. **b**, **c**, and **d** HRTEM images of the TaN/ZrO_2/Ge stacks with different ZrO_2 thicknesses. The samples underwent an RTA at 500 °C for 30 s

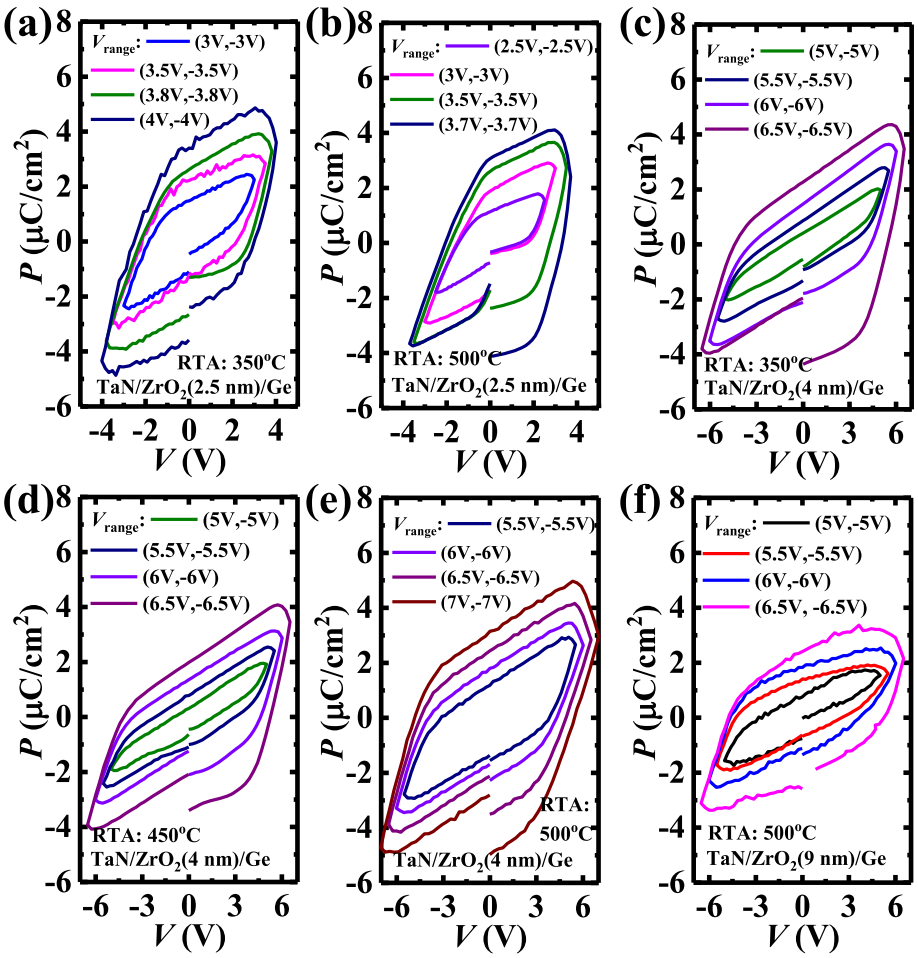

Fig. 2 Measured *P* vs. *V* characteristics of the TaN/ZrO_2/Ge capacitors with different ZrO_2 thicknesses and various annealing temperatures

kHz. Devices annealed at 350 °C and 450 °C exhibit the obvious wake-up effect. No wake up or imprint is observed for the 4 nm ZrO_2 ferroelectric capacitor underwent annealing at 500 °C. Figure 4b compares the P_r as a function of sweeping cycles for the devices with the different ZrO_2 thicknesses. The 4 nm ZrO_2 ferroelectric capacitor achieves improved stability of P_r endurance compared to the 2.5 nm and 9 nm devices during the 10^6 endurance test.

The switching *P* is observed in amorphous ZrO_2 capacitance, and it is inferred that the mechanism must be different from that of the reported doped poly-HfO_2 ferroelectric films. We propose that the underlying mechanism for ferroelectric behavior is related to the oxygen vacancy dipoles. It is well known that, as TaN metal deposited, the Ta oxygen scavenger layers will increase the oxygen vacancy concentration inside ZrO_2 [10]. Oxygen vacancies also appear at the ZrO_2/Ge interface. Figure 5 shows the schematics of the switchable *P* in TaN/ZrO_2/Ge originating from the migration of oxygen vacancies and negative charges to form the positive and negative dipoles. It is speculated that the negative charges in ZrO_2 are related to the Zr vacancy [11], which is similar to those in Al_2O_3 film [12]. The migration of the voltage-driven oxygen vacancies has been widely demonstrated in resistive random-access memory devices [13, 14]. Notably, this is the first demonstration of three-terminal non-volatile transistors dominated by the voltage-driven oxygen vacancies.

The *P*-*V* hysteresis enables the ZrO_2 FeFETs to obtain a large and stable MW for the embedded NVM (eNVM) applications. Figure 6 shows the measured I_{DS}-V_{GS} curves of 2.5, 4, and 9 nm ZrO_2 FeFETs for the two polarization states with 1 μs program/erase (P/E) conditions. The transistors were annealed at 500 °C. Program (erase) operation is achieved by applying positive (negative) voltage pulses to the gate of the ZrO_2 FeFETs, to raise (lower) its threshold voltage (V_{TH}). V_{TH} is defined as V_{GS} at 100 nA·W/L, and MW is defined as the maximum change in V_{TH}. All the FeFETs with various ZrO_2 thicknesses have the MW above 1 V with 1 μs

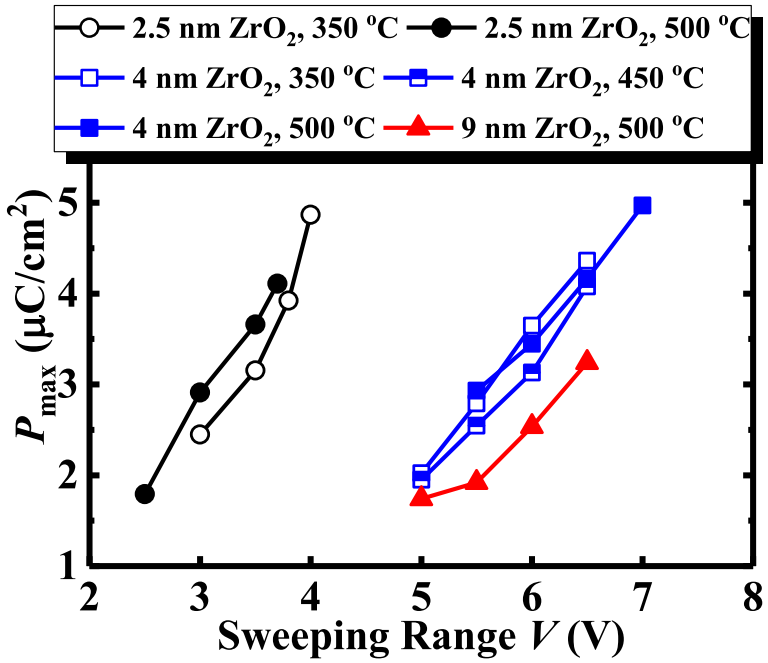

Fig. 3 Comparison of P_{max} as a function of V_{range} for the TaN/ZrO_2/Ge capacitors with different ZrO_2 thicknesses and various annealing temperatures

P/E pulses. To achieve a similar MW, a higher erase voltage is needed for the 9 nm ZrO_2 FeFET compared to the other two transistors. It is seen that a larger magnitude erase V_{GS} is required to obtain the roughly equal shift of *I-V* relative to the initial curve compared to the program V_{GS}. It is speculated that the oxygen vacancies contributing to the *P* mainly come from the reaction between TaN and ZrO_2, like the initial state of the device in Fig. 5a. As a positive V_{GS} (program) is applied, the oxygen vacancies diffuse and accumulate in the layer near the ZrO_2/Ge interface (Fig. 5b), where the distribution of the oxygen vacancy dipoles is quite different from the initial state. So it is easy to shift the *I-V* curve to a

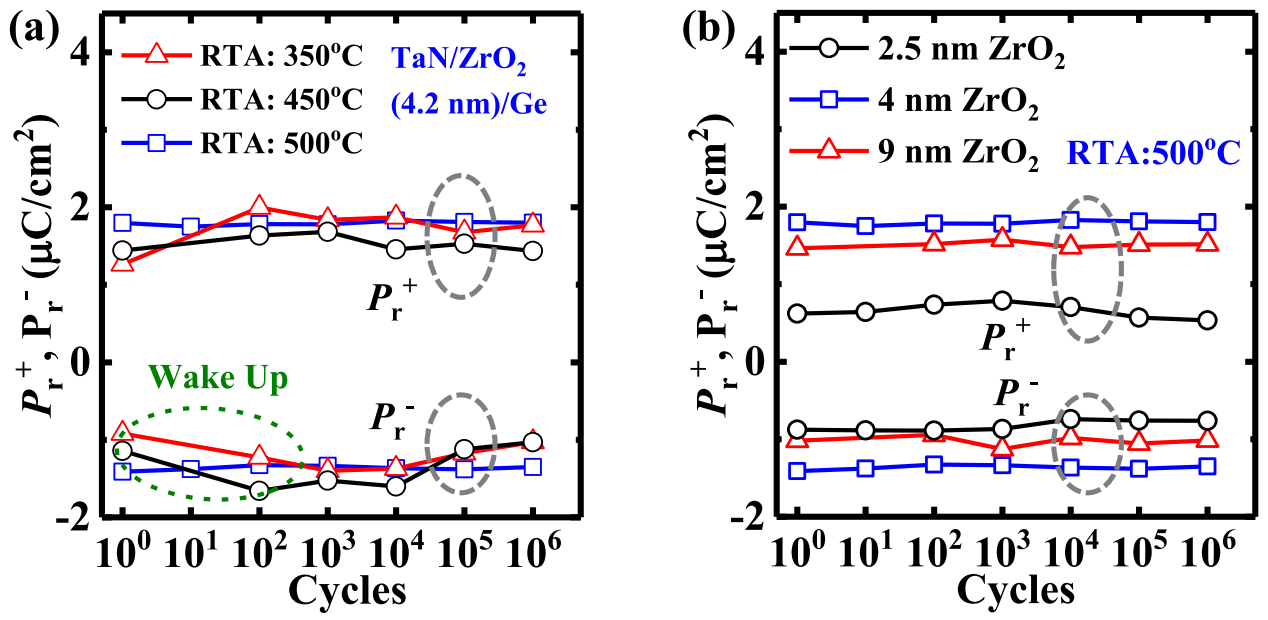

Fig. 4 **a** P_r vs. the number of ms-pulse sweeping cycles for 4 nm ZrO_2 capacitors with different RTA temperatures. **b** P_r vs. number of ms-pulse sweeping cycles for the ZrO_2 capacitors after annealing at 500 °C

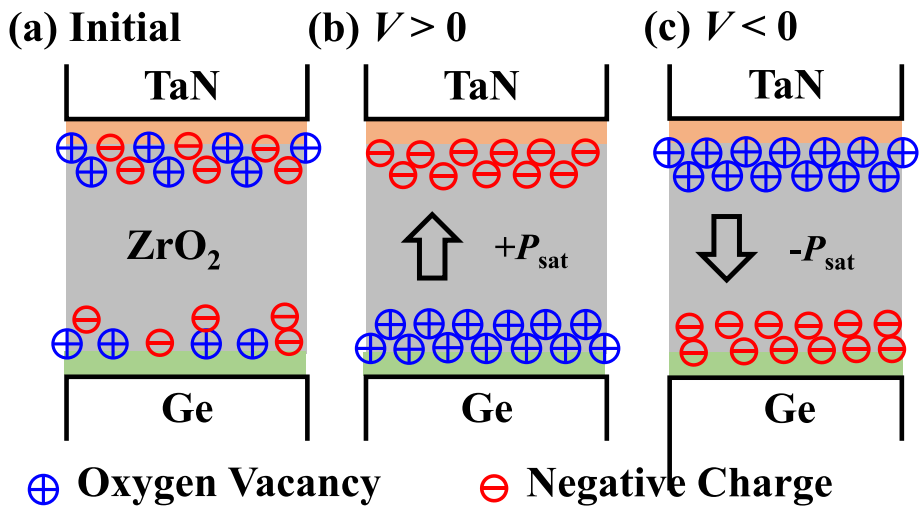

Fig. 5 Schematics of the mechanism for switchable *P* in ZrO_2 capacitors, which is attributed to the migration of voltage-driven oxygen vacancies and negative charges to form dipoles

higher $|V_{TH}|$ with a positive V_{GS}. However, as a negative V_{GS} (erase) is applied, the back diffusion of oxygen vacancies brings the gate stack back to its original state (Fig. 5c). So the magnitude of the negative erase V_{GS} has to be increased to achieve the equivalent shift of *I-V* to the positive program V_{GS}.

As the P/E pulse width is reduced to 100 ns, the ZrO_2 FeFETs still demonstrate the decent MW, as shown in Fig. 7a. Especially, the transistor with 2.5 nm ZrO_2 annealed at 350 °C achieves an MW of 0.28 V. Figure 7b plots MW vs. cycle number for the FeFETs with various ZrO_2 thicknesses with 100 ns P/E pulse condition. The 4 nm ZrO_2 device achieves a significantly improved endurance performance compared to the 2.5 nm and 9 nm ZrO_2 FeFETs, which exhibit the obvious wake-up effect and fatigue within 10^3 cycles.

Finally, the retention testing of the ZrO_2 FeFETs is characterized and shown in Figs. 8 and 9. Figure 8 a shows the evolution of I_{DS}-V_{GS} curves for the two polarization states of the 4 nm ZrO_2 FeFETs underwent RTA at 350, 450, and 500 °C. The charge trapping leads to the reduction of the devices with the time. As shown in Fig. 8b, the retention

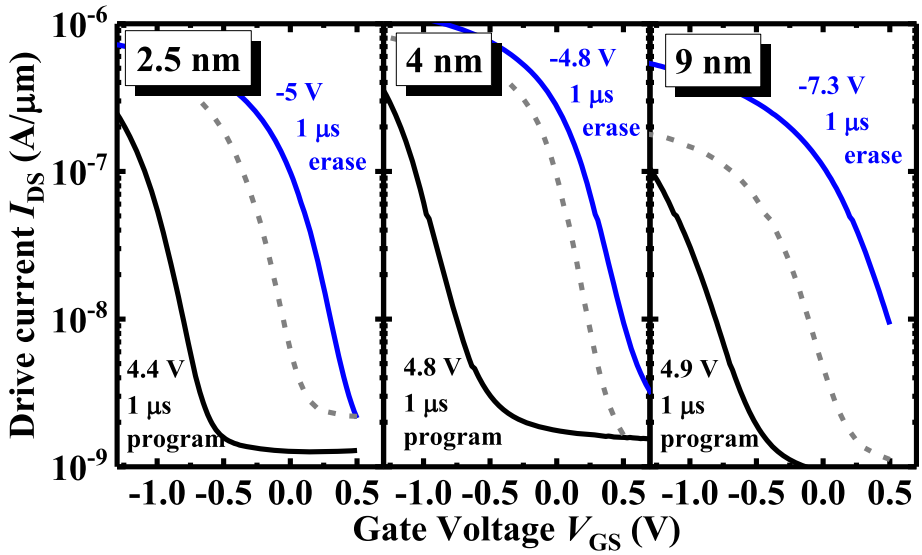

Fig. 6 Measured I_{DS}-V_{GS} curves of the 2.5, 4, and 9 nm-thick ZrO_2 FeFETs for the initial and two polarization states with 1 μs P/E pulses

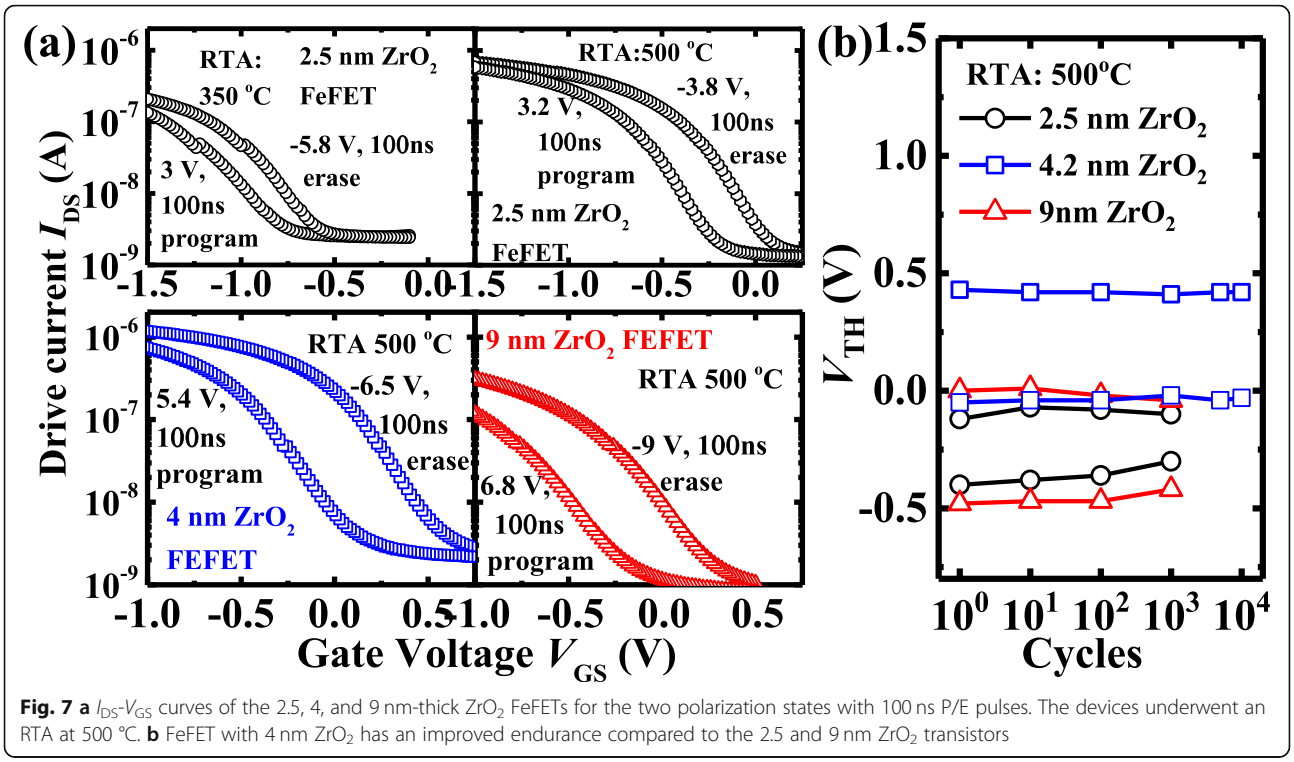

Fig. 7 **a** I_{DS}-V_{GS} curves of the 2.5, 4, and 9 nm-thick ZrO_2 FeFETs for the two polarization states with 100 ns P/E pulses. The devices underwent an RTA at 500 °C. **b** FeFET with 4 nm ZrO_2 has an improved endurance compared to the 2.5 and 9 nm ZrO_2 transistors

performance of the devices can be improved with the increase of the RTA temperature. An MW of ~ 0.46 V is extrapolated to be maintained over 10 years. Figure 9 compares the retention characteristics of the FeFETs with different ZrO_2 thicknesses. The 4 nm ZrO_2 device has an improved retention performance compared to the transistors with 2.5 and 9 nm-thick ZrO_2.

Conclusions

In summary, amorphous ZrO_2 ferroelectric capacitors are experimentally demonstrated, and the ferroelectricity is speculated to be due to the migration of the voltage-driven dipoles formed by the oxygen vacancies and negative charges. FeFETs with 2.5 nm, 4 nm, and 9 nm ZrO_2 have the MW above 1 V with 1 μs P/E pulses. The

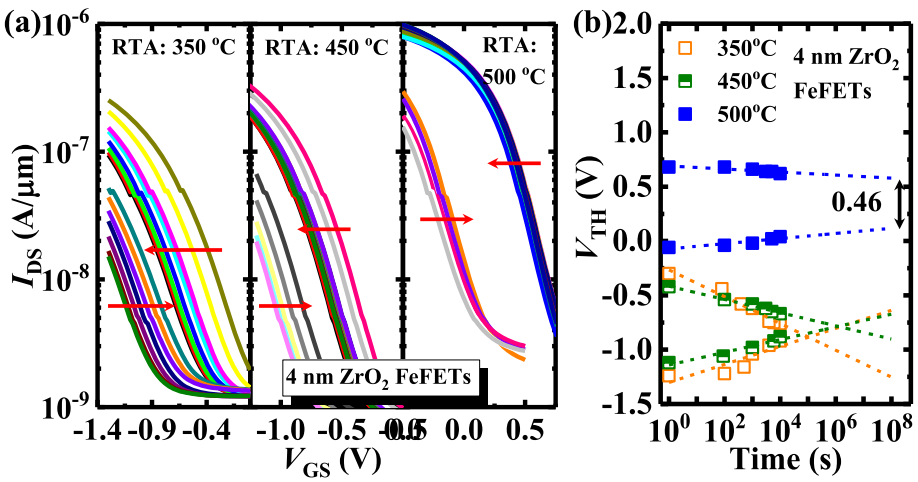

Fig. 8 **a** The evolution of I_{DS}-V_{GS} curves for the two polarization states of the 4 nm ZrO_2 FeFETs with different RTA temperatures. **b** The 4 nm ZrO_2 device annealed at 500 °C has a much better retention performance compared to the transistors with RTA at the lower temperatures

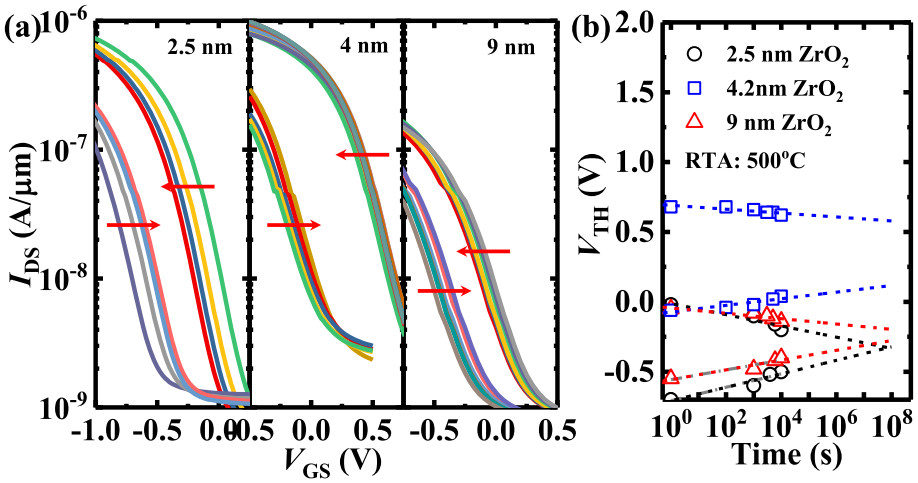

Fig. 9 a The evolution of I_{DS}-V_{GS} curves for the two polarization states for the 2.5, 4, and 9 nm-thick ZrO_2 FeFETs underwent a RTA at 500 °C. **b** The 4 nm ZrO_2 device has an improved retention performance compared to the transistors with 2.5 and 9 nm-thick ZrO_2

improved fatigue and retention characteristics are obtained in the 4 nm-thick ZrO_2 FeFET in comparison with the devices with 2.5 nm and 9 nm ZrO_2. The retention test indicates that the 4 nm ZrO_2 transistor keeps an extrapolated 10-year MW of ~ 0.46 V.

Abbreviations

RTA: Rapid thermal anneal; IL: Interfacial layer; TaN: Tantalum nitride; FeFET: Ferroelectric field-effect transistors; TDMAZr: Tetrakis (dimethylamido) zirconium; Ge: Germanium; ZrO_2: Zirconium dioxide; ALD: Atomic layer deposition; HF: Hydrofluoric acid; BF_2^+: Boron fluoride ion; MW: Memory window; NVM: Non-volatile memory; P_r: Remnant polarization; TEM: Transmission electron microscope; Ni: Nickel; P_{max}: Maximum polarization; RTA: Repaid thermal annealing; V_{range}: Sweeping voltage range

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Not applicable.

Authors' Contributions

HL and YP carried out the experiments and drafted the manuscript. GQH and YL supported the study and helped to revise the manuscript. NZ and CGD helped to do the polarization measurement. YH provided constructive advice in the drafting. All the authors read and approved the final manuscript.

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Availability of Data and Materials

The datasets supporting the conclusions of this article are included in the article.

Competing Interests

The authors declare that they have no competing interests.

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