SCIENCE CHINA
Information Sciences

• PERSPECTIVE •

June 2021, Vol. 64 166401:1–166401:2
https://doi.org/10.1007/s11432-021-3184-5

Multi level cell (MLC) in 3D crosspoint phase change memory array

Nanbo GONG

IBM T.J. Watson Research Center, Yorktown Heights 10598*, USA*

Received 25 January 2021/Accepted 3 February 2021/Published online 1 March 2021

Citation Gong N. Multi level cell (MLC) in 3D crosspoint phase change memory array. Sci China Inf Sci, 2021, 64(6): 166401, https://doi.org/10.1007/s11432-021-3184-5

The success of memory technology is of vital importance in order to handle emerging mass amount of data in our daily lives. Let us take one example here: The IBM summit is the supercomputer released in 2018 and it plays an important role to help researchers run large numbers of calculations and better understand COVID-19[1)]. To enable such powerful computing capability, the IBM summit includes 250 petabytes storage capacity[2)]. To make a fair comparison, this is larger than the total number of all the ants we can find on the earth (on the order of 10^{16}–10^{17})[3)]. Unfortunately, the performance of the memory chips still has so much room for improvement because of the big performance gap between the dynamic-random-access-memory (DRAM) and the flash memory. DRAM is volatile and the stored charge in a DRAM cell will gradually leak out, requiring periodic refresh operation that causes significant power consumption. In contrast, flash memories are suffering from slow access speed and limited endurance characteristics. As such, the performance of chips would be further improved by including the storage class memory (SCM) into the state-of-the-art memory hierarchy and bridge the performance gap between DRAM and Flash memory [1]. Among different non-volatile memory candidates [2, 3], the phase change memory (PCM) technology is considered as one of the most suitable SCM options, which offers reasonable switching speed (between the ones from DRAM and Flash memory), non-volatility, robust endurance and high density [1].

MLC in 1T1R PCM array. To further enhance the density of a PCM array, the multi level cell (MLC) approach is desired. Based on resistance in the phase change material, a PCM cell can be set into a low resistance crystalline state, a high resistance amorphous state, or intermediates between them. With appropriate write-read-verification process, it has been demonstrated that PCM is capable to be programmed into 4 levels (2 bits) with the help of transistors to precisely control the programming current that is applied to the PCM device [4]. Because of the demonstrated 2 bits per cell capability, the whole PCM array is capable to double its density. Although such MLC operation is proved to be possible in a 1 transistor 1 resistor (1T1R) array, the use of transistors limit the density of the array, because transistors are difficult to scale down while providing sufficient enough programming current to write the PCM devices. Another consideration is the balance between using write-read-verification and the latency to operate the PCM arrays. As PCM is aiming for the SCM application, it would be necessary to consider the latency penalty if write-read-verification must be implemented to achieve the MLC operation. That said, the most ideal situation is to use a no-transistor PCM array and successfully obtain MLC results without the need of applying write-read-verification procedures.

OTS-PCM crosspoint array. With respect to the no-transistor PCM array, a PCM cell shows high density potential and it is compatible to be integrated with the two terminal selector devices. It has been shown the memory cell with PCM/barrier/selector can be built using self-aligned process and provides the smallest memory cell footprint ($4F^2$) in a 2D-array [5]. Among several selector options, the ovonic threshold switch (OTS) not only shows sufficient switching time and on-off ratio, but also shows unique potential because of its compatibility to PCM. The back-end-of-line (BEOL) compatible process to fabricate the PCM/barrier/OTS cells makes it a promising technology that is suitable for a 3D crosspoint array, providing a higher density solution than the 2D-array [6–8]. Recently, significant progresses have been reported for the 3D crosspoint technology, showing great potential for a OTS-PCM array to meet all the SCM application requirements at the same time [9, 10].

Challenges for MLC in a crosspoint array. In a PCM crosspoint array, because the no-transistor two terminal structure of the OTS-PCM cell could not unselect cells with the help of transistors, it would be necessary to control the programming conditions in the wordline (WL) and bitline (BL) in order to make sure the unselected cells are not pro-

Email: nanbo.gong@aya.yale.edu

1) https://newsroom.ibm.com/IBM-helps-bring-supercomputers-into-the-global-fight-against-COVID-19.
2) https://www.ibm.com/thought-leadership/summit-supercomputer/.
3) https://en.wikipedia.org/wiki/Lists_of_organisms_by_population.

grammed while the selected cell encounters sufficient programming current and is successfully set or reset accordingly. To write and read the selected cells without turning on unselected cells, the so-called half-selected operating schemes are the most commonly used. Under this scheme, the selected cell could be successfully set and reset by the program voltage, in the meanwhile, the unselected cells stay in "off" state because they face maximum half of the program voltage that is below the threshold switching condition of the OTS-PCM cell [11]. The half-selected scheme requires strict program voltage operating ranges in order to make sure both selected and unselected cells would work as expected, and the limited window of such operating voltage range provides difficulties to obtain sizeable memory window to distinguish different levels of the PCM resistance in a crosspoint array.

In addition, PCM is known to suffer from resistance and threshold voltage (Vt) drift [8]. After resetting the PCM cell, resistance of the PCM gradually moves towards to a higher resistance level, so it is with the threshold voltage. This may not be an obvious issue for a binary bit device application, but it is detrimental for the MLC application because the whole MLC operation is no longer valid anymore if any level fails to be distinguished from the others. In the meanwhile, the OTS selector also shows threshold switching, and the root cause of the selector Vt drift still requires more understanding. As a result, it would be important to understand what is the characteristics of Vt drift in an OTS-PCM cell, and the Vt drift in the cell is a critical issue to overcome in order to make sure an MLC operation would be functional in the OTS-PCM crosspoint array.

A no-verification MLC operation in the OTS-PCM crosspoint array. Recent studies have reported the significant progress on the MLC operations for an OTS-PCM crosspoint array, and an open-loop programming MLC operation in an OTS-PCM crosspoint array has been demonstrated thanks to improved characteristics of the OTS-PCM cells within a 1Mbit array, such as tight Vt distributions and sizeable memory windows [12]. The so called open loop programming avoids the iterative read-verify-rewrite procedure and only applies one write pulse that is desired to program the cell to the target value whenever the cell is written (i.e., without the read and rewrite procedure). The success of this no-verification operation offers a great opportunity to fully utilize the fast write speed characteristics of the PCM devices, making it suitable for the SCM applications. In addition, the critical Vt drift is also comprehensively studied, and it shows that Vt drift is not sensitive to resistance level of the PCM but sensitive to the programming methods that are used to write the PCM into multi-level cell states. It suggests the open-loop programming MLC operation is possible to achieve by adopting suitable programming methods, and Vt drift is able to be modulated accordingly. To further reduce the impact from Vt drift and improve the MLC performance in the OTS-PCM array, material innovation would serve as a silver bullet. It has been shown that with Si incorporated into AsSeGe system, the OTS selector Vt drift is capable to be mitigated significantly [13].

Conclusion. Improving performance of future computing systems requires developing PCM technology to serve as an SCM candidate and bridge the performance gap between DRAM and Flash memory. PCM is capable to be programmed into multi-level and also can be integrated with an OTS selector into a high density crosspoint array without transistors. It is ideal to obtain no-verification-rewirte open-loop programming MLC operation in a no-transistor OTS-PCM crosspoint array, and the challenges to overcome includes sizeable memory window and Vt drift. Recent studies have demonstrated the possibility to obtain such ideal operation in OTS-PCM crosspoint array, with the help of tight distribution of memory window and adopting optimized programming methods that would mitigate Vt drift. It is promising to observe MLC is a feasible approach to further improve future computing system performance, and material innovation would be an important approach to further enhance the MLC performance in the OTS-PCM crosspoint array down the road.

Acknowledgements The author would like to thank Dr. W-C Chien and other colleagues from IBM T.J. Waston Research Center and Macronix International, Emerging Central Lab, for their feedback to this work, and also thank Dr. M. BrightSky, Dr. H -L Lung for management support from IBM-Macronix phase change memory joint project. The author would especially thank Dr. V. Narayanan for management support.

References

1 Breitwisch M, Nirschl T, Chen C F, et al. Novel lithography-independent pore phase change memory. In: Proceedings of IEEE Symposium on VLSI Technology, Kyoto, 2007. 100–101
2 Ma T P, Gong N. Retention and endurance of FeFET memory cells. In: Proceedings of the 11th International Memory Workshop (IMW), Monterey, 2019. 1–4
3 Gong N, Idé T, Kim S, et al. Signal and noise extraction from analog memory elements for neuromorphic computing. Nat Commun, 2018, 9: 2102
4 Chien W C, Ho Y H, Cheng H Y, et al. A novel self-converging write scheme for 2-bits/cell phase change memory for storage class memory (SCM) application. In: Proceedings of Symposium on VLSI Technology (VLSI Technology), Kyoto, 2015. 100–101
5 Lung H L. Self-Aligned, Programmable Phase Change Memory. US Patent, 6 579 760, 2003-06-17
6 Cheng H Y, Chien W C, Kuo I T, et al. Ultra-high endurance and low IOFF selector based on AsSeGe chalcogenides for wide memory window 3D stackable crosspoint memory. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), San Francisco, 2018
7 Yeh C W, Chien W C, Bruce R L, et al. High endurance self-heating OTS-PCM pillar cell for 3D stackable memory. In: Proceedings of IEEE Symposium on VLSI Technology, Honolulu, 2018. 205–206
8 Cheng H Y, Carta F, Chien W C, et al. 3D cross-point phase-change memory for storage-class memory. J Phys D-Appl Phys, 2019, 52: 473002
9 Kau D, Tang S, Karpov I V, et al. A stackable cross point phase change memory. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), Baltimore, 2009
10 Kim T, Choi H, Kim M, et al. High-performance, cost-effective 2z nm two-deck cross-point memory integrated by self-align scheme for 128 Gb SCM. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), San Francisco, 2018
11 Chien W C, Ho H Y, Yeh C W, et al. Comprehensive scaling study on 3D cross-point PCM toward 1Z nm Node for SCM Applications. In: Proceedings of Symposium on VLSI Technology, Kyoto, 2019. 60–61
12 Gong N, Chien W C, Chou Y C, et al. A no-verification multi-level-cell (MLC) operation in cross-point OTS-PCM: IBM/macronix phase change memory joint project. In: Proceedings of IEEE Symposium on VLSI Technology, Honolulu, 2020
13 Cheng H Y, Kuo I T, Chien W C, et al. Si incorporation into AsSeGe chalcogenides for high thermal stability, high endurance and extremely low vth drift 3D stackable cross-point memory: IBM/macronix PCRAM joint project. In: Proceedings of IEEE Symposium on VLSI Technology, Honolulu, 2020