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The Design of a CMOS Nanoelectrode Array with 4096 Current-Clamp/Voltage-Clamp Amplifiers for Intracellular Recording/ Stimulation of Mammalian Neurons

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Abstract

CMOS microelectrode arrays (MEAs) can record electrophysiological activities of a large number of neurons in parallel but only extracellularly with low signal-to-noise ratio. Patch clamp

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electrodes can perform intracellular recording with high signal-to-noise ratio but only from a few neurons in parallel. Recently we have developed and reported a neuroelectronic interface that combines the parallelism of the CMOS MEA and the intracellular sensitivity of the patch clamp. Here, we report the design and characterization of the CMOS integrated circuit (IC), a critical component of the neuroelectronic interface. Fabricated in 0.18-μm technology, the IC features an array of 4,096 platinum black (PtB) nanoelectrodes spaced at a 20 μm pitch on its surface and contains 4,096 active pixel circuits. Each active pixel circuit, consisting of a new switched-capacitor current injector—-capable of injecting from ±15 pA to ±0.7 μA with a 5 pA resolution —-and an operational amplifier, is highly configurable. When configured into current-clamp mode, the pixel intracellularly records membrane potentials including subthreshold activities with ~23 μV_{rms} input referred noise while injecting a current for simultaneous stimulation. When configured into voltage-clamp mode, the pixel becomes a switched-capacitor transimpedance amplifier with ~1 pA_{rms} input referred noise, and intracellularly records ion channel currents while applying a voltage for simultaneous stimulation. Such voltage/current-clamp intracellular recording/stimulation is a feat only previously possible with the patch clamp method. At the same time, as an array, the IC overcomes the lack of parallelism of the patch clamp method, measuring thousands of mammalian neurons in parallel, with full-frame intracellular recording/stimulation at 9.4 kHz.

Keywords

current clamp; extracellular recording; integrated circuits; intracellular recording; microelectrode array; nano-bio interface; nanoelectrode array; neurobiology; neurons; switched capacitor; voltage clamp

I. Introduction

CMOS microelectrode arrays (MEAs) have served as an important tool in neurobiology with their ability to record membrane potentials from a large number of neurons, with the state of the art featuring as many as 10,000's recording channels [1]–[14]. But this neuronal recording by the CMOS MEA is an extracellular technique. The voltage it records outside the neuron is a highly attenuated and filtered version of the actual membrane potential inside the neuron: *e.g.*, action potentials (APs) with intracellular amplitudes of ~100 mV are attenuated to below ~100 μV at the extracellular electrode and their intracellular duration of ~ 10 ms is reduced to as short as 100 μs at the extracellular electrode [12]. Given such a large attenuation through the extracellular neuron-microelectrode interface, the CMOS MEA cannot record small but critical synaptic events, such as post synaptic potentials (PSPs), whose intracellular amplitudes are less than ~5 mV. Another related drawback of the CMOS MEA is the inability for concurrent stimulation and recording of a neuron through the same electrode, as an extracellular stimulation signal needed is over $10^3\times$ larger than the extracellularly recorded signal [15].

In contrast, the patch clamp technique, the gold standard of high-fidelity electrophysiological recording, directly accesses the intracellular solution of a neuron with no attenuation by mechanically puncturing its membrane followed by a tight sealing [16].

The resulting intracellular recording has a far higher sensitivity than the CMOS MEA and can routinely measure synaptic activities. This intracellular recording can be also simultaneously performed with stimulation in the form of current clamp (membrane potential recording with current injected) or voltage clamp (membrane current recording with voltage applied). The current and voltage clamp modes are used for a variety of electrophysiological interrogation of neurons. For example, the current clamp recording of PSPs can find synapses and the voltage clamp, which was used for the first measurement of currents of single ion-channel molecules [17], can characterize the effect of drugs on ion channels. This highly sensitive patch clamp electrode, however, cannot be scaled into a dense array like the CMOS MEA, and only ~10 parallel patch neuron recordings have been possible so far [18].

Recently nano and micro electrodes of three dimensional structure were studied for the possibility of intracellular access [19]–[30]. Some of them are also scalable, defined by top-down fabrication, and so have been hoped for combining the intracellular sensitivity of the patch clamp and the parallelism of the CMOS MEA. But only a few of them [22], [23], [26], [27] could couple intracellularly with mammalian neurons and even then, only on a single or few neuron basis, and without the current/voltage-clamp configurations, thus lacking the capability for simultaneous recording and stimulation through the same electrode.

We have very recently developed a scalable, $64 \times 64 = 4{,}096$ platinum black (PtB) nanoelectrode array on a CMOS integrated circuit (IC), which bridges the previous gap between the intracellular sensitivity of the patch clamp and the parallelism of the CMOS MEA and performs massively parallel intracellular recording from thousands of connected mammalian neurons [31]. The CMOS IC realizes current/voltage-clamp electronics for each of the 4,096 sites, or pixels. At an individual pixel, both the surface PtB nanoelectrode interfacing with a neuron and the underlying CMOS voltage/current clamp electronics operating the PtB nanoelectrode are critical for the stable intracellular recording/stimulation of the neuron. At the same time, its arrayed operation gives rise to the parallelism.

In [31], we reported network-wide intracellular recording with this chip and its application in synaptic connectivity mapping and high-throughput drug screening. The present paper complements [31], reporting the design of the CMOS IC, describing in detail how it enables the intracellular neuronal recording with simultaneous stimulation using current/voltage clamp, a feat only previously possible with the patch clamp technique, and how it parallelizes such high-fidelity recording across the array, overcoming the limitation of the patch clamp.

Section II overviews the CMOS IC. Section III presents the pixel circuit and its current- and voltage-clamp configurations. Section IV presents the new, switched-capacitor based current injector, a crucial pixel circuit component. Sections V and VI present electrical and electrophysiological characterizations.

II. Overview of the CMOS IC

Since we seek to intracellularly record and stimulate a large number of neurons, we build a dense array of electrodes capable of intracellular access with the electrode pitch comparable to mammalian neuron dimensions (20–40 μm diameter somas) on top of a CMOS IC that integrates electronics for current- and voltage-clamp measurements at each pixel electrode. Specifically, the IC, fabricated in a dedicated 0.18-μm, 1-poly, and 6-metal wafer run, contains an array of 4,096 surface Al pads at the chip center (pad-to-pad pitch: 20 μm), connected to 4,096 active pixel circuits distributed in the 4 peripheral quadrants (1,024 circuits per quadrant) (Fig. 1a). PtB electrodes are post-fabricated on each Al pad for intracellular access [31]. The spaces between the quadrants are used for the wiring from electrodes to pixel circuits. Each pixel circuit contains a switched capacitor based current injector and an op-amp (Fig. 1b) to create a current or voltage clamp configuration (Sec. III). The IC area is 10×20 mm^2. We place only one IC in each reticle occupying 20×20 mm^2 to allow a 5 mm handling area on each side of the IC for the post fabrication of PtB electrodes. These handling areas are diced away before wire bonding and packaging [25], [31].

By separating the electrode array region in the center from the active pixel circuit region in the 4 peripheral quadrants, we achieve both the dense 20 μm pitch for the electrode array for high spatial resolution and the large 100×250 μm^2 area for each active pixel circuit for high configurability and low noise. This layout strategy combines the concepts of high-fidelity peripheral electronics from the switched matrix CMOS MEAs [3], [8], [11], [13] and the full-frame readout of the active-pixel sensor (APS) CMOS MEAs [1], [2], [7], [14].

The metallic routing from a pixel circuit to its electrode has a length of 1 ~ 10 mm, depending on the location of the pixel circuit and its electrode. To mitigate the capacitive coupling between adjacent routings, we surround each routing with ground shields (Fig. 2, left). This reduces the cross-coupling capacitance to < 1 fF per routing, virtually ensuring no cross-contamination between different electrode signals (Section V.D). We minimize the parasitic capacitance $C_{p,r}$ between an individual routing and its shield by gradually increasing the spacing between them, as the density of the routings decreases further away from the electrode array. $C_{p,r}$ is ~1–2 pF in electric field simulations (Fig. 2, right for the densest routings). The routings and shields use 4 of the available 6 metal layers and occupy $\sim 1.5 \times 20$ mm^2 in total.

To enable accurate temperature regulation, the IC contains two temperature sensors (based on the voltage differential between two diode branches of different sizes, 1:146 ratio, biased at the same current) and a heater (a 10-Ω poly silicon resistor capable of dissipating 1.3 W) adjacent to the electrode array (Fig. 1a). They regulate the temperature of the IC to 34–37°C for cell health (Section V.A).

The design of this IC with the particular choice of the architecture, building blocks, and target performance is guided by our goal to demonstrate the unprecedented massive parallelism in intracellular recording of neurons. For example, we focus our design efforts significantly on realizing the front-end current/voltage clamp capability in each active pixel circuit, as it is essential for robust intracellular access into neurons; on the other hand, for the

back-end digitization that is not fundamental to the key demonstration goal, we choose to use commercially-available high-precision analog-to-digital converters (ADCs) in order to accelerate the chip development. To drive such off-chip electronics, we implement high-speed analog multiplexers on chip. They require large bias currents to operate at frequencies in excess of 1 MHz, but in our *in vitro* setting the associated heat readily sinks through the open well of solution on the chip. In fact, we actually need an explicit heating of the solution to keep the cells at the temperature around 35 °C. This is in contrast to implantable applications [32], where an IC insulated by biological tissue should maintain low power density to prevent tissue damage.

III. The Active Pixel Circuit

Figure 3a shows the schematic of the active pixel circuit. Its main components are a switched capacitor current injector (Sec. IV) and an op-amp with configurable negative feedback networks, both of which are connected to the same PtB electrode of the pixel. It also contains a transparent latch digital memory and an output multiplexer (shared by 128 pixels per multiplexed analog output). The pixel circuit contains many transmission gate switches, controlled by the digital memory programmable in real time at up to ~10 MHz. Many of these switches are in the op-amp negative feedback networks, making the closed-loop amplifier highly configurable. Four voltage nodes, $V_{s,1}$ through $V_{s,4}$, can be connected to various voltage signals or bias references from off-chip electronics, supporting the high configurability as well as various tests. Of the pixel circuit area of 0.025 mm^2 (Fig. 3b), the op-amp takes the largest part due to large transistors (Fig. 3c, left) for minimizing noise [33]. A dedicated bias network is included for each pixel, as opposed to a global bias, to help isolate the 4,096 op-amps. The current injector occupies only ~0.003 mm^2, almost an order of magnitude smaller than standard current injectors used in MEAs [6], [9], [11], [13], attesting to the advance of our novel design (Sec. IV).

For intracellular recording/stimulation, we operate the pixel circuit of Fig. 3a in pseudo current or voltage clamp mode (Fig. 4), named after the similar configurations of the patch clamp. ‘Pseudo’ emphasizes that our intracellular interface has a finite attenuation, unlike the patch clamp, as seen below.

A. Pseudo Current-Clamp (pCC) Configuration

The pseudo current-clamp (pCC) mode (Fig. 4a) is obtained from Fig. 3a by operating the high output impedance current injector in parallel with the op-amp with the negative feedback configured as a high input impedance voltage amplifier. The current injector runs a current I_e through the electrode. This continuously injected I_e (typically on the order of −1 nA) causes and sustains the membrane permeabilization in a neuron to initiate and maintain intracellular coupling [31]. Another crucial role of this current injection is to compensate the leakage current from within the neuron that inevitably arises due to the membrane permeabilization. At the same time, the voltage amplifier concurrently measures the electrode voltage, V_e, which is an attenuated version of the membrane potential, V_m. In this way we intracellularly record membrane potentials (APs and PSPs) of the neuron. This operation is akin to the patch clamp’s current clamp recording.

The voltage amplifier is a bandpass configuration, traditionally used for low-noise neural recordings [33] (Fig. 4a). Its passband gain from V_e to the amplifier output V_{amp} is the ratio of the feedback capacitors $-C_1/C_2$. This is tunable: C_1 is 3.5 pF but C_2 can be any addition of ~5, ~20, and ~100 fF (Fig. 3a). The amplifier bandwidth covers the electrophysiological spectral range: ~1 Hz to 5 kHz [34]. The low frequency pole, f_1 ~ 1 Hz, is set by C_2 in parallel with the large resistance of feedback antiparallel diode pairs (dps) (options for 1–7 dps; Fig. 3a) biased near zero current. The more the dps, the less the voltage drop on each dp, reducing the nonlinearity and increasing the resistance. These dps are realized using *p*-contacts within an *n*-well and contain parasitic reversed biased *pn* diodes to the substrate and corresponding leakage currents. An additional dp tapped to $V_{s,4}$ sets a small current to tune the DC level of V_{amp} to overcome these leakage currents and to fine tune the feedback resistance, which we discuss experimentally in Sec. V.C. The high frequency pole, f_2, is set by the gain bandwidth product of the amplifier.

In the pCC recording, a change of the membrane potential, V_m, modulates the electrode voltage, V_e, according to:

$$\frac{\Delta V_e}{\Delta V_m} = \frac{R_s}{R_s + R_{jm}} \frac{Z_{p,r} || Z_1}{(Z_{p,r} || Z_1) + Z_e} \approx \frac{R_s}{R_s + R_{jm}} \tag{1}$$

R_s is the seal resistance, R_{jm} is the junctional membrane resistance, and Z_1, $Z_{p,r}$ and Z_e are the impedances of C_1, $C_{p,r}$, and the PtB electrode. The approximation in the last step of Eq. (1) is due to $|Z_e| \ll |(Z_{p,r} || Z_1)|$, which holds as the surface roughness thus large surface area of the PtB electrode greatly reduces Z_e [Sec. V-D]. The front-end attenuation of Eq. (1) precedes the amplifier gain, contrasting the patch clamp's current clamp that has no such front-end attenuation (hence the prefix, 'pseudo' in our current clamp). But as seen shortly, this attenuation is far less than that of the extracellular recording.

For stimulation, we change I_e to modulate V_m according to:

$$\frac{\Delta V_m}{\Delta I_e} \approx R_s \frac{R_m}{R_{jm} + R_m} \tag{2}$$

where R_m is the membrane resistance. Here we have assumed $R_s \ll R_{jm} + R_m$, which holds for most nanoelectrodes (typical values: R_s < 100 MΩ, $R_{jm} \gg$ 100M Ω, R_m ~ 100 MΩ).

Equations (1) and (2) show that a reduction of R_{jm} or an increase in R_s improves the recording amplitude and the ability to manipulate V_m for stimulation. Case in point, the membrane permeabilization (intracellular access) induced by the aforementioned injection of I_e reduces R_{jm} to decrease the attenuation of Eq. (1) by 1~2 orders: APs are measured from rat neurons with ΔV_e of 1 ~ 30 mV [31], contrasting MEA extracellular recording of APs in the range of 10 ~ 100 μV. Overall, the pCC allows intracellular recording of membrane potentials of a neuron with a current injection, where the current injection can be also used for concurrent stimulation. Finally, note only a small fraction (~1–10%) of I_e ~ −1 nA enters the permeabilized neuron, as $R_s \ll R_{jm} + R_m$.

Recently a CMOS MEA [6] as well as our previous version of the CMOS nanoelectrode array [25] intracellularly recorded the membrane potential of cardiomyocytes without using the pCC but by applying a voltage to an electrode followed by a voltage recording. This voltage application also produces an electrode current to permeabilize the cell membrane for intracellular access. But since the voltage application and voltage recording cannot be simultaneous, the electrode current is absent during the recording, and hence, the permeabilization-induced leakage from the cell cannot be compensated during the recording. This still did not prevent the intracellular recording of the membrane potentials of cardiomyocytes, as the tissue of the cardiac cells is electrically more robust due to their gap junction connections. But this voltage-application voltage-recording approach deficient in leakage compensation cannot achieve stable intracellular recording of neuronal membrane potentials, as neurons are electrically isolated via chemical synapses and are therefore far more adversely affected by the leakage and the resulting depolarization.

B. Pseudo Voltage-Clamp Configuration

The pseudo voltage-clamp (pVC) mode (Fig. 4b) is obtained by disconnecting the current injector and configuring the feedback loop of the op-amp to form a transimpedance amplifier. The feedback resistance of the transimpedance amplifier is a switched capacitor, which utilizes the switches in parallel to the feedback dps and the parasitic capacitance C_{par} ~35 fF of the intermediate node between the sets of 2 dps and 4 dps (Fig. 3a). These switches are controlled in real time using the memory with non-overlapping clock phases Φ_1 and Φ_2. We set the effective resistance $R_{TIA} = 1/ f_{TIA} C_{par}$ of the switched capacitor typically around ~700 MΩ using a switching frequency f_{TIA} of ~ 40 kHz. The high-frequency pole of the transimpedance amplifier is set by the feedback capacitance C_2 in parallel with R_{TIA}.

In contrast to the commonly used integrate and reset scheme, which offers the lowest noise option for current measurement [35], the feedback switched capacitor allows for sampling of all pixels via the multiplexer regardless of their sampling position as the output voltage is never completely reset. Rather, a packet of feedback charge, $\Delta Q_{fb} = V_{amp} C_{par}$, is switched from the output to the negative terminal of the amplifier to 'soft-reset' the voltage across C_2, which reaches a steady state across a switching period, $1/ f_{TIA}$, when it is equal to the transimpedance amplifier input current, $I_{in} = \Delta Q_{fb}/ f_{TIA}$. The noise of this configuration is comparable to the integrate and reset scheme, as the input current is integrated across C_2 [35], except we observe significantly more noise from pixels sampled during Φ_1 due to additional leakage current from the 3 dps in parallel to the used switch (Fig. 3a) (Section V.C).

The pVC mode utilizes the transimpedance amplifier in applying a voltage $V_{s,1} = V_e$ to the electrode and simultaneously measuring the electrode current I_e. The bias point of V_e is adjusted to set the bias value of I_e at −1 nA, which induces membrane permeabilization for intracellular access. Then the modulation of V_e is used as a voltage stimulation to induce a change of the membrane potential V_m:

$$\frac{\Delta V_m}{\Delta V_e} = \frac{R_m}{R_{jm} + R_m} \tag{3}$$

where we have used $|Z_e| \ll R_s$, R_{jm}, and R_m, and $R_s \ll R_{jm} + R_m$. The resulting membrane current (ion channel current such as Na^+ spikes) ΔI_m modulates the electrode current in the range of ~100 pA to 1 nA [31] according to

$$\frac{\Delta I_e}{\Delta I_m} = \frac{R_m R_s}{R_s Z_e + R_{jm}(R_s + Z_e) + R_m(R_s + Z_e)} \approx \frac{R_m}{R_{jm} + R_m}. \quad (4)$$

This ΔI_e is measured by the transimpedance amplifier. ΔI_e is an attenuated version of ΔI_m and contrasts the patch clamp's voltage clamp that has no such front-end attenuation (and hence the prefix, 'pseudo' for our voltage clamp). But the attenuation factor is greatly reduced due to the reduction of R_{jm} with the intracellular access (membrane permeabilization with the injection of the bias value of I_e), just like in the pCC case. On the other hand, unlike the pCC, increasing R_s does not improve either the ability to record or stimulate to the first order: as $|Z_e| \ll R_s$, R_{jm}, and R_m, V_j is effectively connected to the pseudo-ground of the amplifier's negative terminal which eliminates shunted membrane current through R_s. Nonetheless, a small R_s will increase the bias value of I_e for a given V_e and also decrease recording/stimulation signal transfer if $R_s \sim Z_e$.

IV. A Switched-Capacitor Based Current Injector

A key building block in the pixel circuit that enables the pCC intracellular recording is the current injector. Our novel design meets the demands of pA-range current precision needed for the membrane permeabilization, high output impedance to hold an injected current at a nearly constant and not to interfere with voltage signal amplification, and a small area such that it can be integrated in each of the 4,096 pixels.

A. Basic Topology and Operating Principle

In Fig. 5a, a capacitor C_{SC}switched between voltages V_1 and V_{OUT} ($V_1 > V_{OUT}$) with non-overlapping clock phases $\square_1$ and $\square_2$ of frequency f_{SC} acts as a resistor $R_{eff} = 1/f_{SC}C_{SC}$. The output current into V_{OUT}, averaged over a clock period, is given by $\overline{I_{OUT}} = f_{SC}C_{SC}(V_1 - V_{OUT})$. As f_{SC} can be varied over many orders of magnitude, $\overline{I_{OUT}}$ can assume a wide range of values, with its minimum value comfortably falling into the pA region. For example, with C_{SC} = 30 fF, $V_1 - V_{OUT}$ = 0.6 V, and f_{SC} increasing from 1 kHz over many orders of magnitude, $\overline{I_{OUT}}$ can be tuned up from 18 pA over the same orders of magnitude. If this switched capacitor drives an electrode immersed in an electrolyte modeled as a Faradaic resistor R_L in shunt with a double layer capacitor C_L (Fig. 5a), the injected $\overline{I_{OUT}} \approx f_{SC}C_{SC}(V_1 - V_{OUT})$ cannot be fixed at a constant as V_{OUT} varies with time. The corresponding small-signal output impedance, $Z_{OUT} = \left|\partial V_{OUT}/\partial \overline{I_{OUT}}\right|$, is $R_{eff} = 1/f_{SC}C_{SC}$.

To increase Z_{OUT} substantially, we can build a source follower circuit around the switched capacitor like in Fig. 5b to set V_1 - V_{OUT} at a fixed value: the V_1 and V_{OUT} nodes of the switched capacitor are connected to the source and gate of the PMOS transistor. V_1 then

follows V_{OUT} to maintain V_1 - V_{OUT} at V_{SG}, the source-gate voltage of the transistor. In the absence of channel length modulation, V_{SG} is fixed at a constant value by the bias current I_0 and independent of V_{OUT}. In this ideal case, $\overline{I_{OUT}} \approx f_{SC}C_{SC}(V_1 - V_{OUT}) = f_{SC}C_{SC}V_{SG}$ is perfectly independent of V_{OUT} and can be set by f_{SC} and C_{SC} to a constant value. Correspondingly, $Z_{OUT} = \infty$. In the realistic case with the transistor channel length modulation, V_{SG} does vary with V_{OUT} but only weakly, so $\overline{I_{OUT}} \approx f_{SC}C_{SC}(V_1 - V_{OUT}) = f_{SC}C_{SC}V_{SG}$ exhibits only a small dependence on V_{OUT}. The corresponding Z_{OUT} calculated with the small-signal model of Fig. 5c is:

$$Z_{OUT} = \frac{r_{o,cm}(R_{eff} + r_{o,sf}) + r_{o,sf}R_{eff}(1 + g_m r_{o,cm})}{r_{o,cm} + r_{o,sf}} \approx (g_m r_o/2) \times 1/(f_{SC}C_{SC}) + r_0/2 \quad (5)$$

where $r_{o,sf}$ and $r_{o,cm}$ are the output resistances of the PMOS transistor and the current (I_0) bias circuit, respectively, and g_m is the transconductance of the PMOS transistor. The second line is approximated by setting $r_{o,sf} \approx r_{o,cm} \equiv r_o$ without losing essence and by using $g_m r_o \gg 1$. As seen, Z_{OUT} is greatly boosted from $R_{eff} = 1/f_{SC}C_{SC}$ by a factor of $g_m r_o/2$.

B. Transient Dynamics

We now discuss the transient behaviour of the switched capacitor current injector of Fig. 5b. During a clock phase Φ_1, C_{SC} is disconnected from V_{OUT} and connected to V_1 via the switch on-resistance $R_{SW}(R_{SW} \ll R_L)$. Throughout this Φ_1 phase, V_{OUT} decays with a slow time constant of the load, $\tau_L = R_L C_L$, and V_1 follows this decay to maintain $V_1 = V_{OUT} + V_{SG}$ (Fig. 6a). In contrast, at the onset of the phase Φ_1, the switched capacitor voltage, V_{SC}, makes a rapid upward transition from V_{OUT} to $V_1 = V_{OUT} + V_{SG}$ (Fig. 6a), rapidly charging C_{SC} (time constant: $\tau_1 = R_{SW}C_{SC} < 1\text{ ns} \ll \tau_L$) with $\Delta Q_{SC} = C_{SC}\Delta V_{SC} = C_{SC}V_{SG}$.

During the subsequent clock phase Φ_2, C_{SC} is disconnected from V_1 and connected to V_{OUT} via R_{SW}. This re-configuration rapidly redistributes the charge $\Delta Q_{SC} = C_{SC}V_{SG}$ between C_{SC} and C_L with a fast time constant $\tau_2 \approx R_{SW}C_L C_{SC}/(C_L + C_{SC}) \approx R_{SW}C_{SC} < 1\text{ ns} \ll \tau_L$, discharging C_{SC} (lowering V_{SC}) and charging C_L (raising V_{OUT}) until $V_{SC} = V_{OUT}$ (Fig. 6a). The resulting change of the output voltage, ΔV_{OUT}, is

$$\Delta V_{OUT} = \frac{\Delta Q_{SC}}{C_{SC} + C_L} = \frac{C_{SC}V_{SG}}{C_{SC} + C_L} \approx \frac{C_{SC}V_{SG}}{C_L}. \quad (6)$$

These changes of V_{SC} and V_{OUT} (V_1 follows V_{OUT} to maintain the difference V_{SG}) occur rapidly during the very early part of the phase Φ_2 due to the short time constant τ_2 (Fig. 6a). The charge packet injected to C_L during the charge redistribution in the early part of Φ_2 is $\Delta Q_{OUT} = C_L\Delta V_{OUT}$. The output current I_{OUT} is due to this charge packet injection, and its average over a clock period is given by

$$\bar{I_{OUT}} = f_{SC}\,\Delta\,Q_{OUT} = f_{SC}C_{SC}V_{SG}\times\left[\frac{C_L}{C_{SC}+C_L}\right] \approx f_{SC}C_{SC}V_{SG} \tag{7}$$

which is consistent with the calculation of Sec. IV-A.

With repeated clock cycles V_{OUT} is then a sequence of a rapid ΔV_{OUT} up-step (time constant τ_2) followed by a slow decay (time constant τ_L) (Fig. 6a). If we break down I_{OUT} into current $I_{OUT,R}$ through R_L and current $I_{OUT,C}$ through C_L ($I_{OUT} = I_{OUT,R} + I_{OUT,C}$) in phase Φ_2, the rapid charging of C_L in the beginning of Φ_2 is described by $I_{OUT} \approx I_{OUT,C} > 0$, while the background slow discharging of C_L through R_L is described by $-I_{OUT,C} \approx I_{OUT,R}$ ($I_{OUT,C} < 0$) with $I_{OUT} \approx 0$ (Fig. 6a). In the initial clock cycles, the charging of C_L by the charge packet injection $\Delta Q_{OUT} = C_L \Delta V_{OUT}$ per clock cycle exceeds its discharging through R_L per clock cycle thus V_{OUT} overall rises, but once C_L is sufficiently charged at later clock cycles, its charging and discharging balance each other, and V_{OUT} reaches a plateau (except voltage ripples) (Fig. 6a, bottom; Fig. 6b). This evolution of V_{OUT} into the steady state, ignoring the ripples, can be quantified by evaluating V_{OUT} at $t = n/f_{SC}$ or at the end of n-th clock phase Φ_2 as follows,

$$V_{OUT}(t) = \Delta V_{OUT}\sum_{k=1}^{n}\exp\left(-\frac{k}{f_{SC}R_LC_L}\right)\times\exp\left(-\frac{1}{2f_{SC}R_LC_L}\right) \approx \overline{I_{OUT}}R_L\left[1-\exp\left(-\frac{t}{R_LC_L}\right)\right], \tag{8}$$

where we have used $f_{SC}\tau_L = f_{SC}R_LC_L \gg 1$ and Eqs. (6) and (7). This converges to $\overline{I_{OUT}}R_L$ in steady state (Fig. 6b), *i.e.*, in the steady state, $\overline{I_{OUT}}$ flows into the electrode to charge C_L and then exactly the same amount of charge leaks out through R_L as expected. This is equivalent to flowing $\overline{I_{OUT}}$ through R_L. In fact, the overall voltage response of the R_LC_L load to the switched-capacitor current injector captured by Eq. (8), ignoring the ripples (ΔV_{OUT} of Eq. (6)), is identical to the voltage response of the R_LC_L load to an ideal step current with a magnitude $\overline{I_{OUT}}$ (Fig. 6b). This justifies our current injector as a constant current injector. The foregoing discussion has assumed $\overline{I_{OUT}}R_L < V_{DD} - V_{OV} - V_{SG}$ (V_{OV}: overdrive voltage of the current mirror transistor); $\overline{I_{OUT}}R_L > V_{DD} - V_{OV} - V_{SG}$, V_{OUT} if will start to roll off and be clipped at V_{DD} (Fig. 6b).

In the pCC mode, the current injector is connected to the electrode (so $V_e = V_{OUT}$ and $I_e = I_{OUT}$) and runs in parallel with the voltage amplifier (Fig. 4a) where $\Delta V_{OUT} = 0.1 \sim 50$ mV for $C_L = 1 \sim 100$ pF. This ripple voltage could interfere with the recording of $\Delta V_e = 1 \sim 30$ mV. We minimize this interference using clock synchronization [Section IV-D].

C. Implementation

The actual switched-capacitor based current injector we implement is shown in in Fig. 7a. It can inject both positive and negative currents. The polarity is controlled by turning on either current source $I_{0,p}$ or $I_{0,n}$, to reduce the circuit to either Fig. 7b for positive injection,

$\overline{I_{OUTPMOS}} \approx f_{SC} C_{SC} V_{SG,PMOS} > 0$, or Fig. 7c for negative injection, $\overline{I_{OUTNMOS}} \approx -f_{SC} C_{SC} V_{GS,NMOS} < 0$. For pCC recording, we use the NMOS configuration of Fig. 7c to set $I_e \sim -1$ nA, for negative current enables intracellular access (Fig. 4a). Here we do not balance the negative injection with a positive injection for a given clock frequency in order to minimize the amount of circuitry and corresponding area: it is only used as a negative current injector for the intracellular experiments.

The bottom of Fig. 7d (solid red box) shows the transistor-level schematic of Fig. 7a. The core switched capacitor circuit uses two transmission gates and can add 10 or 100 fF to the parasitic capacitance $C_{SC,p} \sim 30$ fF of the V_{SC} node for C_{SC}. We remove the body effect of transistors M_n and M_p to minimize the $|V_{SG}|$ dependency on V_{OUT} by tying the source and body nodes in both the PMOS and NMOS transistors (the 0.18-□m technology we use is a triple-well process). A control signal, EN_{POS}, in the bias network enables either the $I_{0,p}$ or $I_{0,n}$ current sources of Fig. 7a for positive or negative injection. The clock can be selected from three clock inputs, CLK[1:3], and this enables flexible control of f_{SC} across the 4,096 pixels.

D. Clock-Sampling Synchronization

As the current injector in the pCC configuration utilizes switched capacitances, f_{SC} is synchronized to the pixel multiplexer to minimize aliasing of switching induced noise, ΔV_{OUT} of Eq. (6), in the recorded amplifier output signal, V_{amp}. The aliased ΔV_{OUT} amplitude dominates the noise of the pCC configuration and is larger than any parasitic charge injection or clock feedthrough as it is directly related to the discharging of the switched capacitor into the current injector's output node/input of the amplifier. To start, V_{amp} is sampled by a 128:1 output multiplexer (Fig. 3a, c) operated at a frequency of $f_s \sim 1.2$ MHz resulting in a pixel sample frequency, $f_{s,pixel} = f_s/128 \sim 9.4$ kHz. To synchronize f_{SC} to $f_{s,pixel}$ across all 128 pixels in the multiplexer, f_{SC} should be an integer multiple of $f_{s,pixel}$ ($f_{SC} = nf_{s,pixel}$, $n = 1, 2, \ldots$) while f_s should be an integer multiple of f_{SC} ($f_s = mf_{SC} = 128\, f_{s,pixel}$, $m = 1, 2, \ldots$). Taken together ($n \cdot m = 128$), f_{SC} must be a power of 2 multiple of $f_{s,pixel}$ to eliminate aliasing ($f_{sc} = 2^N f_{s,pixel}$, $N = 0, 1, 2, \ldots$).

However, this constraint limits the resolution of injected current as $\overline{I_{OUT}} \propto f_{SC}$. To elaborate, the minimum $|\overline{I_{OUT}}|$ at $f_{s,pixel} \sim 9.4$ kHz would result in available $|\overline{I_{OUT}}|$ of only 150 pA, 300 pA, 600 pA, 1.2 nA, 2.4 nA, etc. To obtain a higher resolution in the injected current, a non-symmetric clocking scheme is used for generation of f_{SC} (Fig. 8). Effective single integer multiples are established by spacing n pulses as evenly as possible with $1/f_s$ resolution throughout the total multiplexer period of $1/f_{s,pixel} = 128/f_s$ (Fig. 8a). The resultant digital bit stream is then repeated at $128/f_s$ (equivalent to $1/f_{s,pixel}$, ~100 μs) to form a continuous output. The current resolution used for experiments is then $n \cdot 150$ pA, $n = 1, 2, \ldots, 64$. The non-symmetrical switching can increase ΔV_{OUT} by up to 50% at $n = 63$ (Fig. 8b), yet the synchronization minimizes this increase from affecting signal measurement. A dedicated microprocessor is used to generate the non-symmetric clocks (CLK[1:3] in Fig. 7). During experiments (Section VI.A.) we observe low frequency ΔV_{OUT} noise most likely due to clock drift between the microprocessor and acquisition electronics.

The same synchronization scheme is used for the pVC configuration, whose transimpedance amplifier also uses a switched capacitance. In this case, we commonly set $f_{TIA} = 4\ f_{s,pixel} =$ 37.6 kHz to minimize switching noise.

V. Electrical Characterization

A. Experimental Setup

The IC is packaged and placed on a printed circuit board (PCB) (Fig. 9). The IC and PCB are programmed and read through three National Instruments PXIe-6358 data acquisition (DAQ) cards and interfaced to a computer through LabVIEW software. For digital programming, each pixel is addressed in a shift register (4,096 bits) with real time adjustment/latching of the bit lines (B[1:25] in Fig. 3). For recording, the 4,096 pixel amplifier outputs are divided into 32 subgroups. Each subgroup contains 128 outputs from 2 rows of the array, feeding its own 128:1 analog output multiplexer on chip. Each of the 32× distributed in-pixel multiplexers, shown in Fig. 3c, right, consumes 0.45 mW of total power. 32 NMOS source followers, each consuming 6.86 mW, are then used to buffer the 32× 128:1 multiplexer outputs from the IC to 32× 16 bit analog-to-digital converters of the DAQ cards. Adjacent pixel-to-pixel cross talk within the multiplexer was measured at −43 dB. The overall data rate of recording is 77 MBps.

The IC's V_{SS} is set to earth ground and $V_{DD} = 3.6$ V; this is set higher than the 3.3 V transistors we use, in order to increase both output and stimulation voltage ranges. The $V_{s,1}$ to $V_{s,4}$ nodes are connected to DAQ analog outputs, which are low pass filtered ($f_{-3dB} \sim 1$ Hz) to provide bias voltages or buffered with a bandwidth of ~100 kHz to provide voltage signals for various pixel circuit characterizations. The extracellular solution is biased using a Pt or Ag/AgCl reference electrode at V_{ref} , which is adjustable from 0 V to 3.6 V. To regulate the temperature for cell health, the two temperature sensor signals from the IC are fed to an analog PI controller on the PCB, which then sets the voltage of a regulator on the PCB to drive the integrated heater. The designed accuracy for the temperature regulation is <1°C and is calibrated using a thermocouple placed on the surface of the device in solution. In addition to the IC's total power dissipation of 1.25 W when the array is fully enabled, the heater typically dissipates 0.55 ~ 0.85 W to maintain 35 °C (Table I). This extra power dissipation is needed to overcome heat loss of the solution on top of the device to the ambient environment and contrasts with MEAs designed for interfacing to thermally insulating tissues or environments. Like the integrated pixel array, the PCB is designed to be highly configurable to ensure ample experimental flexibility and is adjusted using analog switches digitally controlled through a serial interface.

B. Measurement of Pixel Current Injector

We first characterize the pixel current injector by connecting V_{OUT} to the PCB via $V_{s,3}$, bypassing the pixel electrode and the solution. Fig. 10a shows the measured positive and negative $\overline{I_{OUT}}$ *vs.* f_{SC} (1 kHz ~ 10 MHz) for $V_{OUT} = V_{s,3} = 1.8$ V ($V_{DD} = 3.6$ V, $V_{SS} = 0$ V). They confirm the linear response of $\overline{I_{OUT}}$ to f_{SC} over the 4 decades of frequency, from which we extract $V_{SG,PMOS} = 0.63$ V, $V_{GS,NMOS} = 0.56$ V, and $C_{SC,p} = 26$ fF. The minimum $|\overline{I_{OUT}}|$ is ~15 pA at $f_{SC} = 1$ kHz and the maximum $|\overline{I_{OUT}}|$ is ~0.7 μA at $f_{SC} = 10$ MHz.

To demonstrate the weak dependence of $|\overline{I_{OUT}}|$ on V_{OUT}, $V_{OUT} = V_{s,3}$ is swept from 0 V to 3.6 V while fixing f_{SC} at 100 kHz. Both currents show flat responses (Fig. 10b), with the positive $\overline{I_{OUT}}$ rolling off around V_{DD}- $V_{SG,PMOS}$ ~ 3.0 V and the negative $\overline{I_{OUT}}$ rolling off around V_{SS} + $V_{GS,PMOS}$ ~ 0.6 V. The measured variations of $\overline{I_{OUT}}$ in the flat regions are only within ~5 % for $C_{SC} = C_{SC,p}$. Its deviation from theoretical 0.3% is due mainly to the voltage dependence of $C_{SC,p}$ (for C_{SC} = 100 fF + $C_{SC,p}$ where the $C_{SC,p}$ effect is weaker, the current variation is reduced to <2 %). In addition, this variation of $\Delta\,\overline{I_{OUT}}/\overline{I_{OUT}}$~5% for the V_{OUT} sweep remains the same regardless of $f_{SC} \propto \overline{I_{OUT}}$ because Z_{OUT} is approximately inversely proportional to $\overline{I_{OUT}}$ [Eq. (5)]. The discrete negative injection levels for the clock-sampling synchronization scheme (Sec. IV-D) were then measured using $C_{SC} = C_{SC,p}$, the configuration used for the pCC intracellular measurements. For the pixel shown in Fig. 11, left, $\overline{I_{OUT}}$ is at distinct multiples of −147 pA, corresponding to $nf_{s,pixel}$. At $n = 8$, $\overline{I_{OUT}}$ shows <5% variation around ~ −1.2 nA across the array.

To measure the output ripple voltage ΔV_{OUT} [Eq. (6)] and to highlight the ability for small amplitude current injection, the current injector was tested in solution using a small, 2 μm diameter Pt electrode (with no PtB deposition) post fabricated on the pixel pad (*e.g.*, Fig. 15, top right). This post fabrication involves photolithography to define the hole, dry etching of the foundry passivation to expose the Al pad, deposition of 20 nm Ti and 200 nm Pt, and lift-off [31]. The pixel op-amp was configured as a buffer to measure the voltage ripple during the current injection. We increase f_{SC} from 0 Hz to 1 kHz and then decrease it back to 0 Hz, all in 200 Hz increments (Fig. 12, bottom). This results in ~5 pA step current increases/decreases for positive/negative injections (Fig. 12, top). The ripple voltage can be clearly seen (Fig. 12, middle at f_{SC} = 600 Hz), with ~20 mV step size for both positive and negative injections. This ripple voltage for the 2 μm diameter Pt electrode with C_L = 1.7 pF is much larger (est. 50×) than the ripple voltage for the PtB electrode that has a much larger C_L due to its rough surface texture that increases its surface area. These time-dependent behaviors of $|\overline{I_{OUT}}|$ and V_{OUT} are consistent with the theoretical considerations of Sec. IV-B (Fig. 6).

C. Measurement of pCC and pVC Amplifiers

The pCC amplifier configuration was first tested to investigate the optimal number of feedback dps for voltage amplification: the input ($V_{s,1}$) output (V_{amp}) DC transfer curve was measured for each of the 0 to 7 dps options across the array (Fig. 13a). This test is important to ensure array-wide operation: leakage currents across the multiple feedback dps can induce offset voltages that can saturate the amplifier, reducing the number of available pixels. Sharp transitions of the array wide median $V_{amp,DC}$ from the lower (0.2 V) to upper (2.8 V) output voltage rails for increasing the number of feedback dps show their sensitivity to the leakage currents (Fig. 13a, right). To overcome this sensitivity, not only do we choose the optimal number of feedback dps but we also use the dp connected to $V_{s,4}$ to set a current across the feedback dps to tune their offset and impedance.

For the extracellular recording of the membrane potential (this is done later in Section VI by setting $I_e = 0$ in the pCC configuration so as not to cause membrane permeabilization), we use 2 feedback dps in parallel to C_2 = 5 fF to set a passband gain of 275 V/V with a

bandwidth f_1 = 100 Hz to f_2 = 5 kHz (Fig. 13b). The 100-Hz pole substantially filters out the 1/ f noise, given that the open-loop amplifier has a 1/ f noise corner of ~10 Hz. The measured input referred noise is 5.6 μV_{rms} when integrated from 1 Hz to 4.7 kHz (Fig. 13b).

The pCC intracellular recording mode (done later in Section VI with non-zero I_e) must deal with larger amplitude signals (ΔV_e > 1 mV or ΔV_{amp} > 300 mV). In this case, since the 2 feedback dps exhibit non-linear clipping, we instead use 6 feedback dps to lessen the voltage seen on each dp with large output voltages. In this configuration, the feedback current is especially essential to control $V_{amp,DC}$ across the array that would otherwise be saturated due to the sharp slope observed in Fig. 13a with 6 dps. With this measure, signals as large as ΔV_e > 20 mV can be recorded without distortion. On the other hand, the large impedance of the 6 dps causes f_1 < 1 Hz; this lets in a larger amount of 1/ f noise (as the open-loop amplifier has the 1/ f corner at ~10 Hz), resulting in an increased integrated input referred noise of ~23 μV_{rms} at A_v = 30 V/V (Fig. 13b). Digital filters can reduce this additional low frequency noise depending upon the signal frequencies of interest (*e.g.*, PSPs range from ~100 Hz to 1 kHz).

Figure 14 shows the characterization of the pVC transimpedance amplifier. Input current, I_{in}, is applied using $V_{s,4}$ through C_1 = 3.5 pF (Fig. 14a, left) to measure the transimpedance gain R_{TIA} ~ 700 MΩ for $f_{SC,pVC}$ = 4 $f_{s,pixel}$ = 37.6 kHz and for $V_{s,1}$ = 1.0 V ~ 2.4 V (Fig. 14a, right). The bandwidth of the transimpedance amplifier extends from DC to 2 kHz set by R_{TIA} and C_2 = 100 fF (Fig. 14b, left) with an input referred noise as low as 1.1 pA_{rms} integrated from 1 Hz to 4.7 kHz (Fig. 14b, right). Gain and noise measurements across the array show a distinct spatial dependency due to multiplexer sampling and its relation to the clock phases (Fig. 14c): pixels which are sampled during Φ_1 exhibit larger noise and gain in comparison to Φ_2. These variations could be optimized in future designs by incorporating a dedicated switched feedback element synched to the multiplexer in the pixel circuit and using a traditional integrate and reset method for the lowest noise performance [35].

D. Characterization of Electrode and Routing Capacitance

For optimal pCC and pVC coupling [Eqs. (1)–(4)], we desire a small electrode impedance (Z_e) or a large electrode capacitance C_e. Concretely: $C_e \gg (C_{p,r} + C_1)$ is the condition to obtain the final expression in Eq. (1), eliminating the attenuation due to the electrode; and $|Z_e| \ll R_s, R_{jm}$, is the condition to obtain the final expressions of Eqs. (3) and (4) with no attenuation due to the electrode. To minimize Z_e (*i.e.*, to increase C_e), PtB is electrodeposited onto Pt electrodes post fabricated on the Al pads, as the surface roughness of PtB increases the electrode surface area (*e.g.*, Fig. 15, right) [31]. For the PtB deposition, $V_{s,1}$ is used to apply a voltage ramp to V_e from 0 V to −1.2 V at 50 mV/s with respect to a Pt reference in a solution of 0.5 mM H_2PtCl_6 and 25 mM $NaNO_3$ [36]. Z_e is measured across the array periodically throughout the deposition by applying a 1–25 mV 5 kHz sine wave sequentially to each pixel and measuring the resultant current through the reference electrode (Fig. 15, left). Z_e is reduced by almost 2 orders: *e.g.*, in Fig. 15, it is reduced to ~300 kΩ (C_e ~ 100 pF).

This C_e satisfies $C_e \gg (C_{p,r} + C_1)$ for the final expression of Eq. (1) to hold, with C_1 ~ 3.5 pF and $C_{p,r}$ ~ 600 fF - 2 pF, depending on the routing length. We extract this $C_{p,r}$ by comparing the amplifier gain measured from $V_{s,1}$ to V_{amp} with C_1 connected to $V_{s,4}$ at ground and the same gain but with C_1 connected to V_e (Fig. 16). Also $|Z_e| \ll R_s, R_{jm}$ for Eqs. (3) and (4) is satisfied with R_s and R_{jm} in the MΩ range. The electrode-to-electrode coupling was also measured in a similar manner by applying a 1-V AC signal to all V_e but the pixel measured: a total of 3.0 fF of electrode-to-electrode capacitance was measured, of which, 2.3 fF was due to adjacent electrode pads while 0.7 fF was from pixel circuit to electrode routing cross-coupling capacitance.

Beyond reducing Z_e, the surface roughness of the PtB also strongly interacts with the cell membrane to form a tight seal [31], increasing R_s. This not only further ensures $|Z_e| \ll R_s, R_{jm}$ for Eqs. (3) and (4) to be valid for the pVC operation, but also reduces the attenuation of the pCC recording [Eq. (1)] and enhances the pCC stimulation effectiveness [Eq. (2)].

VI. Electrophysiological Measurements

We demonstrate pCC and pVC intracellular recording and stimulation with dissociated rat neurons, cultured on the IC for 10–14 days *in vitro*. We use PtB vertical nanoneedles for pVC and PtB vertical nanoneedles with pad edge electrodes for pCC [31]. Fig. 17 shows an example *extracellular* signals recorded using the high-gain, low-noise voltage amplifier configuration of our CMOS IC—-similar to other CMOS MEAs [1], [2], [11]–[14], [3]–[10] —-as a reference for comparison to the intracellularly recorded signals we will present now.

A. pCC Neuron Measurements

To demonstrate the pCC operation, we first determined the threshold I_e needed for intracellular access by changing I_e from 0 ~ −3.0 nA with a step of −150 pA and measuring V_e with the rat neurons on top (Fig. 18a). The threshold I_e was determined when V_e substantially increased and APs were clearly distinguished (Fig. 18a). The intracellular threshold so determined lied between −1.1 to −2.2 nA across the array.

To quantify the overall noise at the electrode beyond the input referred noise of the pCC amplifier, we performed two types of experiments. First, we measured V_e for various bandwidths again by changing I_e from 0 ~ −3.0 nA, but this time without a neuron above (Fig. 18b, left shows the data for an example pixel). Second, we measured V_e with the I_e below the intracellular threshold so that no intracellular coupling occurs even if there is a neuron above (Fig. 18b, right shows the data across the array). These experiments show that on top of the ~23 μV_{rms} input referred noise of the pCC intracellular-mode amplifier (Section V. C), there is an additional noise of 40 ~ 150 μV_{rms} largely below 10 Hz in frequency. This extra noise originates from the electrode (~10 μV_{rms}), solution (~30 μV_{rms} [12]), and the current injector's ripple voltage (0 ~ 110 μV_{rms}, dependent upon $|I_e|$). If the clock of the switched-capacitor current injector and that of the output multiplexer were perfectly synchronized, the ripple voltage noise would disappear in its entirety (Section IV. D), but in reality, the two clocks slightly drift from each other at low frequencies below 10

Hz, which aliases the ripple voltage into the recording noise at the low frequencies. The non-uniformity of the noise across the array (Fig. 18b, right) is attributed to variations in f_1 arising from feedback diode leakage current variation. By comparing this overall noise to the AP amplitudes of 1 ~ 30 mV measured at the electrode in the pCC intracellular mode (*e.g.*, Fig. 18a, right), we obtain a signal-to-noise ratio > 20, on par with the patch clamp. The signal-to-noise ratio for PSPs is also > 1, so subthreshold (synaptic) signal measurement is also possible. An example of such subthreshold sensitivity is shown in Fig. 18c, where excitatory PSPs (EPSPs) are clearly measured with ΔV_e amplitudes of ~200 μV to ~1 mV at the electrode.

A stimulation experiment with intracellular coupling at $I_e \sim -1.1$ nA with periodic +550 pA injections (Fig. 18d), during which increased neuron AP firings are observed, demonstrates the ability to intracellularly record ΔV_e and adjust I_e simultaneously to stimulate the neuron through the same electrode.

The scalability of the device for network-wide intracellular recording was demonstrated with intracellular measurement of more than 1,700 neurons in parallel for a > 40% intracellular coupling rate [31]. The subthreshold sensitivity enabled cross-pixel AP to PSP correlation that allowed mapping of 304 synapses between 396 neurons, which demonstrates the capability of the IC for synaptic connectivity mapping applications [31].

B. pVC Neuron Measurements

To demonstrate the pVC operation, we gradually increased the magnitude of V_e to determine the threshold for intracellular access (Fig. 19). Since no spontaneous activity is observed for pVC due to its low input impedance, voltage stimulations were applied to activate the neuron's ion channels: at $V_e = -0.65$ V to −0.7 V distinct Na^+ spikes and K^+ repolarization currents are observed during stimulation, clearly distinguished in the high-pass (100 Hz) filtered version of the measured electrode current, ΔI_e. The pVC mode clearly enables the ability to measure I_e and adjust V_e simultaneously, allowing for concurrent intracellular recording of ion channel currents and stimulation of membrane potentials.

Such intracellular ion-channel measurement of mammalian neurons can be useful for high-throughput drug screening applications, where current high-throughput intracellular tools, *i.e.*, the planar patch clamp, are limited to non-neuronal, artificial cell lines. As a first demonstration towards this end, we measured the effects of ion-channel drugs affecting both the Na^+ and K^+ currents of the dissociated rat neurons [31].

VII. Conclusion

We have presented the CMOS IC that contains 4,096 pCC/pVC pixel circuits, with each connected to a PtB electrode. The electrodes form a dense, 20 μm pitch 64 × 64 array. Overall the IC enables large-scale intracellular recording of neurons with the ability of simultaneous excitations. It is the flexibility of the pixel circuit, containing a new switched-capacitor based current injector and a highly configurable op-amp, that enables both the pCC and pVC modes within each pixel circuit. The lateral separation of the pixel circuit from electrode decouples the electrode pitch from the larger pixel circuit area for the low noise

design with the high configurability. The device has been fabricated in 0.18 μm CMOS technology, electrically characterized, and verified biologically with *in vitro* rat neurons. We summarize and compare the performance of this CMOS nanoelectrode array to start-of-the-art CMOS MEAs as well as our prior CMOS nanoelectrode array in Table II [3]–[6], [14], [25].

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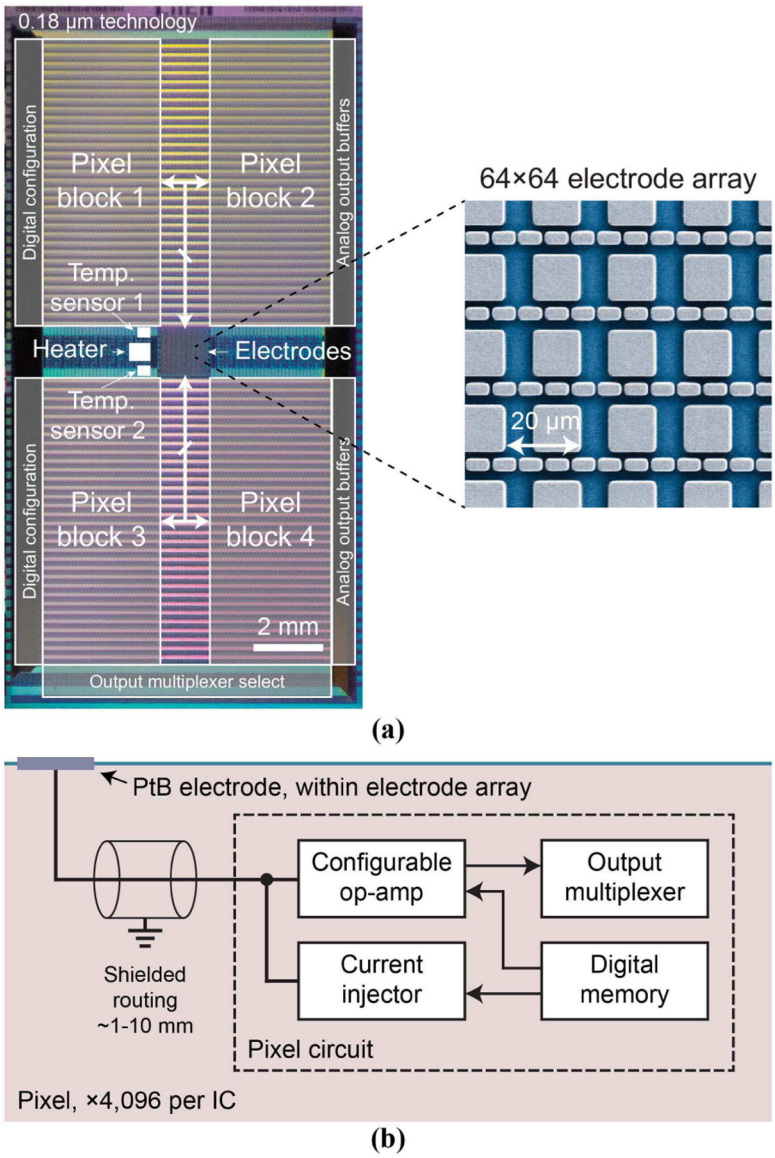

Fig. 1.

(a) Chip micrograph (10 × 20 mm^2) along with a false colored scanning electron microscope (SEM) image of the 4,096 Al pads before post fabrication of PtB electrodes. (b) Block diagram of an active pixel circuit.

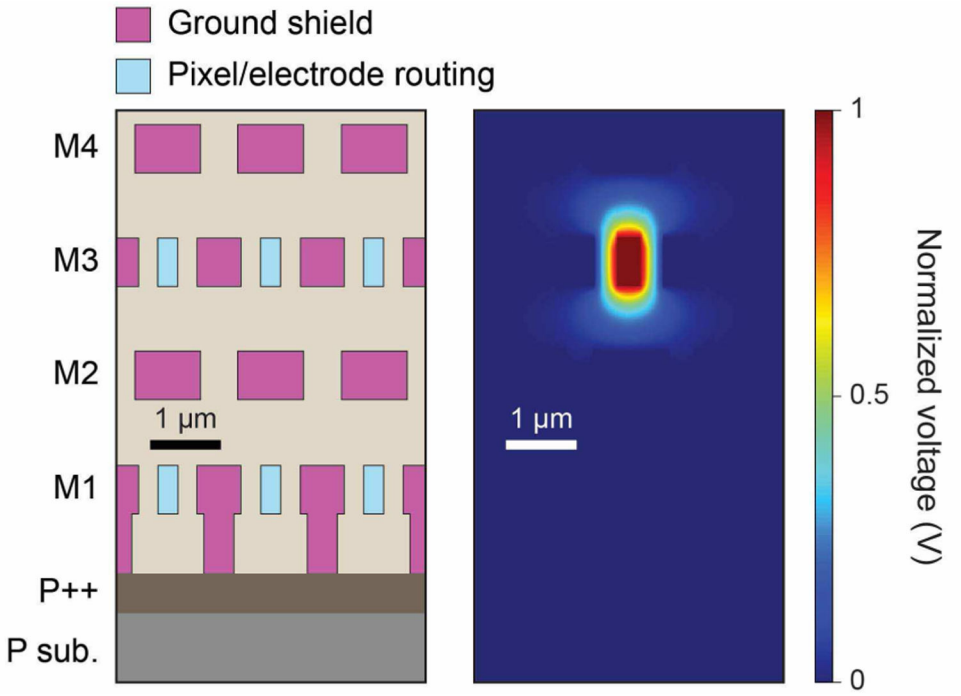

Fig. 2.

(left) Cross section of the densest pixel circuit to electrode routings using the bottom four metal layers; M5-M6 are used for other routings. (right) Electric field simulation to calculate the routing parasitic capacitance.

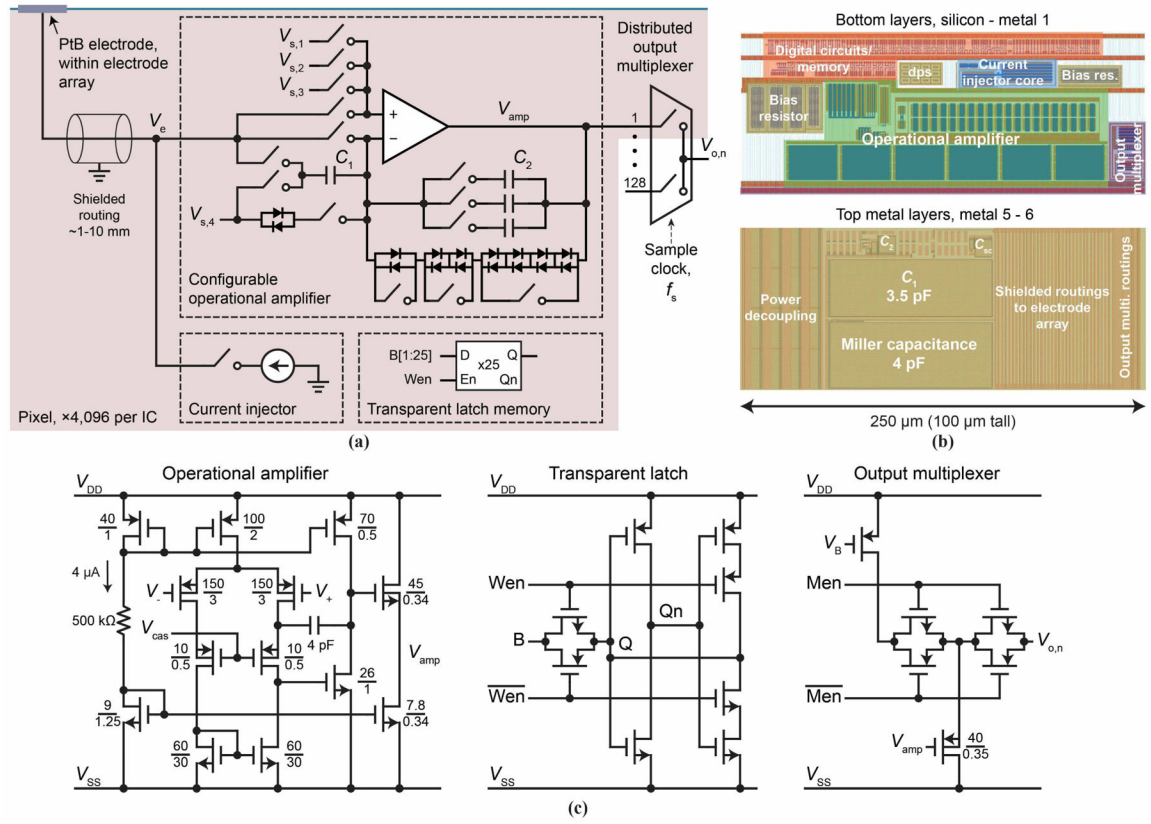

Fig. 3.

(a) Active pixel circuit schematic. The switches (transmission gates) are controlled by the transparent latch memory to configure the pixel for experiments. C_1 = 3.5 pF; C_2 has the options of adding any of ~5 fF, ~20 fF, and ~100 fF. (b) Active pixel circuit layout. Metal-insulator-metal capacitors are identified on the topmost metal layers. (c) Transistor-level schematics of various pixel components, in particular, op-amp (left), transparent latch (middle), and output multiplexer (right); the schematic of the current injector is shown in detail in Fig. 7.

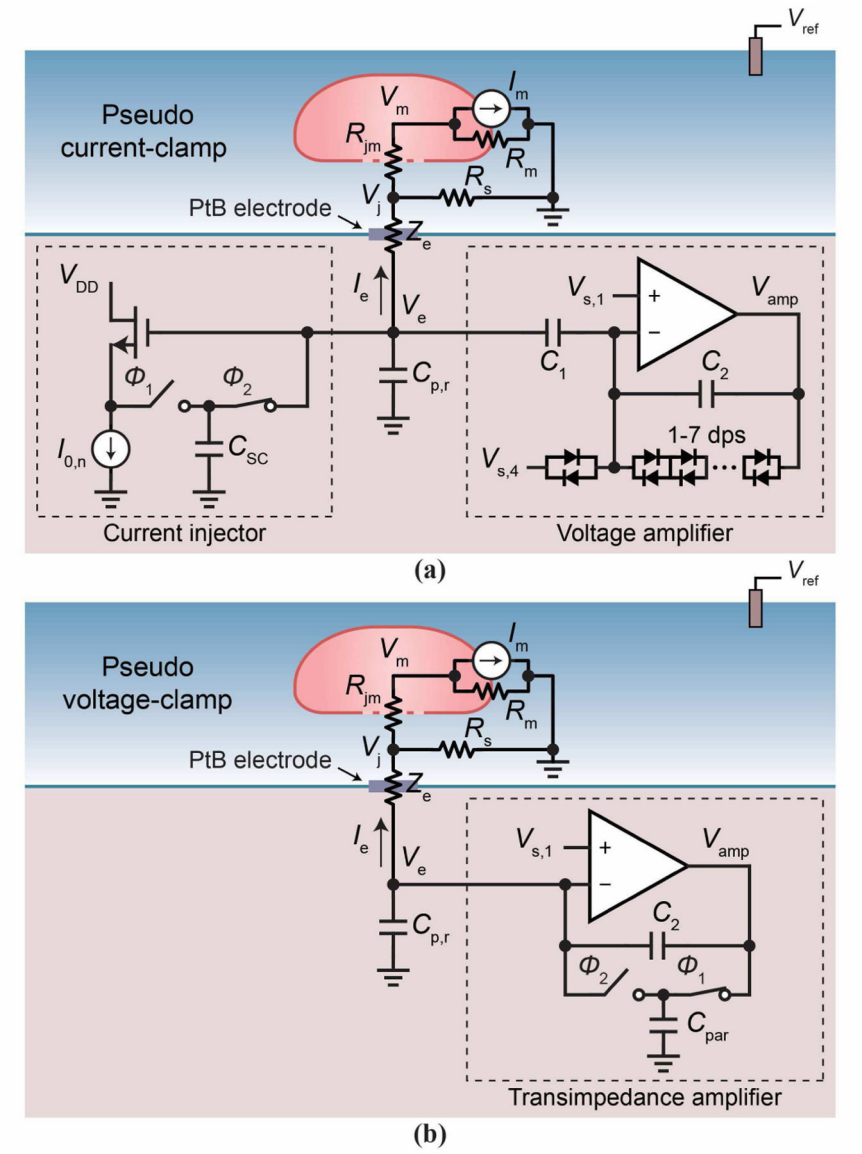

Fig. 4.

(a) The pCC pixel configuration. (b) The pVC pixel configuration.

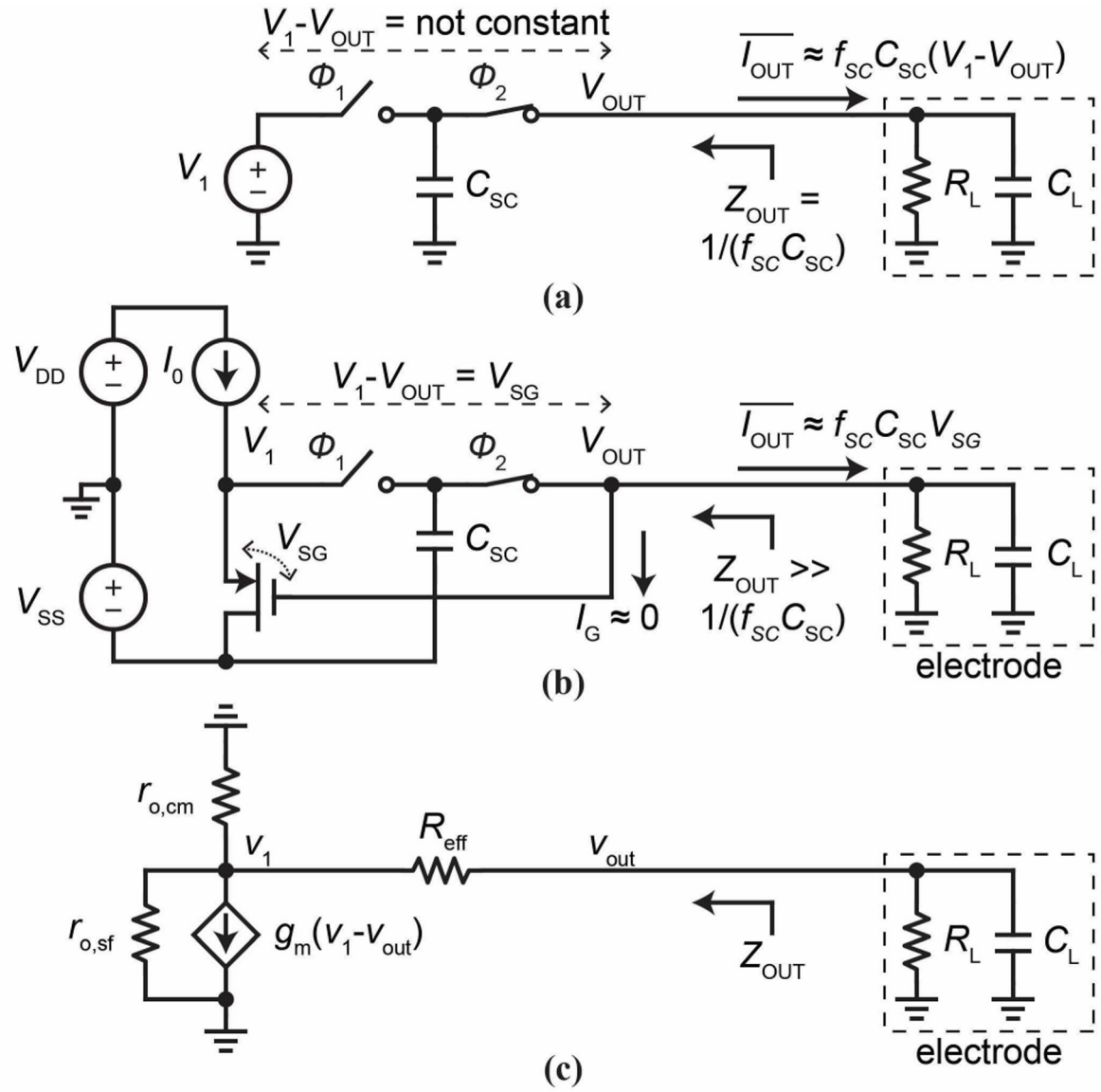

Fig. 5.

(a) Switched capacitor driving an electrode. (b, c) Switched capacitor with active circuit to increase output impedance and its small-signal model.

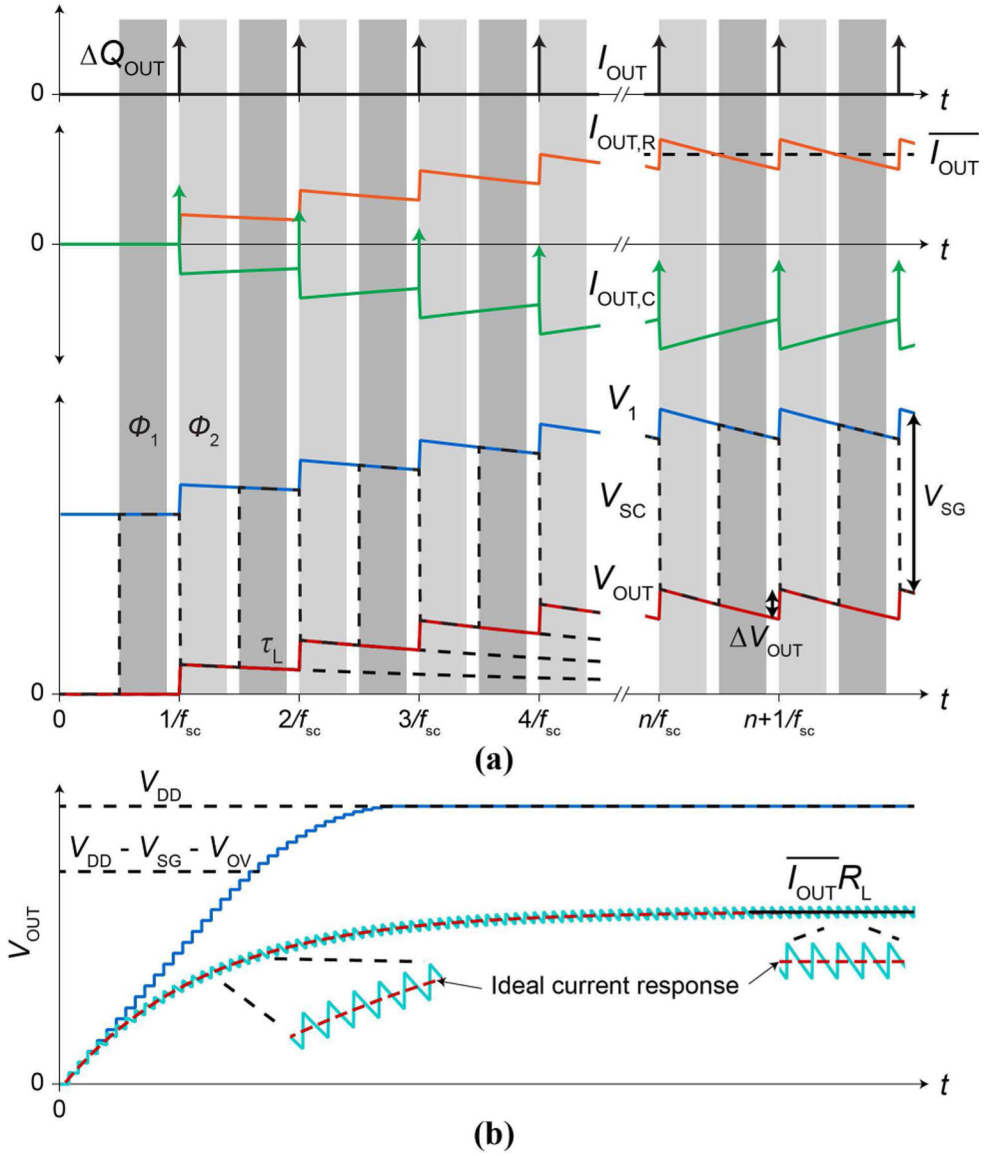

Fig. 6.

(a) Timing diagram for I_{OUT}, $I_{OUT,R}$ $I_{OUT,C}$, and V_1, V_{SC}, V_{OUT}. (b) $V_{OUT}(t)$ for the R_LC_L load (cyan, solid) in juxtaposition with $V_{OUT}(t)$ for a C_L-only load (blue, solid). The response of the R_LC_L load to an ideal step current is overlaid (red, dashed) for comparison.

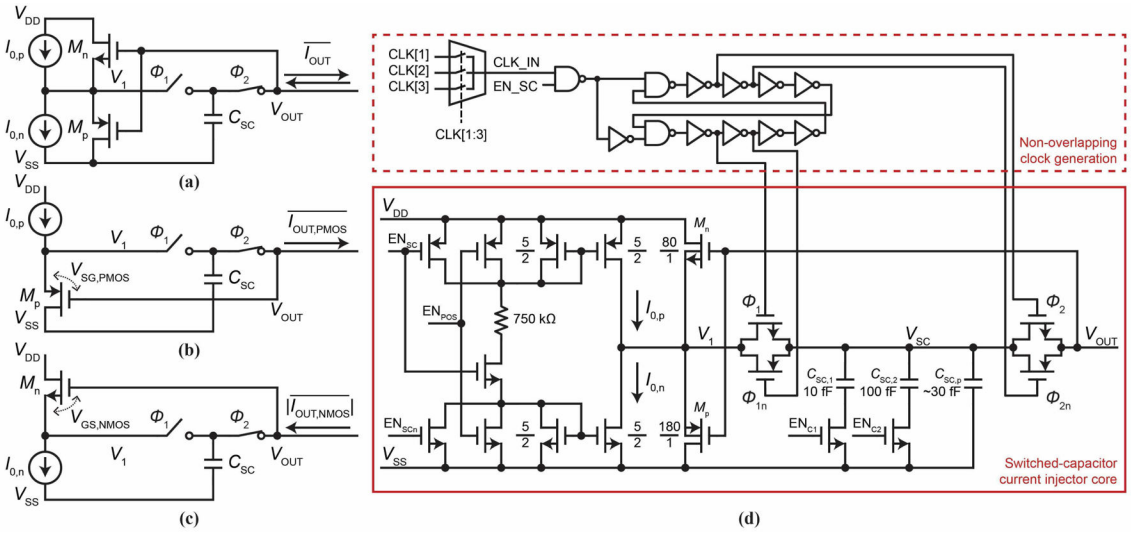

Fig. 7.

(a) The current injector we implement. (b) With $I_{0,p}$ on and $I_{0,n}$ off, part (a) is reduced to what is shown here, capable of positive current injection. (c) With $I_{0,n}$ on and $I_{0,p}$ off, part (a) is reduced to what is shown here, capable of negative current injection. (d) Transistor-level schematic of the current injector including the non-overlapping clock generation circuit. Control signals CLK[1:3], EN_{SC}, EN_{POS}, EN_{C1}, and EN_{C2} are controlled by the pixel's transparent latch memory.

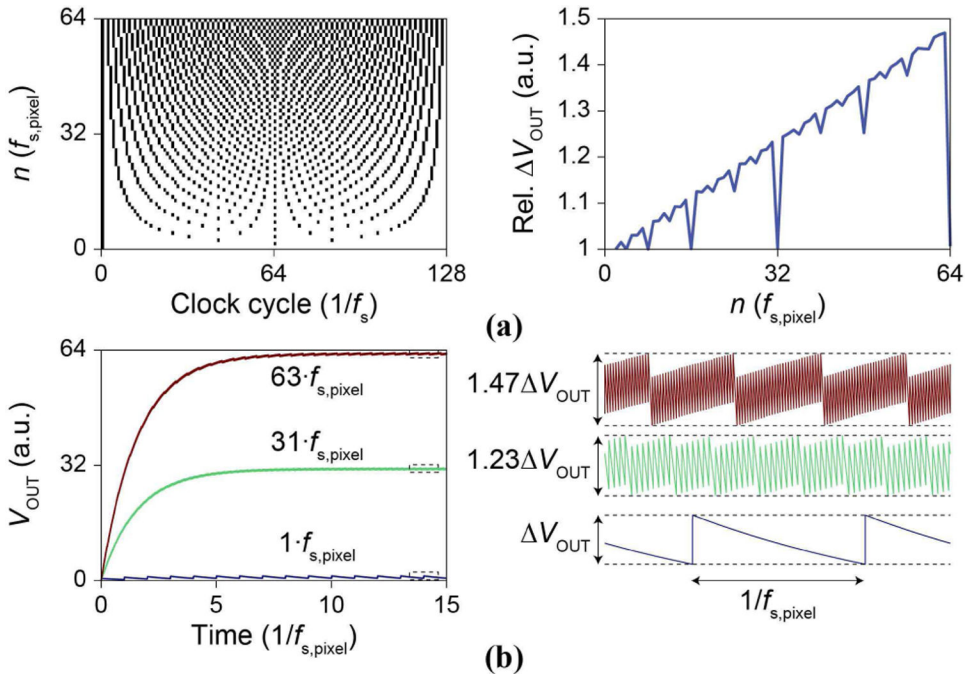

Fig. 8.

(a, left) pCC clocking scheme to synchronize the switched-capacitor current injector's f_{sc} to the multiplexer sampling at f_s. Black indicates f_{sc} high, white indicates f_{ss} low. The clock sequence is repeated after $128/f_s$. (right) ΔV_{OUT} is increased due to the scheme. (b) Simulated V_{OUT} traces for positive current injection for three different magnitudes and their steady state $V_{OUT}(t)$ ripple voltage.

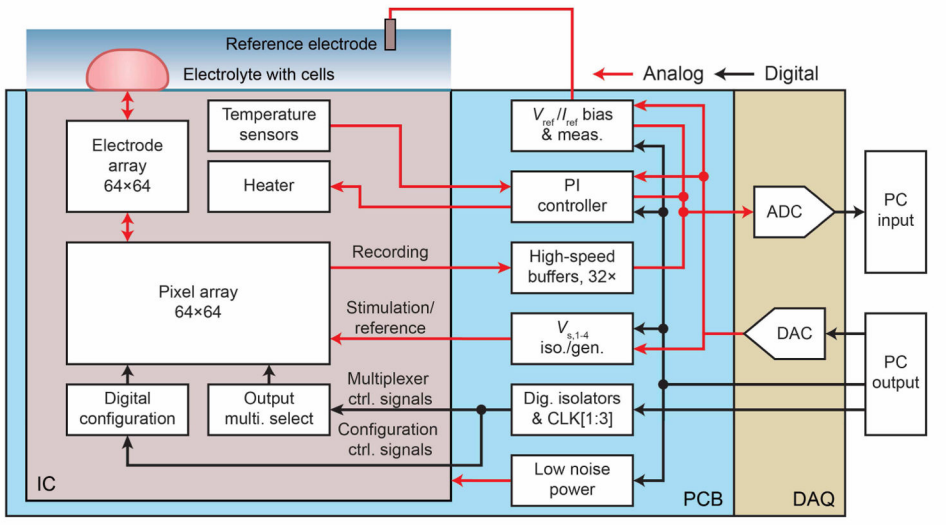

Fig. 9.

System architecture of the IC and external electronics showing analog and digital signal flow.

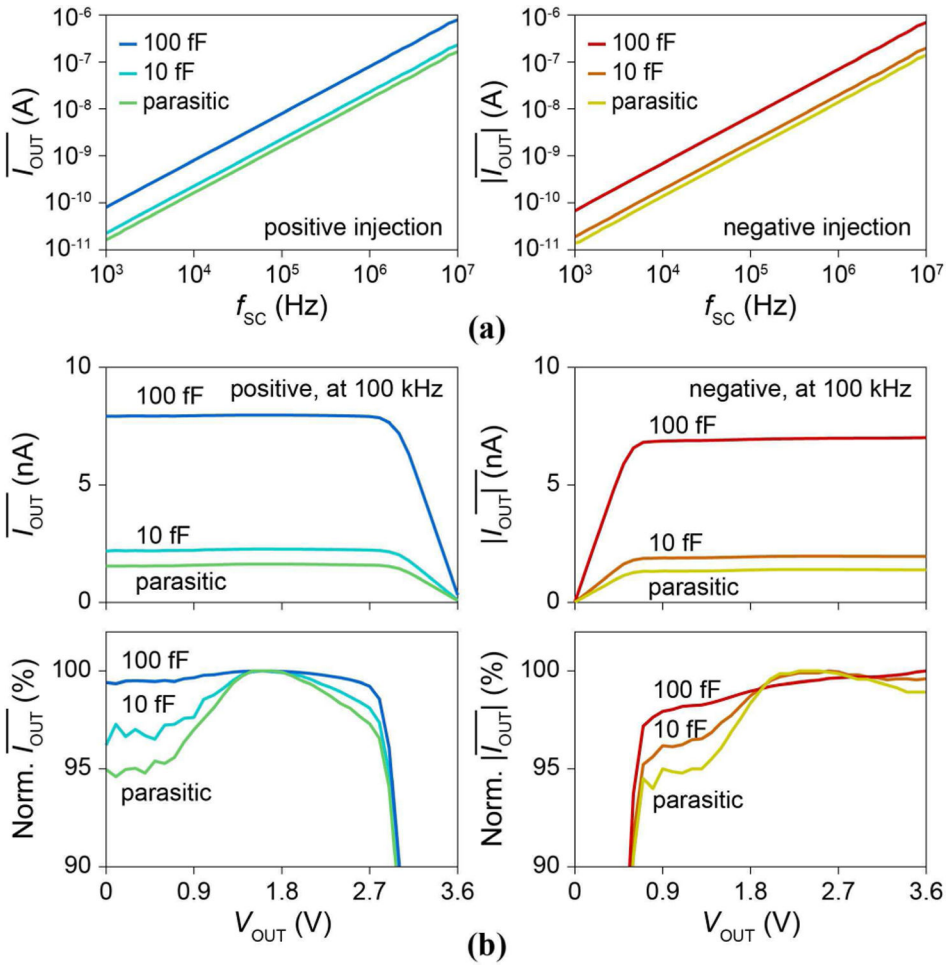

Fig. 10.

(a) Positive and negative $\overline{I_{OUT}}$ vs. f_{SC} for V_{OUT} = 1.8 V. (b) Positive and negative $\overline{I_{OUT}}$ vs. V_{OUT} for f_{SC} = 100 kHz.

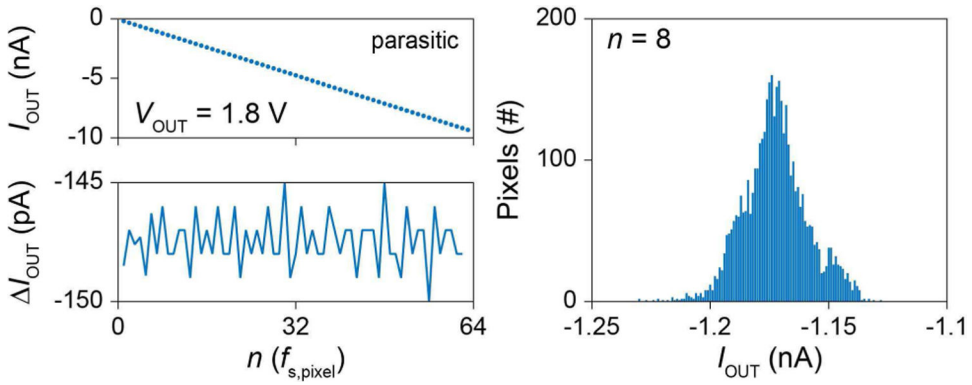

Fig. 11.

(left) I_{OUT} vs. n of the pCC clock synchronization scheme. (right) Distribution of I_{OUT} at n = 8 for all 4,096 pixels, bin size of 1 pA.

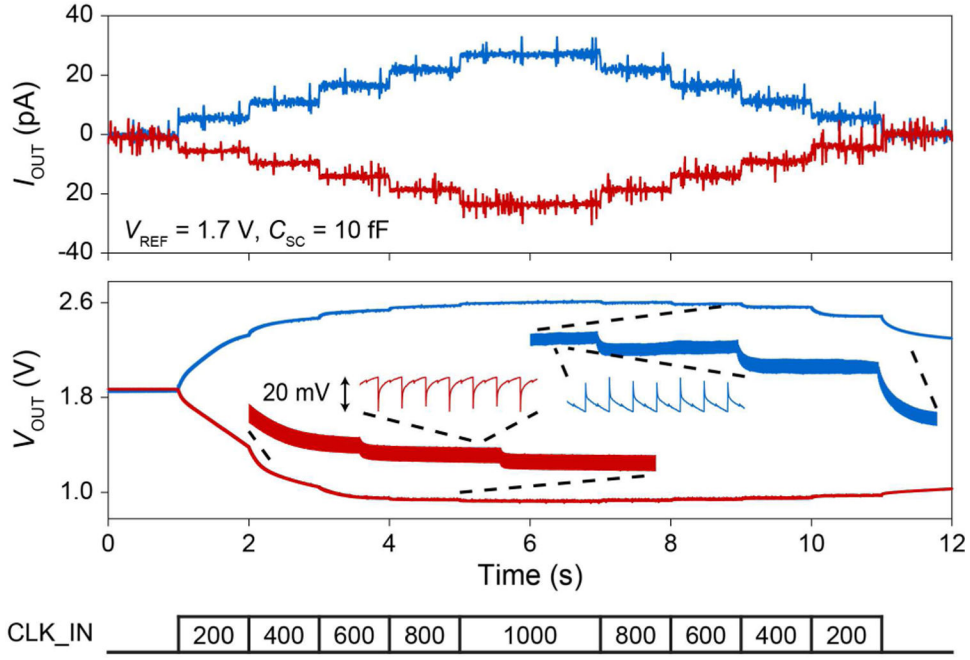

Fig. 12.

Small amplitude current injection measurement in solution with a post-fabricated Pt electrode. An Ag/AgCl reference was used at V_{REF} = 1.7 V to set V_{OUT} to ~1.8 V. The insets show the ripple voltage of V_{OUT} for f_{SC} = 600 Hz.

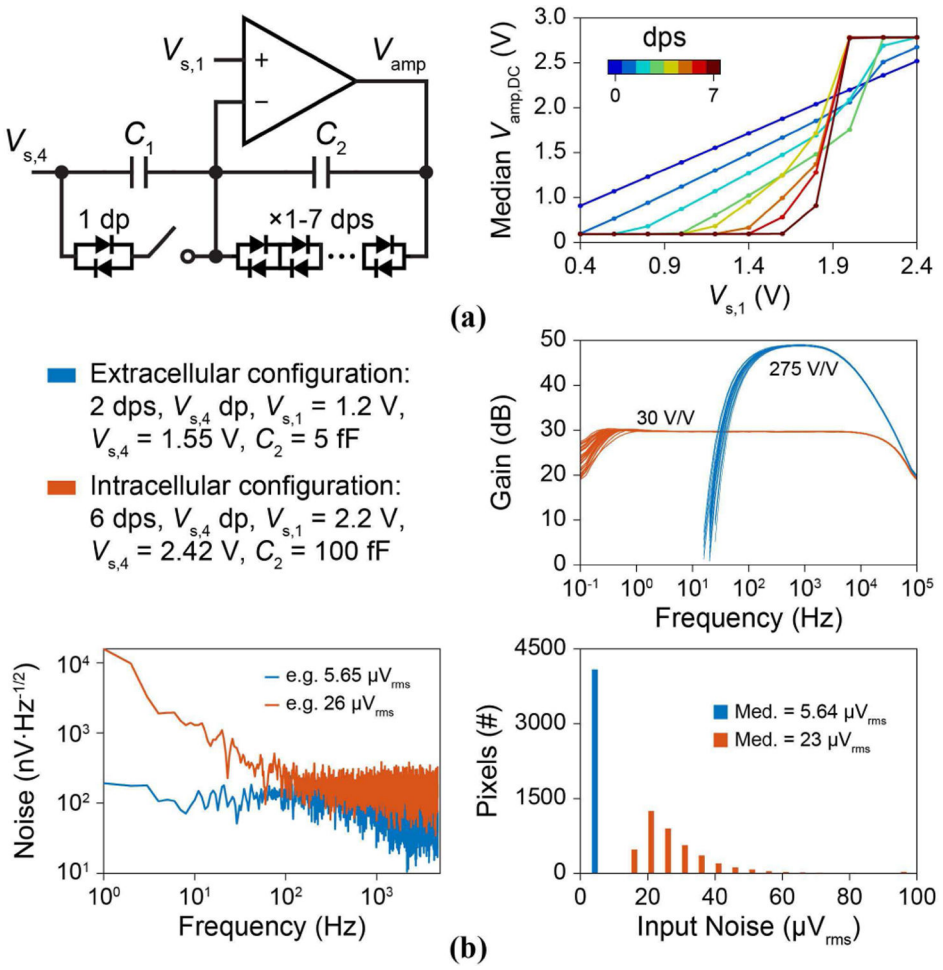

Fig. 13.

pCC amplifier characterization. (a) The array's median $V_{amp,DC}$ vs. $V_{s,1}$ for each of the 1-to-7 feedback dp options (without the $V_{s,4}$ dp). (b) Measurements of the extracellular and intracellular configurations: gain vs. frequency for 32 pixels, input referred noise for a single example pixel, and input referred noise integrated from 1 Hz to 4.7 kHz across the array.

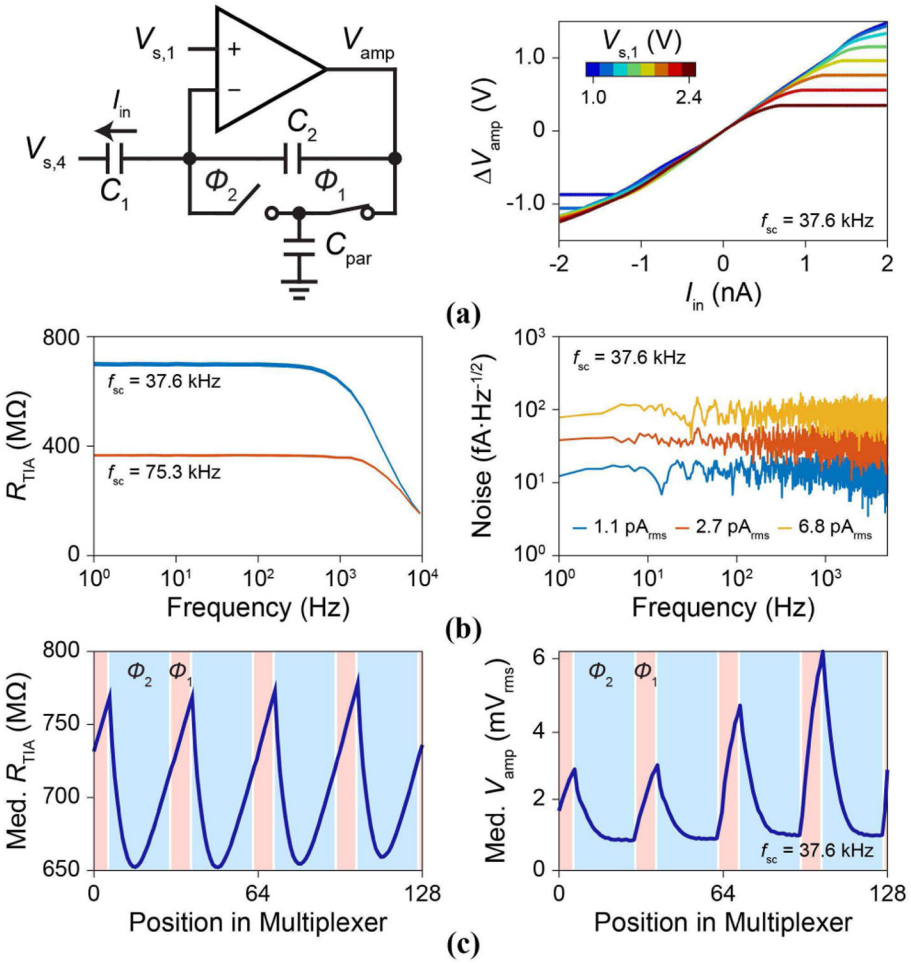

Fig. 14.

(a, left) pVC transimpedance amplifier measurement setup. (right) Measured transimpedance with 2.5-ms Iin pulse inputs ($V_{s,1}$: 1.0 ~ 2.4 V). (b, left) Transimpedance gain, R_{TIA} vs. frequency for 32 pixels for $f_{SC,pVC}$ = 37.6 kHz and 75.3 kHz. (right) Input referred current noise for 3 pixels. (c) Median R_{TIA} and V_{amp} voltage noise of 128 pixels sharing an output multiplexer.

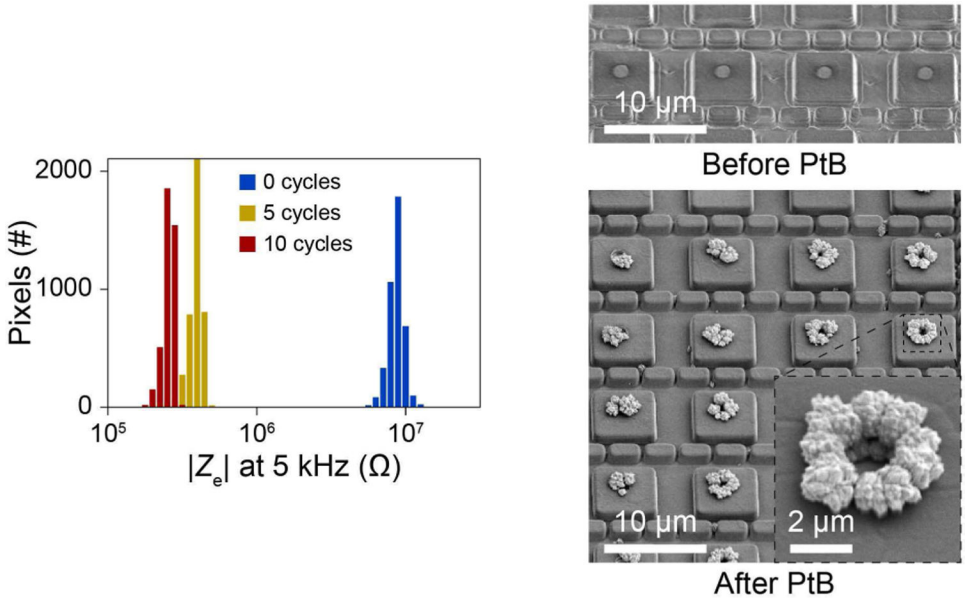

Fig. 15.

(left) $|Z_e|$ at 5 kHz measured across the array during PtB deposition. (right) SEM images of planar hole electrodes before and after PtB deposition.

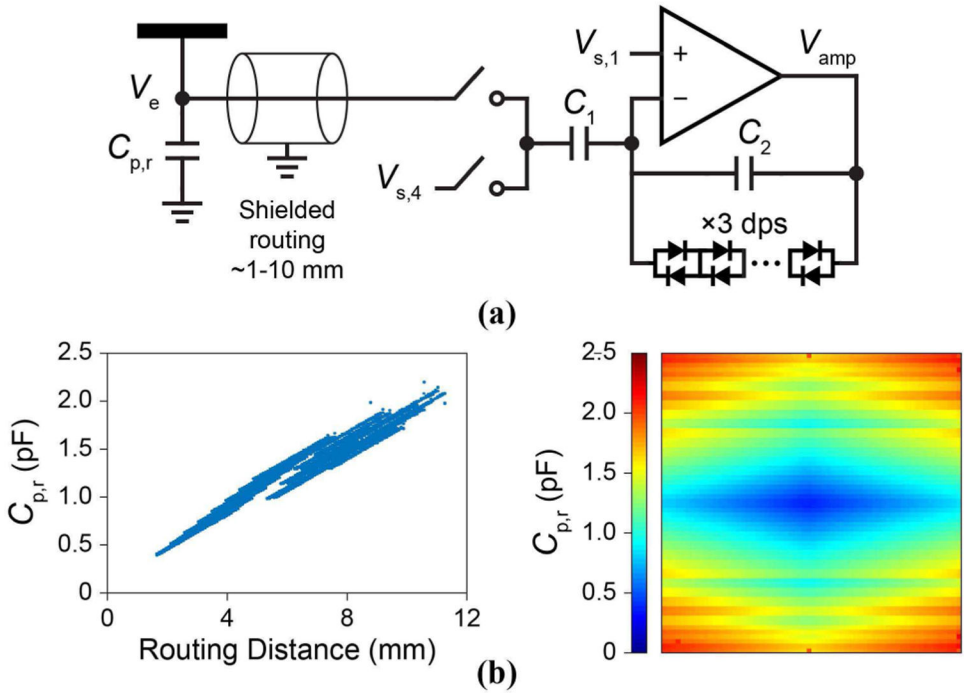

Fig. 16.

(a) The configuration for measurement of $C_{p,r}$. (b, left) Dependence of $C_{p,r}$ on the electrode pixel routing distance. (right) Heat map across the array.

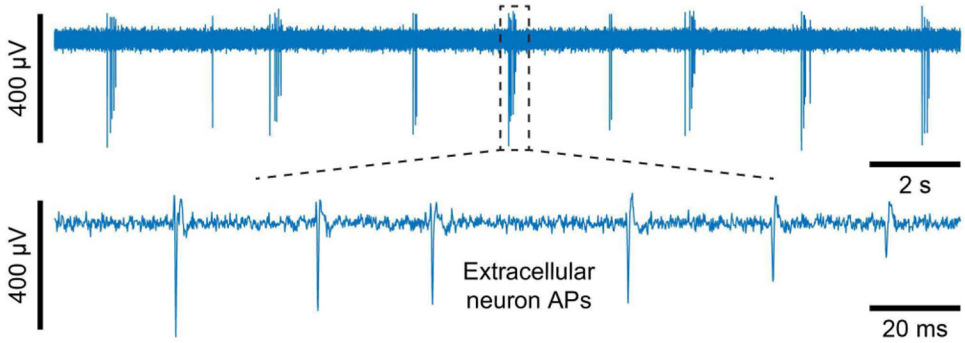

Fig. 17.

Example of extracellular recording of a dissociated rat neuron using a PtB planar hole electrode.

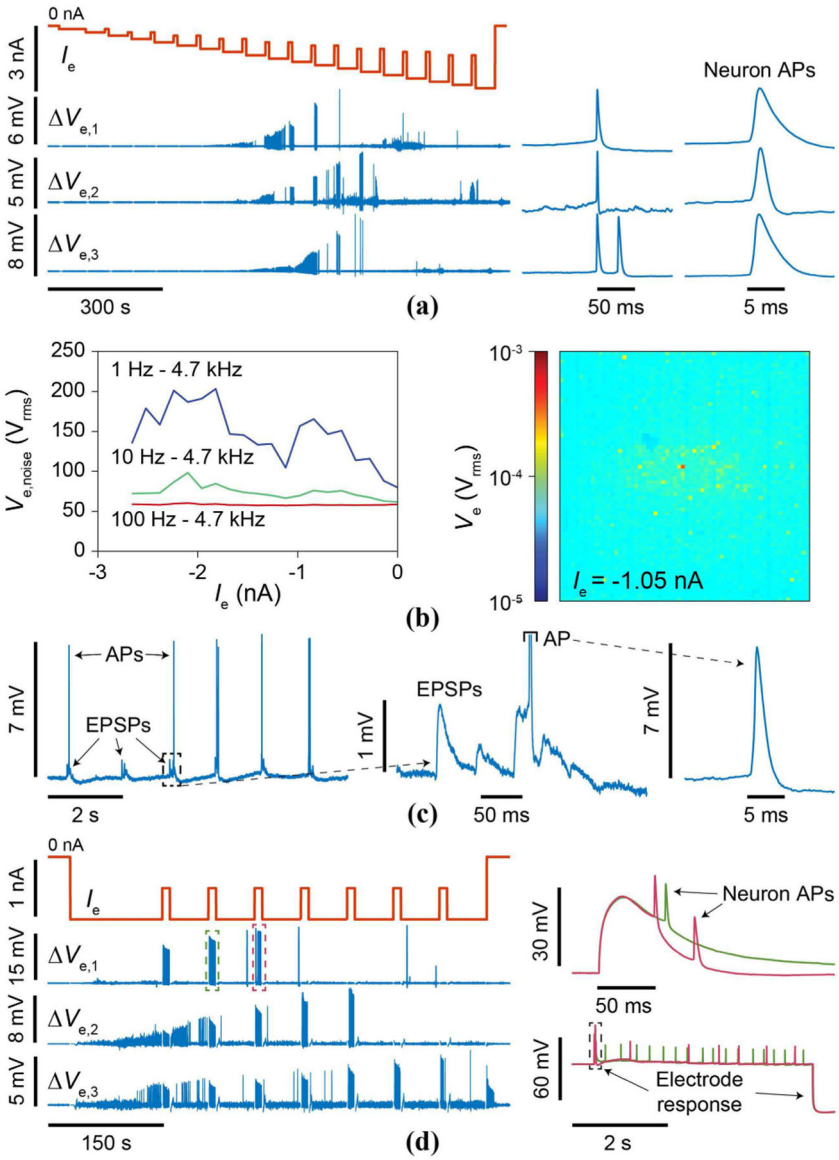

Fig. 18.

(a) Ramped experiment to determine intracellular threshold I_e with dissociated rat neurons. (b) Integrated $V_{e,noise}$ for an individual pixel without an interfacing neuron (left) and V_e amplitude integrated from 100 Hz - 4.7 kHz across the array below threshold for the experiment of (a). (c) Excitatory PSP (EPSP) measurement. (d) Stimulation is achieved through adjustment of I_e.

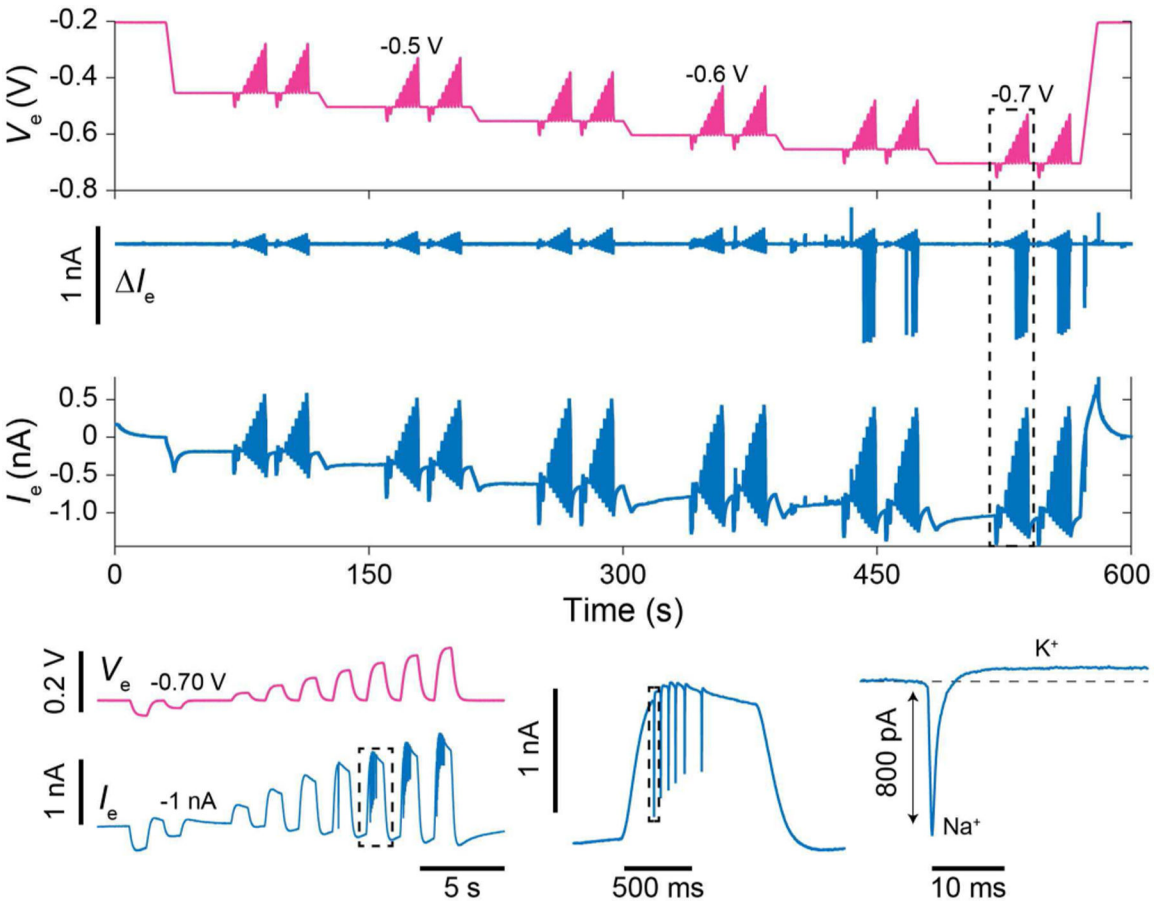

Fig. 19.

Ramped V_e experiments in the pVC configuration to determine threshold for intracellular access using a PtB nanoneedle electrode and dissociated rat neurons. V_e stimulations are applied to activate ion channels.

TABLE I

POWER CONSUMPTION OF THE CMOS DEVICE

Circuit	Power/Circuit
Operational amplifier (x4096)	225 μW
Current injector (x4096)	24 μW
Output multiplexer (x32)	7.3 mW
Fully enabled array power consumption	**1.25 W**
Maximum heater power	1.3 W
Typical heater power to maintain 35°C	0.55 – 0.85 W

TABLE II

PERFORMANCE COMPARISON OF STATE-OF-THE-ART CMOS MICRO AND NANO ELECTRODE ARRAYS

		[3]	[4], [14]	[5]	[6]	[25] (Our prior work)	This work
Technology node		**0.18 µm**	**0.18 µm**	**0.13 µm**	**0.13 µm**	**0.35 µm**	**0.18 µm**
Electrode shape		**Planar microelectrode with surface roughness**	**Planar microelectrode**	**Planar microelectrode**	**Planar microelectrode**	**Vertical nanoelectrode**	**Vertical nanoelectrode with surface roughness**
Electrode pitch		13.5 µm	25.5 µm	58 µm	15 µm	126 µm	20 µm
No. electrodes		59,760	65,536	1,024	16,384	1,024	4,096
No. recording channels		2,048	65,536	4	1,024	1,024	4,096
Cell-electrode interface modality	Extracellular voltage recording	Yes	Yes	Yes	Yes	Yes	Yes
	Intracellular voltage recording with no concurrent stimulation	-	-	-	Yes (cardiomyocyte)	Yes (cardiomyocyte)	Yes (cardiomyocyte)
	Intracellular voltage recording with current injection (current clamp)	-	-	-	-	-	Yes (neuron)
	Intracellular current recording with voltage application (voltage clamp)	-	-	-	-	-	Yes (neuron)
	Constant voltage stimulation (CVS)	Yes	Yes	-	Yes	Yes	Yes
	Constant current stimulation (CCS)	Yes	-	Yes	Yes	-	Yes
	Impedance monitoring	-	-	-	Yes	-	-
	Impedance spectroscopy	Yes	-	Yes	Yes	-	-
	Chemical	Yes	-	-	-	-	-
No. stimulation waveform generation units		16 (V or I)	External (V)	4(I)	64 (V) + 64 (I)	External (V)	External (V) + 4,096 (I)
No. stimulation waveforms		6 (V or I)	1(V)	4(I)	64 (V) + 64 (I)	3 (V)	3 (V) + 3 (I)
No. sites for simultaneous CVS		N/A	65,536	-	4,096	1,024	4,096
No. sites for simultaneous CCS		6	-	4	64	-	4,096
CVS/CCS range		±1.5 V/±300 µA	3.3 V/-	- / ± 32 µA	± 1.65 V/± 382.5 nA	4 V/ -	3 V / ± 300 µA

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		[3]	[4], [14]	[5]	[6]	[25] (Our prior work)	This work
Technology node		**0.18 µm**	**0.18 µm**	**0.13 µm**	**0.13 µm**	**0.35 µm**	**0.18 µm**
Electrode shape		**Planar microelectrode with surface roughness**	**Planar microelectrode**	**Planar microelectrode**	**Planar microelectrode**	**Vertical nanoelectrode**	**Vertical nanoelectrode with surface roughness**
CVS/CCS resolution (LSB)		2.9 mV/ 29 nA	N/A	250 nA	103 mV/2 pA	-	- /5pA (140 pA for PCC)
Channel gain		30–7000	50–250	22–412	2–3000	150–375	30–275
Channel bandwidth (maximum)		1 Hz- 10kHz	100 Hz – 10 kHz	0.1 Hz-26 kHz	0.5 Hz −10 kHz,	1 Hz-5kHz	<1 Hz to 30 kHz
Input-referred noise (rms)	Full band	5.4 µV		12.6 µV	12 µV	250 µV	23 µV
	AP band	2.4 µV	10 µV	7 µV	7.5 µV		5.6 µV
ADC		10b @ 20 kS/s	External	External	10b @ 20 kS/s	External	External
Temperature control		Yes (temp, sensor)	-	-	-	-	Yes (temp, sensor with heater and external PID controller
Total power		86 mW	153 mW	N/A	95 mW	12 mW	1.25 W (w/o heater)

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