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A 3.5 mV Input Single-Inductor Self-Starting Boost Converter with Loss-Aware MPPT for Efficient Autonomous Body-Heat Energy Harvesting

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Abstract

A single-inductor self-starting boost converter is presented suitable for thermoelectric energy harvesting from human body heat. In order to extract maximum energy from a thermoelectric generator (TEG) at small temperature gradients, a loss-aware maximum power point tracking (MPPT) scheme was developed that enables the harvester to achieve high end-to-end efficiency at low input voltages. The boost converter is implemented in a 0.18 μm CMOS technology and is more than 75% efficient for a matched input voltage range of 15 mV–100 mV, with a peak efficiency of 82%. Enhanced power extraction enables the converter to sustain operation at an input voltage as low as 3.5 mV. In addition, the boost converter self-starts with a minimum TEG voltage of 50 mV leveraging a dual-path architecture without using additional off-chip components.

Keywords

DC-DC boost converter; thermoelectric generator; body heat; energy harvesting; cold-start; battery-less

I. INTRODUCTION

ENERGY harvesting can be used to power wireless sensor nodes for realizing fully autonomous networks [1], or for powering miniaturized, self-sustaining wearable devices for preventive healthcare and continuous vital sign monitoring [2]. Microwatt-scale power

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extracted from human body heat using thermoelectric generators (TEG) can provide such power autonomy efficiently, and this approach excels in indoor environments where other energy sources, such as solar energy, are less abundant. However, the small temperature gradient (ΔT) of a few degrees between the skin surface and the ambient environment generates only a few tens of millivolts of open-circuit voltage from a centimeter scale TEG; impedance matching for maximum power transfer further reduces the input voltage to the DC-DC boost converter. This makes efficient power conversion especially challenging, and for fully autonomous applications, the converter must also self-start at this low input voltage.

In recent years, a variety of DC-DC boost converter architectures have been reported to address the challenges posed by low input voltage. One such boost converter designed for thermoelectric energy harvesting can operate with an input voltage as low as 20 mV [3]. However, this architecture lacks maximum power point tracking (MPPT), reducing the total extracted output power of the harvester despite high converter efficiency; the design also requires an additional source of energy for initial start-up of the converter. Boost converter architectures sustaining operation with an input voltage as low as 10 mV have also been demonstrated [4], [5], but these approaches also fail to self-start at low input voltage, making them unsuitable for fully battery-less energy harvesting.

For low-voltage self-start, off-chip transformers have been exploited to start a boost converter at tens of millivolts from a TEG [6], [7]; however, the implementation in [6] for high resistance TEGs is not capable of generating microwatts of power from low temperature differential (e.g. body-heat), whereas transformer reuse in [7] restricts the efficiency of the converter to 61%. High peak efficiency and low-voltage cold-start of the boost converter is demonstrated in both [8] and [9], but these require multiple inductors, increasing the form-factor and off-chip component count for the harvester. Cold-start of the boost converter at 70 mV in [10] and at 57 mV in [11] are achieved by means of integrated self-start techniques, but overall converter efficiency is comparatively low. Hence, it is evident that high efficiency and self-start of the converter at low voltages are fundamentally difficult problems to address using a single architecture and requires further investigation.

In this work, we present a single-inductor boost converter architecture that is capable of harvesting energy efficiently and can also self-start at low voltage from a thermoelectric generator [12]. A unique loss-aware maximum power point tracking (MPPT) scheme is proposed that reduces the total losses of the boost converter while ensuring maximum power transfer (MPT) from the source to the input, improving the end-to-end efficiency and output power of the harvester. The boost converter delivers power to the output with more than 75% efficiency at input voltages above 15 mV, and it achieves a peak efficiency of 82% with 50 mV input. Efficient low-voltage operation of the converter enables sustained operation at an input voltage as low as 3.5 mV. In addition, a dual path architecture is proposed which assists in self-starting the converter with an input voltage as low as 50 mV, without requiring additional off-chip components. The harvester generates a regulated output voltage of 1.2 V and operates over a TEG output voltage range of 7 mV–200 mV.

The rest of the paper is organized as follows: Section II describes the boost converter architecture and theoretical basis of loss-optimized maximum power transfer; Section III

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explains detailed circuit implementations and design methodology; performance of the fabricated chip is presented in Section IV; and, Section V provides a brief conclusion.

II. SELF-STARTING BOOST CONVERTER ARCHITECTURE

A TEG generates voltage, V_{TG}, proportional to the ΔT between human skin and environment with only a few ohms of source resistance, R_{TG}. A dual-path DC-DC converter architecture is implemented to boost the voltage as shown in Fig. 1 by utilizing a single off-chip inductor to achieve efficient power conversion as well as low-voltage self-start.

A. Low-voltage self-start and dual-path operation

A one-shot cold-start technique demonstrating fast and low-voltage cold-start of a boost converter is adopted for self-start [11]. During cold-start, as shown in Fig. 2a, a charge-pump-based on-chip voltage multiplier clocked by a low-voltage ring oscillator boosts the input voltage V_{IN}. The boosted output of the charge pump, V_{CP}, is used to generate a single start-up strobe pulse, V_{ST}. This pulse turns on the start-up low side switch, M_{ST}, for a small duration, which charges the inductor, L, with current from the TEG.

On the falling edge of V_{ST}, inductive overshoot at V_S turns on the PMOS diode, M_D, asynchronously and the inductor current charges the on-chip storage capacitor, C_{INT}. This intermediate storage capacitor is chosen small enough (200 pF) so that energy accumulated during the strobe cycle can charge it sufficiently to generate a voltage, V_{INT}, momentarily higher than 500 mV following the falling edge of V_{ST}. A secondary oscillator (OSC) powered by V_{INT} starts operation and generates a switching clock, CK, to continue operation of the inductive boost converter. Now the inductor is energized with more current every CK cycle using a wider low-side switch, M_{LS}, as shown in Fig. 2b, and energy is transferred to C_{INT}; this is an asynchronous mode of operation. A voltage regulation block is also activated in this phase to track V_{INT}.

A power-on-reset (POR1) circuit senses the rise of V_{INT} and turns on switch S_1 as soon as V_{INT} crosses 1V. As shown in Fig. 2c, this activates a secondary path of inductor energy transfer, which operates synchronously using a high-side PMOS switch, M_{HS}, and powers the final output, V_{OUT}. The n-well of M_{HS} (and of M_D) is always biased to the highest potential using dynamic body biasing (DBB) to avoid inefficient body-current (Fig. 1). S_1, implemented using a PMOS transistor, is held off in the previous phases utilizing the charge pump output, V_{CP}, and restricts the start-up energy of the inductor from flowing to the synchronous path on the falling edge of V_{ST}. This helps in kick-starting the asynchronous path with a relatively small amount of energy and accelerates the overall start-up process. With low available TEG power, discontinuous conduction mode (DCM) operation is used for synchronous boost conversion [13], implemented by a zero current sensing (ZCS) block to adjust the on-time, t_{HS}, of M_{HS}.

During this handover phase, illustrated in Fig. 2c, the high-efficiency synchronous path charges the output capacitor, C_{OUT} (1uF), while the asynchronous path provides power to the control circuits. The dual paths are operated in a time-multiplexed manner by means of a dead-time, Δt, between t_{LS} and t_{HS}. Output, EN, of the voltage regulation block, which

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monitors V_{INT}, enables Δt to force M_D to turn on briefly; the inductor current is rerouted to the asynchronous path during this dead time and recharges C_{INT}. With the falling edge of CK_{HS}, as M_{HS} is turned on, the inductor current reverts back to the synchronous path to charge C_{OUT}.

Finally, as V_{OUT} crosses 0.7V, detected by POR2, the PMOS power switch S_2 is turned on, shorting V_{OUT} and V_{INT}; Δt is deactivated with the help of a multiplexer. As illustrated in Fig. 2d, the boost converter now operates in an exclusively synchronous mode to provide both control power and output power. The rising V_{OUT} disables the start-up clock and turns off the start-up voltage multiplier, avoiding unnecessary power consumption during normal operation of the boost converter. As $POR2$ goes low, the EN signal from the same voltage regulation block is now utilized to enable/disable the switching clock and regulate V_{OUT} by means of an on-off hysteretic control scheme.

The proposed dual-path architecture utilizes the asynchronous path to speed up the start-up process, leveraging the one-shot cold-start mechanism, and ultimately starts a high-efficiency synchronous boost converter at low input voltage without requiring an additional off-chip inductor.

B. Boost converter losses and maximum power transfer

Efficiency of the boost converter and maximum power transfer at the input determine the final output power available to the load.

1) Losses in a DC-DC boost converter: The voltage conversion gain, K, of a boost converter operating in DCM mode is given as

$$K = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{t_{LS}}{t_{HS}}\right), \tag{1}$$

where t_{LS} and t_{HS} are the on-times of M_{LS} and M_{HS} respectively as shown in Fig. 3a. For applications with low V_{IN}, required K being large, $t_{LS} \gg t_{HS}$, and the input power, P_{IN}, flowing into the converter can be calculated as

$$P_{IN} = \frac{1}{T} \cdot \frac{1}{2} \cdot V_{IN} I_P (t_{LS} + t_{HS}) \approx \frac{1}{2} \cdot \frac{V_{IN}^2 t_{LS}^2}{LT} \tag{2}$$

where T is the time period of the switching clock and $I_P = V_{IN} t_{LS}/L$ (when $t_{LS} \ll$ inductor charging time constant) is the peak inductor current. On the other hand, conduction power losses, P_C, due to the on-resistance of M_{LS} and M_{HS} can be derived as

$$\begin{aligned} P_C &= P_{C,LS} + P_{C,HS} \\ &= \frac{1}{3} \cdot \frac{I_P^2}{T} \cdot (R_{LS} t_{LS} + R_{HS} t_{HS}). \end{aligned} \tag{3}$$

By expressing t_{HS} and I_P in (3) in terms of t_{LS},

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$$P_{\mathrm{C}} = \frac{1}{3} \cdot \frac{V_{IN}{}^2 t_{LS}{}^3 R_{\mathrm{C}}}{L^2 T} \tag{4}$$

where $R_{\mathrm{C}}=(R_{\mathrm{LS}} + R_{\mathrm{HS}}/K)$ represents the total conduction resistance contributed by LS and HS switches. For high values of K, conduction loss contributed by the LS path dominates.

Power consumed by the control circuits is mostly the switching power required for the drivers to drive the large LS and HS switches. If the total lumped switch gate capacitance of the control circuit is C_{SW}, the switching power is given as

$$P_{\mathrm{SW}} = C_{\mathrm{S}} V_{\mathrm{OUT}}^2 \cdot f_{\mathrm{S}} = C_{\mathrm{S}} K^2 V_{IN}^2 \cdot f_{\mathrm{S}} \tag{5}$$

where $f_{\mathrm{S}} = 1/T$ is the switching frequency.

Additional power losses due to timing imperfections, leakage currents, and parasitic loading are small and can be neglected. Hence, the total power loss of the converter can be approximated as

$$P_{\mathrm{LOSS}} = P_{\mathrm{C}} + P_{\mathrm{SW}} = \frac{1}{3} \cdot \frac{V_{IN}^2 t_{\mathrm{LS}}{}^3 R_{\mathrm{C}}}{L^2 T} + C_{\mathrm{S}} K^2 V_{IN}^2 \cdot f_{\mathrm{S}}\,. \tag{6}$$

The loss of the converter when normalized with input power (2) and expressed in terms of duty-cycle, $D = t_{\mathrm{LS}}/T$, as

$$\frac{P_{\mathrm{LOSS}}}{P_{\mathrm{IN}}} = \frac{2 D R_{\mathrm{C}}}{3L} \cdot \frac{1}{f_{\mathrm{S}}} + \frac{2 C_{\mathrm{S}} K^2 L}{D^2} \cdot f_{\mathrm{S}}^2, \tag{7}$$

exhibits concave behavior with respect to f_{S}, as plotted in Fig. 3b, where conduction loss dominates at lower f_{S} and switching loss dominates at higher f_{S}. With other parameters fixed, an optimal f_{S} minimizes $P_{\mathrm{LOSS}}/P_{\mathrm{IN}}$ and thereby maximizes the efficiency of the DC-DC converter, η_{DCDC}, as

$$\eta_{\mathrm{DCDC}} = \frac{P_{\mathrm{IN}} - P_{\mathrm{LOSS}}}{P_{\mathrm{IN}}} = 1 - \frac{P_{\mathrm{LOSS}}}{P_{\mathrm{IN}}} \tag{8}$$

2) Maximum power transfer at input: The internal resistance, R_{TG}, of the TEG limits the amount of power that can be extracted from the generator. For maximum power transfer, the input resistance, R_{IN}, of the boost converter must be matched with R_{TG}. The extent of matching can be expressed as the efficiency of maximum power point tracking, η_{MPPT}, defined as the proportion of the theoretical maximum power ($V_{\mathrm{TG}}{}^2/4R_{\mathrm{TG}}$) entering the converter. As a TEG operates as a linear source for small values of ΔT [14], R_{TG} can be assumed constant for body-heat energy harvesting applications, and one-time tuning of the power converter to set $R_{\mathrm{IN}} = R_{\mathrm{TG}}$ is sufficient to ensure MPPT; this saves additional control power compared to continuous MPPT approaches [15].

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The input resistance of a DC-DC boost converter operating in discontinuous conduction mode can be derived by calculating the average input current [16], [17], and can be expressed in terms of duty-cycle, D, as $R_{IN} \approx (2Lf_S)/D^2$. Hence, for a fixed value of L and D, input matching can be achieved by tuning the f_S of the switching clock, as shown in Fig. 3c.

C. Loss-optimized maximum power point tracking

Although a fixed f_S of the switching clock with $D = 0.5$ can assure maximum power transfer at the input, it may not be the optimal frequency for the normalized loss and can result in a low conversion efficiency, η_{DCDC}. Similarly, the optimal value of f_S required to maximize η_{DCDC}, obtained from (7) at $D = 0.5$, can cause an input impedance mismatch and thereby reduce η_{MPPT}. The end-to-end efficiency of the harvester, η_{HARV}, is determined by the final output power as a proportion of the available input power and can be expressed as

$$\eta_{HARV} = \eta_{MPPT} \times \eta_{DCDC}. \tag{9}$$

As such, input matching using f_S-only tuning may not improve the overall output power of the harvester; the efficiency of the converter must be enhanced while assuring MPPT at the input. To mitigate this trade off, a loss-aware MPPT architecture was developed, where η_{DCDC} is improved by reducing converter losses while keeping the input matched by tuning both D and f_S; this enhances the η_{HARV} across the input voltage range and enables operation with V_{IN} as low as a few millivolts.

At perfect input matching, $R_{TG} = R_{IN}$, normalized loss can be re-formulated using (7) as

$$\frac{P_{LOSS}}{P_{IN}} = \left(\frac{4R_C}{3R_{TG}}\right) \cdot \frac{1}{D} + \left(C_S K^2 R_{TG}\right) \cdot f_S \tag{10}$$

Centimeter-scale TEGs have an internal resistance of a few ohms [14]. For moderately low TEG voltage (e.g. 50–200 mV) and corresponding conversion gain K, low duty-cycle results in higher conduction loss, as evident from (10). This is mainly due to an effective increase of conduction time, t_{LS}, at a lower value of f_S required for input matching. An increase in D, accompanied by a proportional increase in f_S to maintain the R_{IN} value for input matching, can effectively reduce the conduction time as illustrated in Fig. 4a, where the value of D is changed from 0.5 (red line) to 0.9 (blue line). The increase in f_S does not significantly affect the switching loss, as evident in Fig. 4b, due to the moderate value of K.

However, as the input voltage goes further lower, the required value of K becomes higher, and the same pair of (D, f_S) may no longer provide low loss, which impacts the overall converter efficiency. For TEG voltages below 40 mV, the input power is low enough that the switching power is comparable to the input power, and converter losses are dominated by the switching loss; this is also evident from (10). Lower f_S and D, as shown in Fig. 5a, are beneficial in this case to reduce the dominant switching loss without impacting the input MPPT. The resulting longer conduction time minimally affects losses due to small I_L at low

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V_{IN}. As shown in Fig. 5b, decreasing the duty-cycle from 0.9 to 0.5 can minimize the converter losses and improves η_{DCDC} without impacting η_{MPPT}.

Hence, η_{HARV} can be improved across a wide-range of TEG voltages by varying the duty-cycle and frequency of the converter clock. While continuous loss-optimization could be achieved in theory, in this work we have implemented a loss-aware MPPT scheme using an adaptive clock whose duty-cycle and frequency are switched between discrete pairs of (D,f_S) for input matching based on the dominant losses of the converter at moderate and very-low TEG voltages applicable for body-heat energy harvesting applications.

III. CIRCUIT IMPLEMENTATIONS

A low-voltage, self-starting boost converter requires startup circuits that function at voltages well below the threshold of transistor with minimal conduction, along with reduced leakage control circuits to make the converter efficient.

A. Ultra-low-voltage integrated cold-start

A voltage multiplier is needed to step up the small input voltage and power the control circuits of the inductive converter during start-up [8], [10], [18]. On-chip voltage multiplication using charge pumps at small input supply is challenging due to the ultra-sub-threshold conduction of the switches. A high-gate boosting technique demonstrated in [11] improves the gate overdrive of the switches to enhance conduction at small supply; however, this approach requires multiple charge pumps, which consumes more area. In this work, a single charge pump is used to achieve similarly boosted overdrive for the charge transfer switches (CTS) during the conduction phases of the charge pump stages.

A dual gate-boosting architecture is shown in Fig. 6a, where the initial stages of the charge pump use deep-*n*-well NMOS switches and the later stages use PMOS switches for charge transfer. The charge pump is a dual-phased Dickson architecture [19] with 15 stages in total. Higher voltages from later stages are fed back to improve gate overdrive of the NMOS switches of earlier stages; at the same time, lower voltages from earlier stages are utilized to improve the gate overdrive of PMOS switches of later stages. The dual gate boosting action using internal nodes eliminates the need for additional charge pump stages.

The gate-boosting action of the switches is done symmetrically, where the output nodes of stages 1 & 9, stages 2 & 10, and so forth, are used to generate gate drive for the respective CTSs. As shown in Fig. 6b, dual-phased voltages, $P2$ and $P2B$ at the output of stage 2 and $P10$ and $P10B$ at the output of stage 10 are used to generate gate clocks $G2-G2B$ and $G9-G9B$, respectively, using dynamic inverters $D1-D4$. The gate clocks for the second stage, $G1$ and $G1B$, are reused in the first stage with appropriate phasing to avoid additional charge pump stages. The final stage of the charge pump uses a diode-connected deep-*n*-well NMOS to avoid reverse charge flow during a voltage droop at the output. The boosted gate clocks are non-overlapping with the pumping clock phases, CK and CKB, to avoid reverse charge flow between consecutive stages during non-charge-transfer phases. Non-overlapping phases of the internal dual-phased voltages, $PX-PXB$ and $NX-NXB$, are generated using non-overlapping clocks and level shifters (NOV-LS).

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A stacked-inverter based ring-oscillator [20] is used to generate an on-chip start-up clock at small input voltages. The stage capacitance is 22 pF to achieve low enough slow switching limit (SSL) output impedance, $N/(Cf_S)$ [21], with the minimum sized CTSs to minimize loading of the weakly driven gate clocks. It is important to note that although a high gate-boosting action takes place as the internal voltages gradually increases towards the steady-state value, initial voltage boosting is slow and depends only on the leakage current of the switches. However, usage of PMOS switches for the later stages allows boosting of the later stages quickly, which then boosts the NMOS switches; the circular action results in rapid dual gate boosting and fast build-up of the output voltage, V_{CP}.

The boosted voltage, V_{CP}, is used to power a one-shot generator. The basic building block of the one-shot generator as implemented in [11] comprises a two-transistor reference generator, leakage-based comparator, and a thyristor-based delay element. It generates an output pulse with a sharp falling edge to create inductive overshoot at V_S, which kick starts the asynchronous path by forward biasing the PMOS diode M_D.

B. Zero current sensing for high-efficiency boost conversion

The synchronous boost converter is operated in DCM mode, favorable for low power operation [13], where the inductor is disconnected from the output once I_L reaches zero value to avoid reverse energy flow. A digital zero current sensing (ZCS) scheme is adopted to save power. Instead of using a comparator [22], a flip-flop-based sensing mechanism [3] is used. The ZCS circuit block, shown in Fig. 7a, employs a flip-flop to sample the voltage, V_S, at the rising edge of $CK_{HS,DEL}$, a delayed version of CK_{HS}, and to track the zero point of I_L. It generates a high or low output signal corresponding to an overshoot or undershoot of V_S, respectively, depending upon the status of I_L around the zero-crossing point. The delay between CK_{HS} and $CK_{HS,DEL}$ plays a critical role in sensing the transition of V_S and is chosen as 24 ns to make sure that there is sufficient time for the voltage to transition following the closure of the high-side PMOS switch on the rising edge of CK_{HS}. As illustrated in Fig. 7b, a rising edge of $CK_{HS,DEL}$ will sense a high V_S at the flip-flop input when the inductor energy is not yet fully transferred to the output and I_L is still approaching the zero value; the resulting output, $(INC/\overline{DEC})$, increments a counter to create a longer delay between the falling edges of CK_{LS} and $CK_{LS,DEL}$ using a programmable delay block. This generates a wider low phase of CK_{HS} in the next cycle to improve the inductor energy transfer with a longer on-time of the HS switch. Conversely, a low in the $INC/\overline{DEC}$ signal indicates that inductor energy is fully transferred to the output and reverse current has started to flow from the output capacitor toward the input; this directs the counter to decrement, reducing the on-time of the HS switch in the following cycle. At steady state, the counter value toggles between two adjacent values in consecutive clock cycles. In order to accommodate a wide range of input voltages, a 7-bit counter is used to generate the required t_{HS} with the programmable delay block, comprising unit delay elements, each capable of delaying the input pulse by 24 ns. Conventional delay blocks using capacitive elements incur high switching power consumption and also result in high crow-bar current due to slow transitions. To avoid this, a low power unit delay element, as shown in Fig. 7a, was designed for the programmable delay block, where a resistive discharge path is used to create a delay in the falling edge of the input pulse only. The pull-up and pull-down paths of intermediate

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inverters are controlled to reduce the crow-bar current during the delay time. Also, individual delay elements are enabled only when needed, saving power at low input voltages.

C. Variable clock generation for loss-aware MPPT

The proposed loss-aware MPPT requires selection of duty-cycle, D, and frequency, f_S, of the switching clock based on the input voltage to minimize overall losses of the converter while matching its input impedance to the source.

As implemented, the system supports two (D,f_S) pairs, and a threshold input voltage for selecting between them must be chosen based on dominant losses in each regime. To determine the dominant loss mechanisms across the input voltage range, the overall converter losses for a fixed inductor value are normalized to the input power from a portable TEG [14] and analyzed using transistor-level simulation of the complete energy harvester by varying the frequency of the switching clock with a duty-cycle of $D = 0.5$. A 100 μH shielded power inductor [23] is chosen for the converter based on the required start-up energy to be stored in the inductor during the strobe-cycle for one-shot cold-start operation [11]. With a TEG source resistance of approximately 5Ω and an inductor DC resistance of 110 mΩ, it is observed that switching losses dominate overall converter losses for TEG voltages below 40 mV. For higher source voltage, conduction losses start to dominate over the switching losses as the input power increases. From this assessment we have chosen a matched V_{IN} of 20 mV (V_{TEG} = 40 mV) as the threshold value; below this value, the alternate (D,f_S) pair is used for the switching clock. In order to avoid rapid toggling of (D,f_S) near the threshold, a hysteretic guard-band is used, where V_{IN} of 25 mV is chosen as the upper voltage threshold for changing (D,f_S).

For determination of D and f_S values needed to maximize end-to-end efficiency of the harvester across the input voltage range, normalized losses of the converter were analyzed by varying the duty-cycle of the switching clock parametrically with frequency. Based on that analysis, a duty-cycle of $D = 0.55$ and a frequency f_S = 8.33 kHz were chosen for the switching clock at input voltage below 20 mV to match the input impedance with minimized losses of the converter. For higher input voltage, as the input power increases, a higher duty-cycle is needed, with the corresponding higher frequency required for MPPT. However, for higher values of V_{IN}, the voltage conversion ratio, K, reduces, as does the ratio t_{LS}/t_{HS}. This limits the maximum allowable D that ensures DCM operation such that $t_{LS} + t_{HS} \leq 1/f_S$. As such, a duty-cycle of $D = 0.91$ and frequency of f_S = 25 kHz were selected for use at higher input voltages. Although this selection changes the input impedance value marginally compared to that with the chosen (D,f_S) pair for $V_{IN} < 20$ mV, the impact of this input impedance mismatch on the harvester output power is neglible for the higher input voltage range.

Direct, continuous sensing of V_{IN} requires additional power consumption and further increases losses. As an alternative, t_{HS} can be used as a proxy indicator, as it is directly proportional to V_{IN} as long as V_{OUT} and t_{LS} are fixed (1). As shown in Fig. 7a, the counter code in the ZCS circuit, $X0-X6$, sets the required t_{HS} for each V_{IN} and hence can be re-used to achieve comprehensive V_{IN} tracking obviating the need for additional circuitry. The ZCS

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code is utilized to select the appropriate (D,f_S) pair for the switching clock, CK, using a low-power digital circuit, shown in Fig. 8a.

A digital look up table, as shown in Fig. 8a, comprises a series of flip-flops and combinational logic to generate clocks with different combinations of duty-cycle and frequency. As shown, 16 flip-flop stages form a frequency divider and can generate frequencies between $f_0/16$ to $f_0/2$, where f_0 denotes the base clock frequency. Consecutive positive and negative edge-triggered flip-flops are used to create a wide range of duty-cycle by tapping the intermediate outputs and combining them with OR gates. A duty-cycle of $0.5\pm n/2K_f$ is generated for even values of n, and $0.5\pm(n-1+2D_0)/2K_f$ for odd values of n, where D_0 denotes the base clock duty-cycle, K_f denotes the frequency division factor, and n can be any code between zero and (K_f-1). A base clock with f_0 of 100 kHz and $D_0 = 0.67$ is generated using a low-power oscillator architecture [24], primarily designed to initiate and operate the asynchronous converter (OSC in Fig. 1).

From the wide range of available values of (D,f_S), the required pair variants are generated by selecting the corresponding code stored in a programmable register. Additionally, tunability of D_0 and f_0 of the base clock using separate control bits provides further flexibility for fine-tuning CK to calibrate out any static variation of R_{TG} for different TEG parts.

Fig. 8b illustrates selection of the (D,f_S) pair with transient variation of V_{IN} near the threshold. For $V_{IN} > 20$ mV, the charging time of the inductor, t_{LS}, is equal to 36.67 μs. As V_{IN} decreases to 20 mV, the ZCS code required to generate the corresponding t_{HS} becomes 20, as illustrated in Fig. 8b. A decoder detects this and selects the lower (D,f_S) pair using the digital look up table. At this point, t_{LS} is 66.67 μs and the ZCS code threshold required to generate the t_{HS} for V_{IN}=25 mV with the same delay elements becomes 46. Now the (D,f_S) pair reverts to the higher values. As t_{LS} reverts to 36.67 μs, the ZCS code would gradually converge to 25 to generate the t_{HS} required for $V_{IN} = 25$ mV; the ZCS code being still higher than 20 (lower threshold), the (D,f_S) setting of the clock would not change. This hysteresis avoids unnecessary toggling of the (D,f_S) around a single threshold without adding complexity to the the ZCS circuit. The hysteresis is implemented with a simple RS latch to set or reset the value of (D,f_S) based on the decoder output.

While implemented here using two pairs, in future work the number of discrete (D,f_S) pairs and associated input voltage regions could be increased to further enhance efficiency across a wide input voltage range.

D. Dual-path operation and output voltage regulation

The dual-path operation of the boost converter during startup is made possible with the help of a voltage regulation block activated immediately following the one-shot cold start. As shown in Fig. 9a, a switched capacitor voltage divider divides the intermediate boosted voltage, V_{INT}, to $V_{INT}/2$, which is compared against two reference voltages, $V_{REF,LO}$ and $V_{REF,HI}$, generated using ultra-low-power on-chip reference generators [25]. During start-up, this information is used to control (on/off) the dead-time, Δt, between CK_{LS} and CK_{HS}. This Δt forces the inductor current to flow through the diode M_D for a short time to recharge V_{INT}, as illustrated in Fig. 9b, before the current is steered back to V_{OUT}; this continues

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until V_{OUT} crosses 0.7V and is shorted to V_{INT} with a low *POR*2 signal. During fully synchronous operation, the same control loop regulates V_{OUT} by enabling or disabling the switching clock, resulting in an energy-efficient hysteretic mode of voltage regulation.

IV. MEASUREMENTS

The energy harvester was implemented in a 0.18 μm CMOS process. A die micrograph is shown in Fig. 10; the converter circuits occupy an active area of 1.02mm^2.

Electrical performance of the chip was characterized using a bench-top power supply with an added series resistance of 5Ω, equivalent to the R_{TG} of a centimeter-scale TEG. Measured start-up transients, shown in Fig. 11a, demonstrate self-start of the boost converter with a minimum TEG voltage (V_{TG}) of 50 mV. At this input voltage, it takes 252 ms from cold start for V_{OUT} to reach 1.2V with an off-chip output capacitor of 1 μF. With higher V_{TG}, the output power of the start-up charge pump increases, and the start-up time decreases as shown in Table I.

A magnified region of the transient waveforms in Fig. 11b shows the parallel operation of the asynchronous and synchronous paths of the boost converter during start-up. The falling edge of the strobe triggers the asynchronous path, which feeds power to the control circuits for the synchronous path. As V_{INT} crosses 1V, the synchronous path is enabled and the inductor energy is fully shared by the two paths. Once V_{INT} crosses $V_{REF,HI}$ it is regulated by the dead-time-based enable/disable control until V_{OUT} is shorted with it and the converter enters into high-efficiency, fully-synchronous conversion mode. The MPPT is enabled only after this point, and the hysteretic on-off voltage regulation regulates V_{OUT} at 1.2V.

A measured transient plot in Fig. 12 demonstrates the operation of the proposed MPPT scheme using adaptive duty-cycle and frequency of the switching clock. As shown, transition of the TEG voltage from 15 mV to 50 mV results in a change of the (D, f_S) pair of the switching clock to optimize the efficiency of the converter. The switching clock with the new (D, f_S) pair still tracks the maximum power point at the input of the converter by matching R_{IN} with R_{TG}, evident by a measured $V_{IN} = V_{TG}/2$.

Load and line regulation of the boost converter output are shown in Fig. 13. V_{OUT} is regulated at 1.2V with a step in the load current, I_{LOAD}, from 1 μA to 60 μA and then to 10 μA, and also when V_{TG} is changed among 20 mV, 50 mV, and 80 mV. The output voltage ripple depends on the difference between the two on-chip reference voltages used for hysteretic on-off regulation, and the frequency of the ripple depends on the available power from V_{TG}, drawn I_{LOAD}, and the size of C_L.

The efficiency of the boost converter was measured using a source meter (Keithley 4120) as current load. The maximum available output power for different values of V_{TG} was measured by varying I_{LOAD} for each V_{TG} and ratioed with the input power to plot the variation of the efficiency of the boost converter with TEG voltages, as shown in Fig. 14. The converter achieves an efficiency (η_{DCDC}) of more than 75% for a V_{TG} above 30 mV (V_{IN} above 15 mV). The η_{DCDC} achieves a peak value of 82% with V_{TG} = 100 mV. The corresponding peak end-to-end efficiency of the harvester (η_{HARV}) is 80%.

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Once started, high η_{HARV} at low input voltage enables the converter to sustain operation at a V_{IN} as low as 3.5 mV as shown in Fig. 15, thanks to the loss-aware MPPT scheme. Below this V_{IN}, losses exceed available power and the converter stops operation. Utilization of the harvester power at a TEG voltage of 15 mV is shown in Fig. 16. The converter consumes a measured quiescent current of 470 nA at a V_{TG} of 50 mV, which scales down to 240 nA for a V_{TG} of 7 mV by means of the adaptive duty-cycle and frequency of the switching clock.

The performance of the implemented harvester is compared alongside state-of-the-art thermoelectric harvesters in Table II.

When tested with a commercial TEG (Marlow TG12–6-01L), the harvester self-starts with a ΔT of just 1.4°C and sustains operation until the ΔT between the skin surface and ambient environment falls below 0.2°C. The experimental setup is shown in Fig. 17. The minimum TEG voltage required to self-start the harvester is tested across 7 chips, and the measured value varies between 48 mV and 53 mV.

V. CONCLUSION

A single-inductor boost converter is demonstrated capable of achieving high efficiency at low input voltage from a TEG attached to human body. Enhanced efficiency of the converter while ensuring maximum power transfer at the input enables the complete harvester to achieve high end-to-end efficiency across the input voltage range by means of a loss-aware MPPT scheme by changing the duty-cycle and frequency of the switching clock. This not only helps to achieve peak efficiency at lower input voltage but also enables the harvester to sustain operation at a voltage as low as 7 mV from the TEG which corresponds to a ΔT of 0.2°C.

One-shot integrated cold-start along with a dual-path converter architecture achieves low voltage (50 mV) start-up and makes the harvester completely autonomous, removing the need for a battery at any stage of operation. These features together make the implemented TEG-based harvester ideal for powering energy-efficient wearables using human body heat.

Acknowledgments

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Biography

Soumya Bose (S’16) received the B.E. degree in electronics and telecommunication engineering from the Indian Institute of Engineering Science & Technology (IIEST), Shibpur, India, in 2009, the M.Tech. degree from Indian Institute of Technology (IIT),

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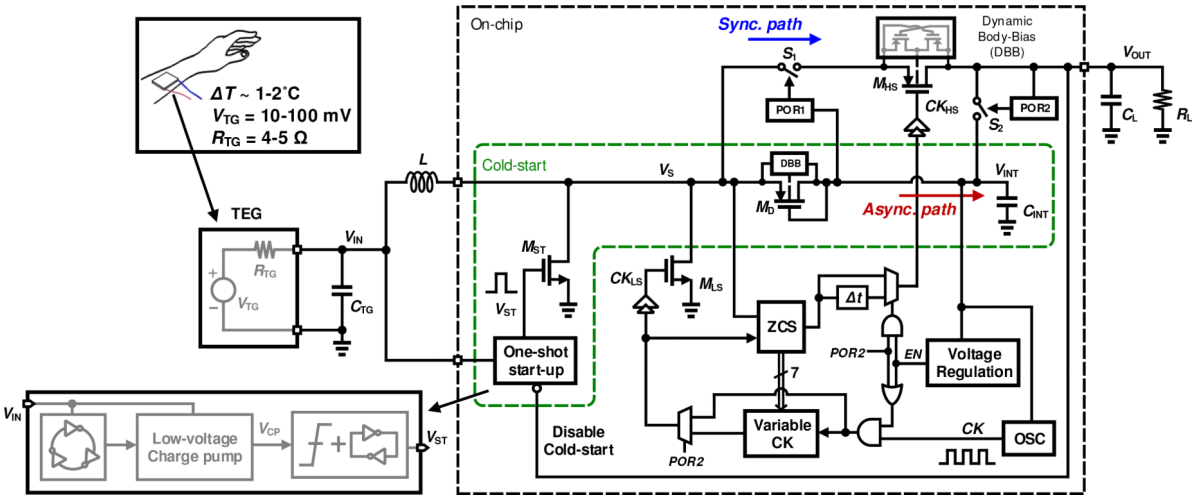

Fig. 1.

Self-starting single-inductor boost converter architecture for low-voltage thermoelectric energy harvesting utilizing human body heat.

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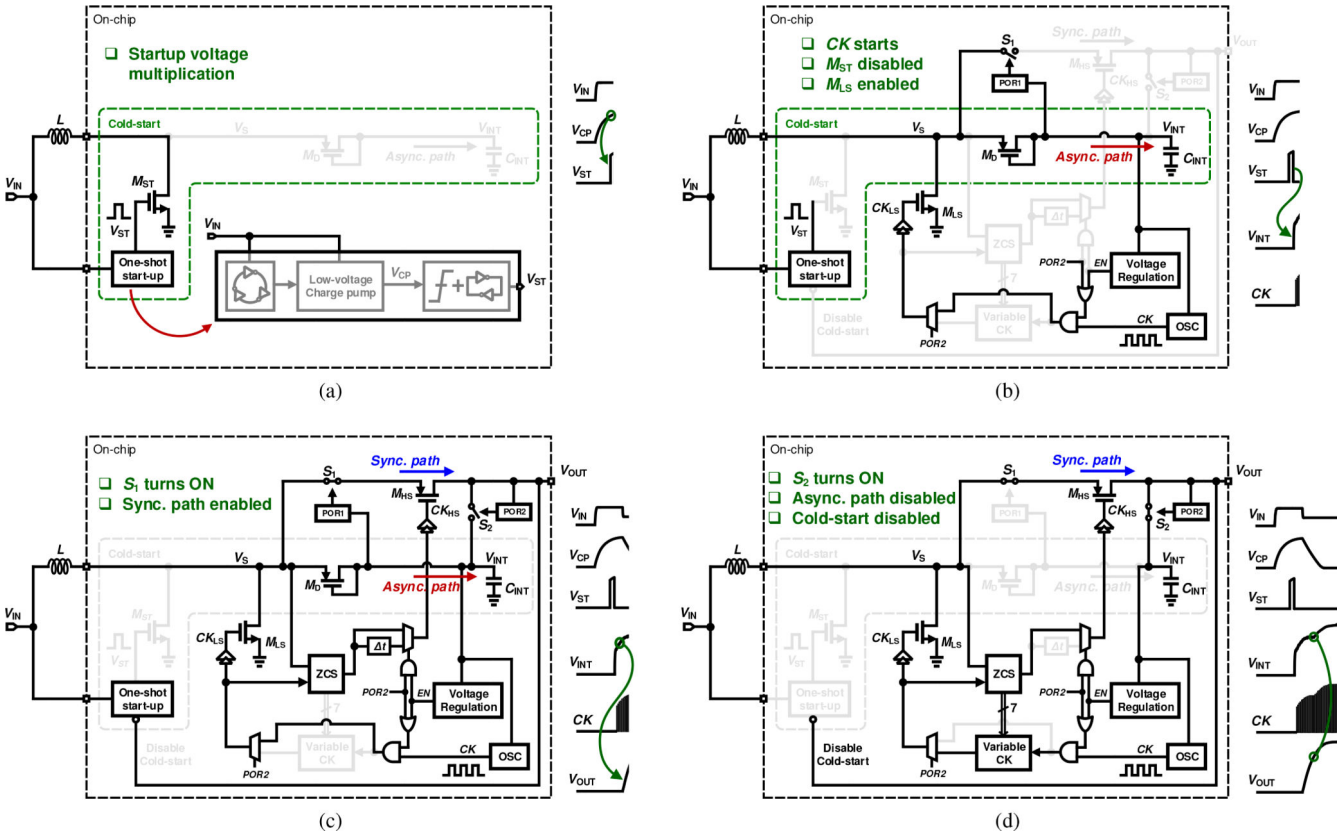

Fig. 2.

Illustrated phases of operation of the energy harvester architecture: (a) cold-start operation, (b) asynchronous operation, (c) dual asynchronous and synchronous operation (handover phase), and (d) fully synchronous operation (primary boost conversion).

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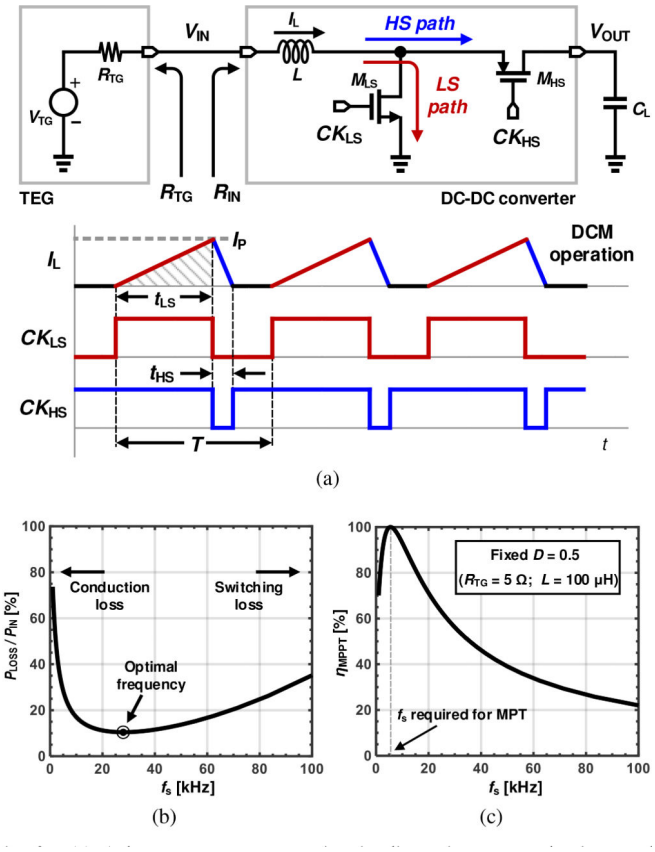

Fig. 3.

(a) A boost converter operating in discontinuous conduction mode (DCM), (b) power loss of the converter normalized with the input power across varying frequency, and (c) tuning converter switching frequency to achieve input resistance matching for maximum power transfer.

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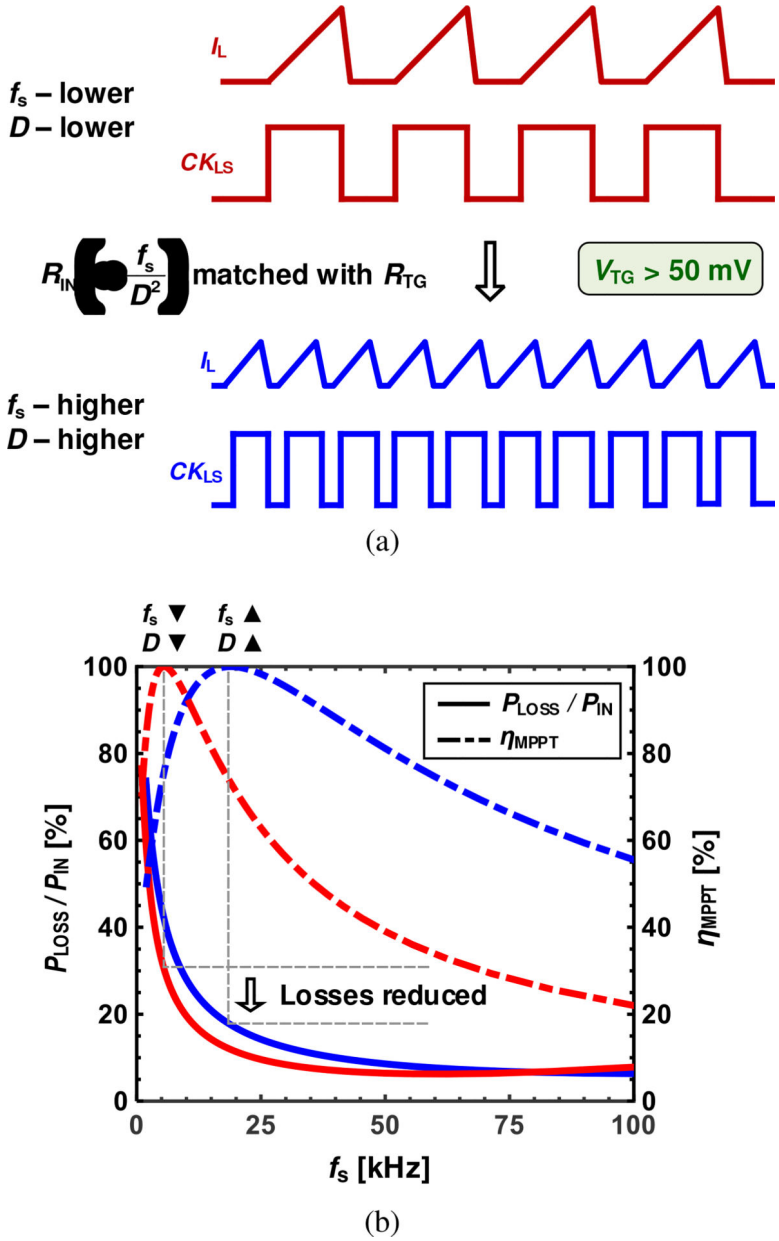

Fig. 4.

(a) Reduction in the charging time and peak current of the inductor resulting from an increase of f_S and D of the switching clock, without impacting input impedance matching. (b) Corresponding decrease in the overall losses of the converter for source voltages above 50 mV, normalized with the input power, due to smaller conduction losses.

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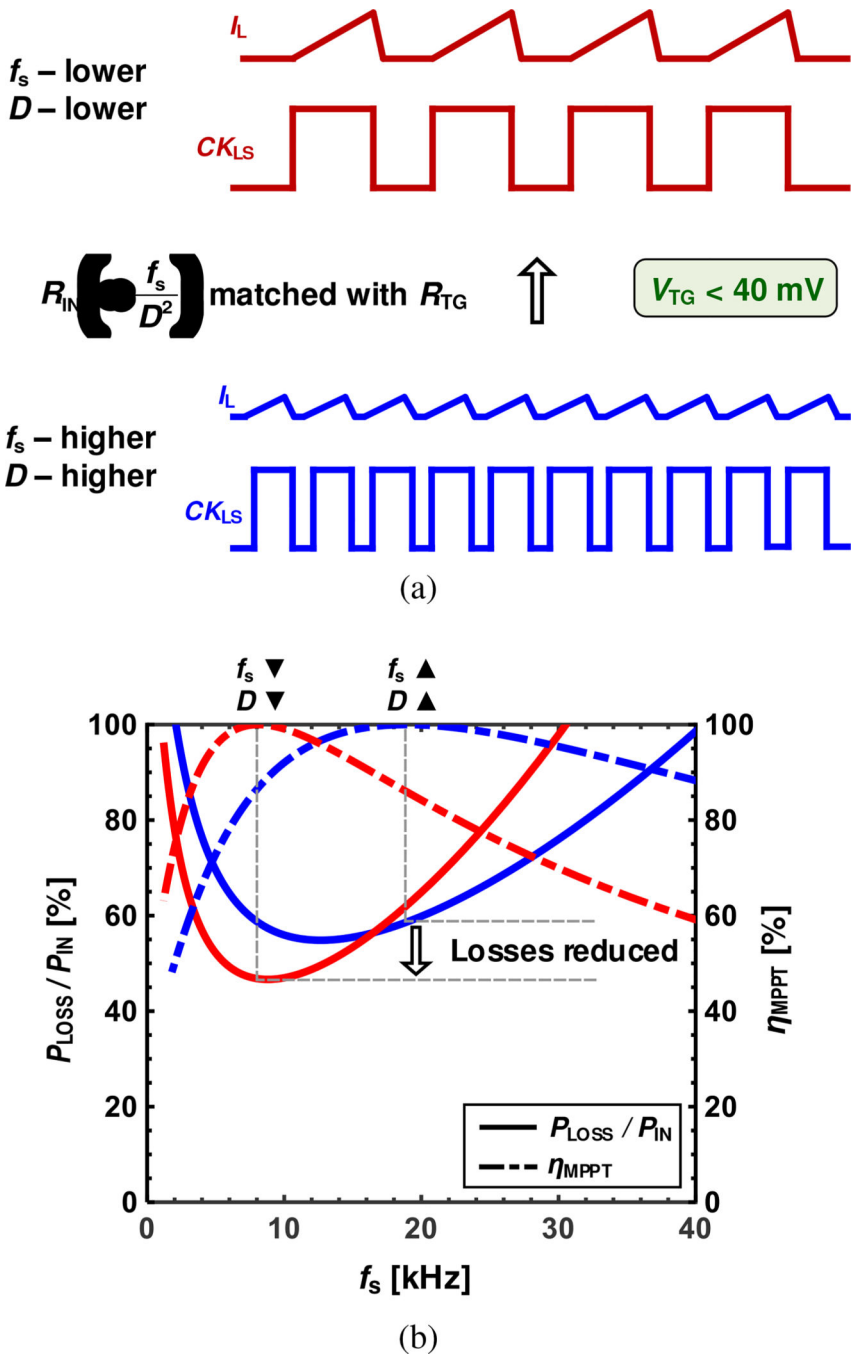

Fig. 5.

(a) Reduction of f_S at very low source voltage (<40 mV) reduces the dominant switching losses and is accompanied by a proportional decrease in D to ensure MPPT. (b) Corresponding improvement in the overall converter losses normalized with the input power.

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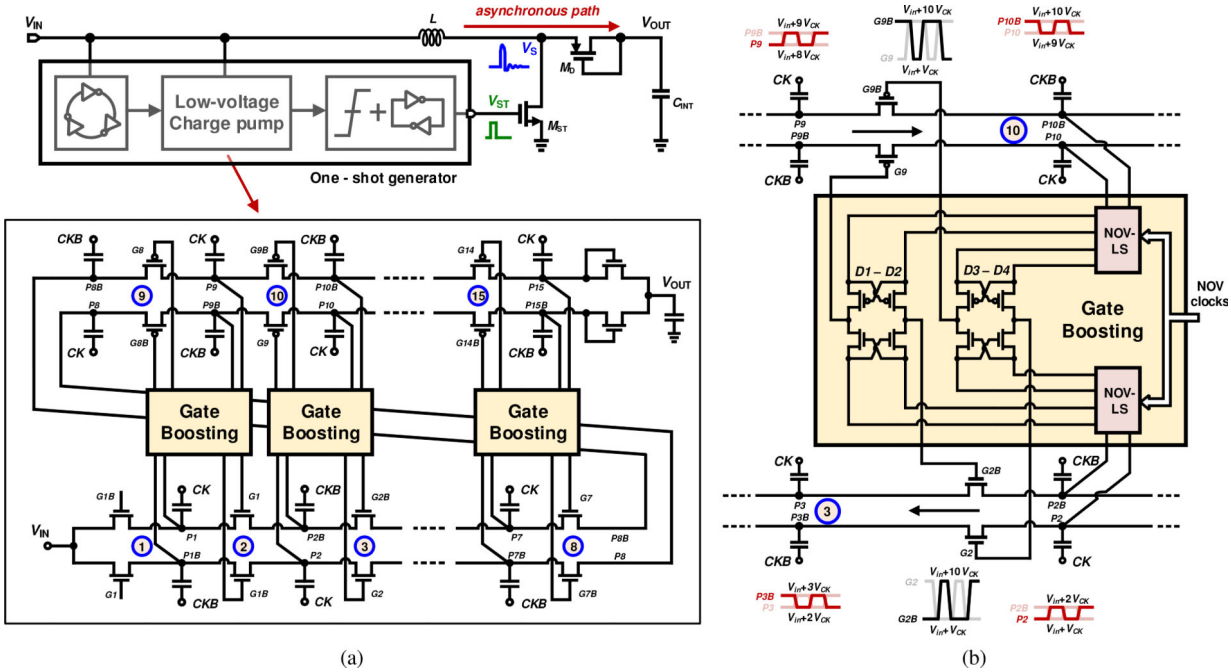
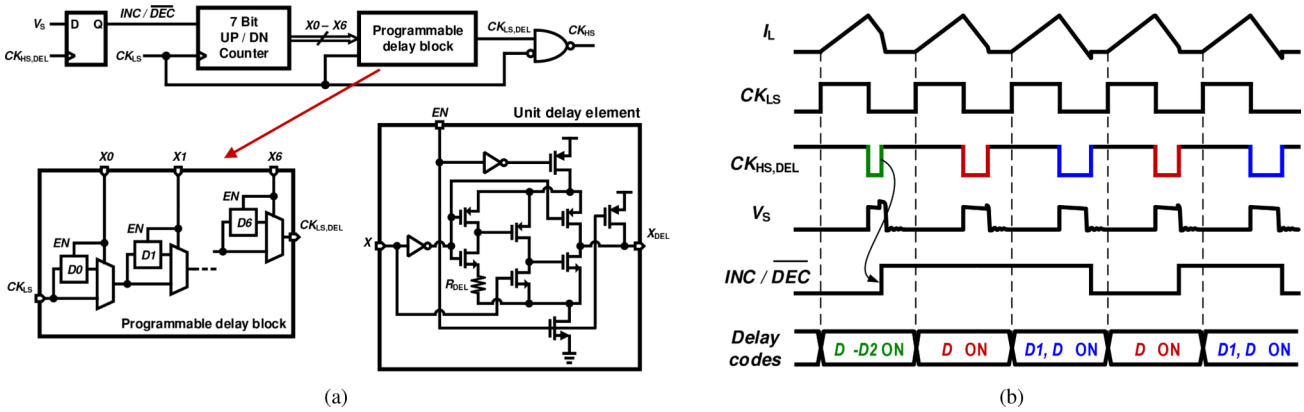


Fig. 6.

(a) One-shot start-up with on-chip voltage multiplier. (b) High dual gate-boosting using internal voltages and both NMOS and PMOS switches.



(a) (b)

Fig. 7.

(a) Implementation of zero current sensing (ZCS) using digital sensing and (b) timing diagram showing operation of ZCS.

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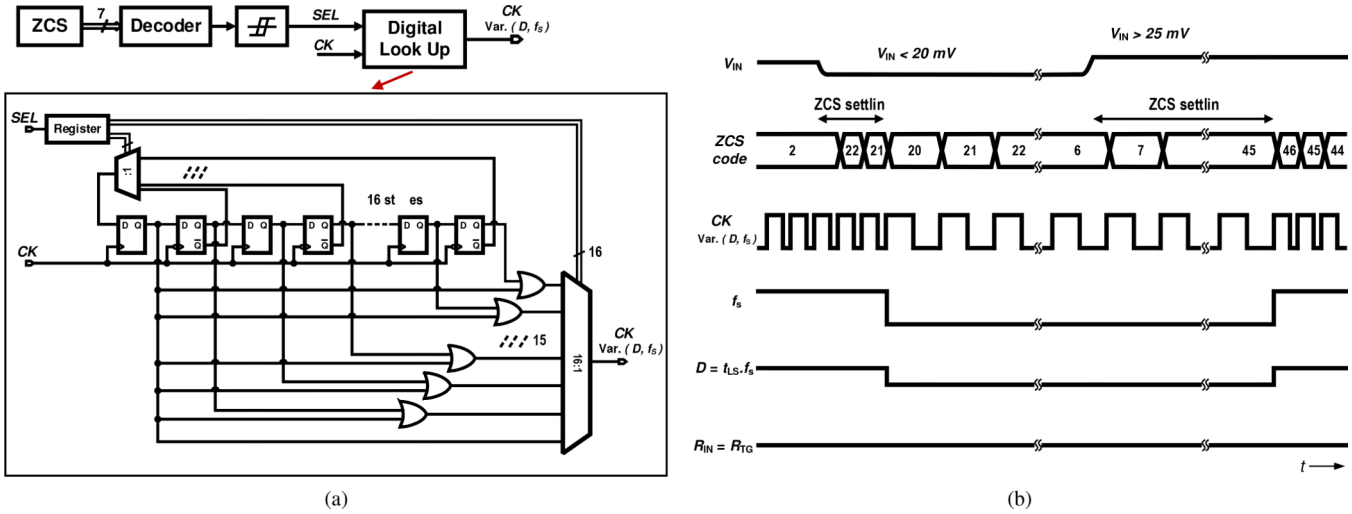

Fig. 8.

(a) Implementation of loss-aware MPPT using digital circuits. (b) Timing diagram showing adaptive duty-cycle and frequency of the switching clock for optimizing loss of the converter while ensuring maximum input power transfer.

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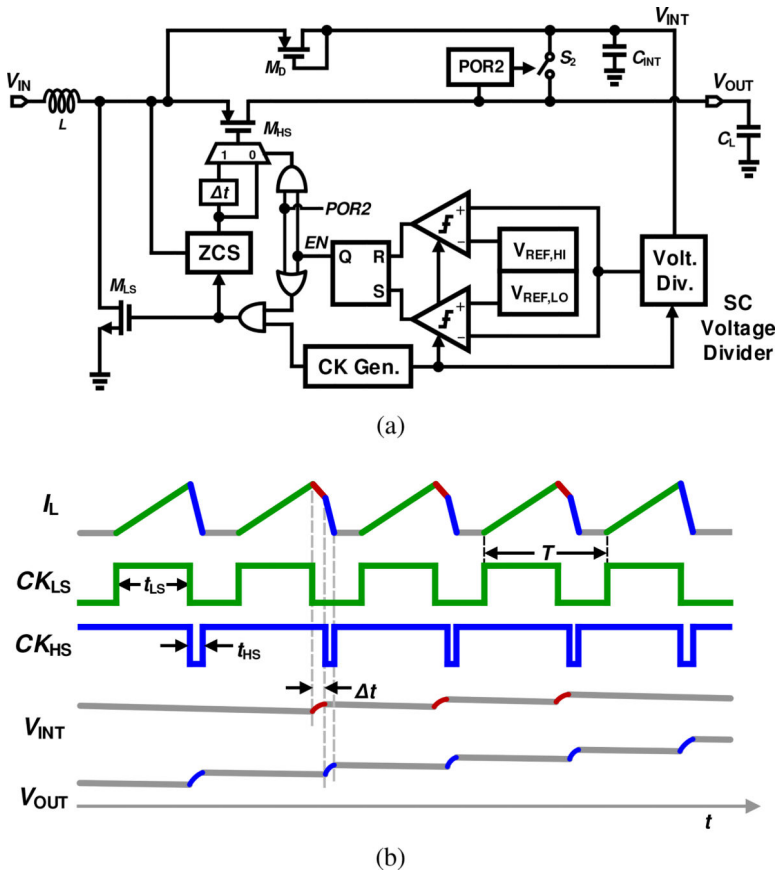

Fig. 9.

(a) Hysteretic on-off voltage regulation using on-chip voltage references. (b) Time-multiplexed, dual-path operation of the single-inductor DC-DC boost converter during start-up.

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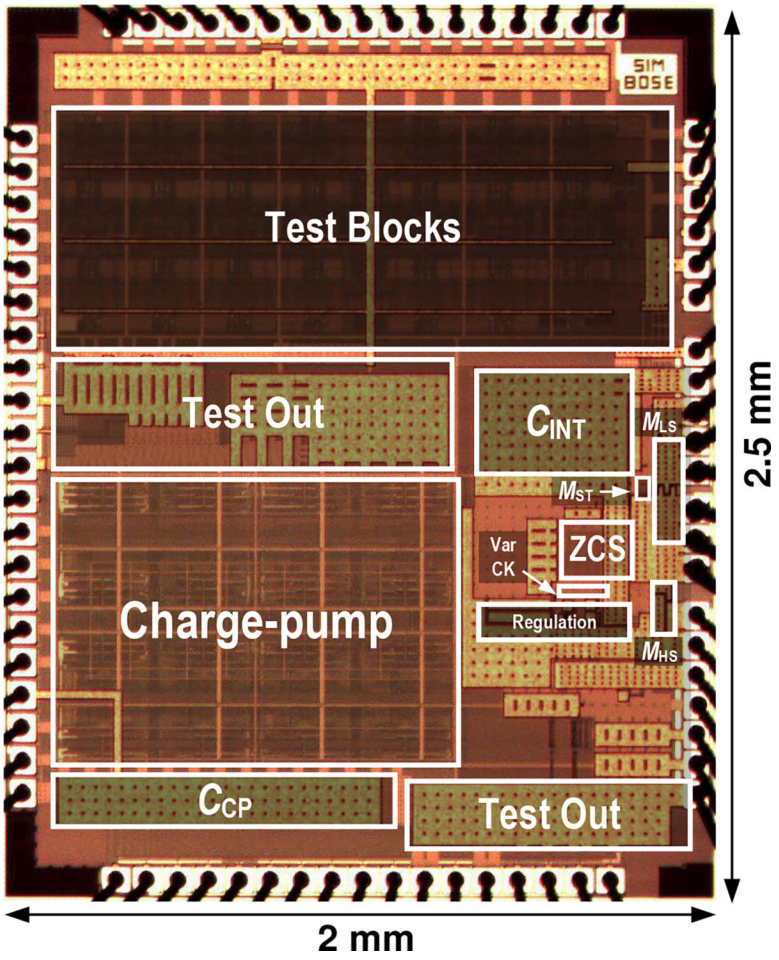

Fig. 10.
Die photo of the chip fabricated in 0.18 μm CMOS technology.

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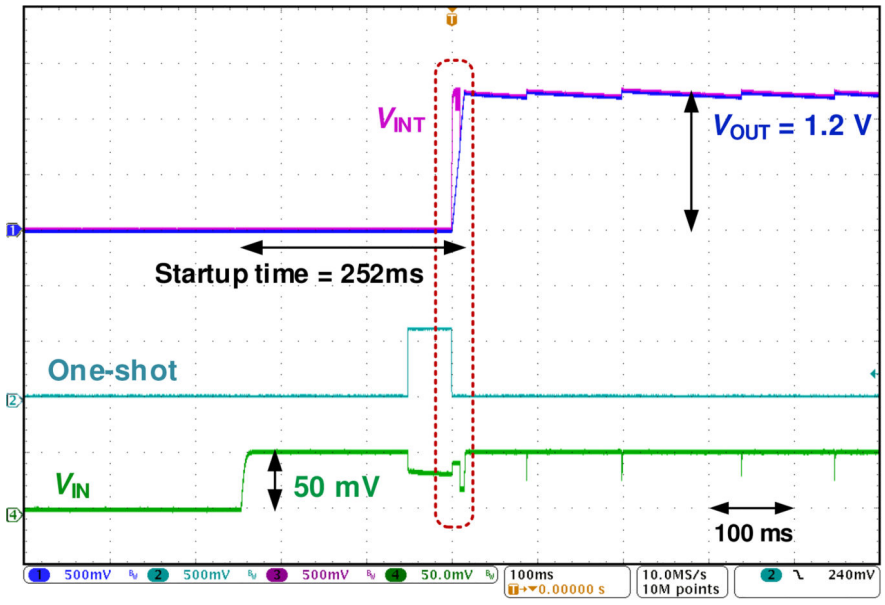
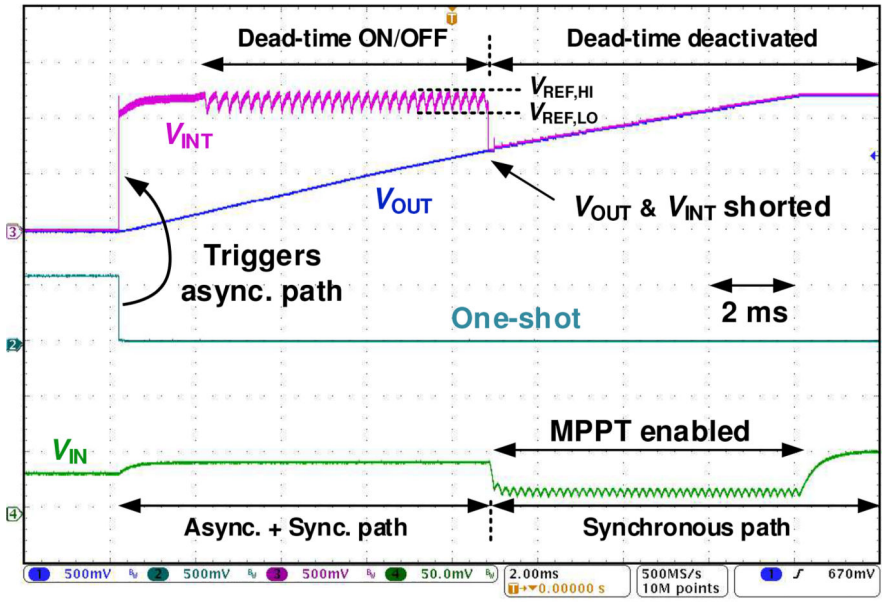


(a)



(b)

Fig. 11.

(a) Measured start-up transients demonstrate self-start of the boost converter with minimum input voltage of 50 mV, and (b) zoomed waveform shows one-shot triggered cold-start sequences, including parallel asynchronous-synchronous operation of the single-inductor boost converter.

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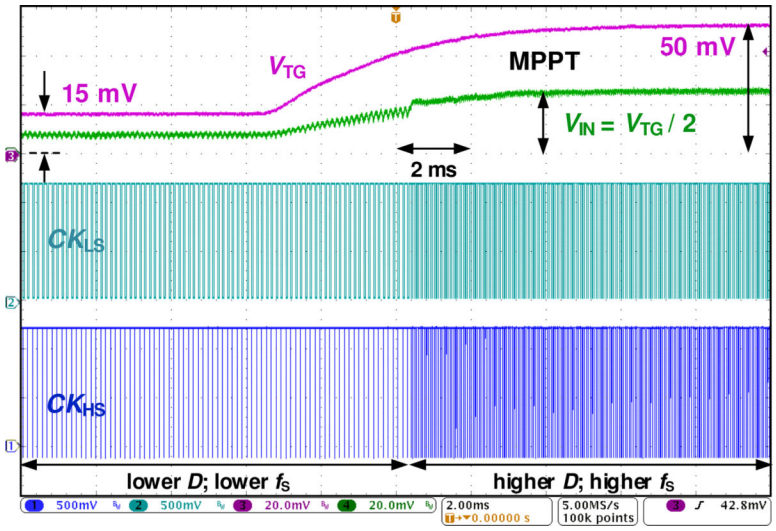

Fig. 12.

Measured transients showing adaptive change of duty-cycle and frequency of switching clock with variation of input voltage for loss-aware MPPT at the input of the converter.

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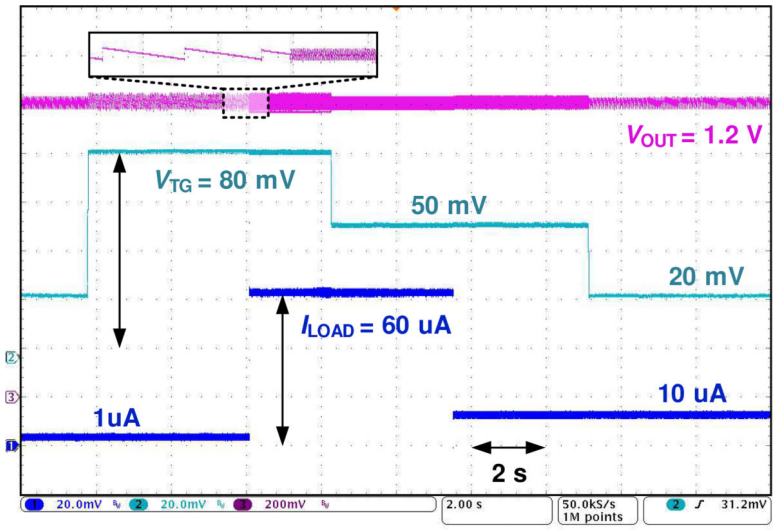

Fig. 13.
Load and line regulation of the output of the boost converter.

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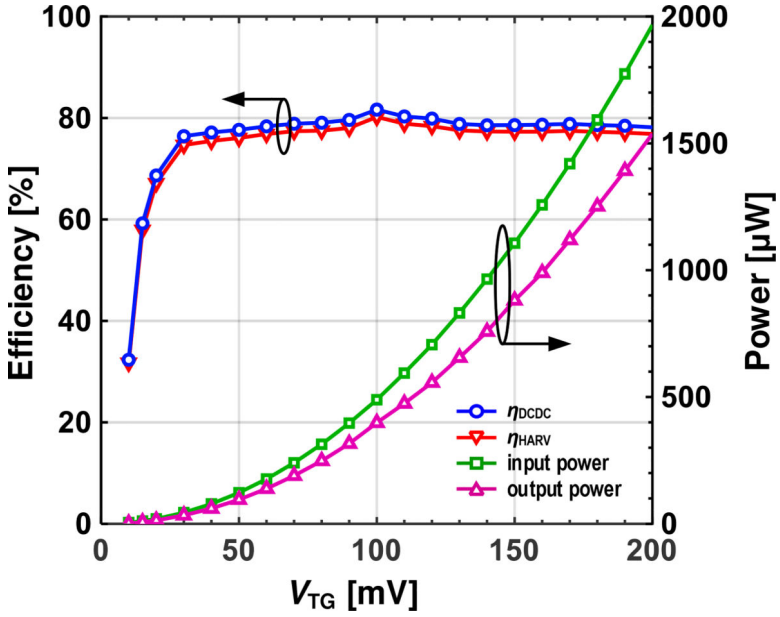

Fig. 14.
Measured efficiency of the boost converter for different TEG voltages.

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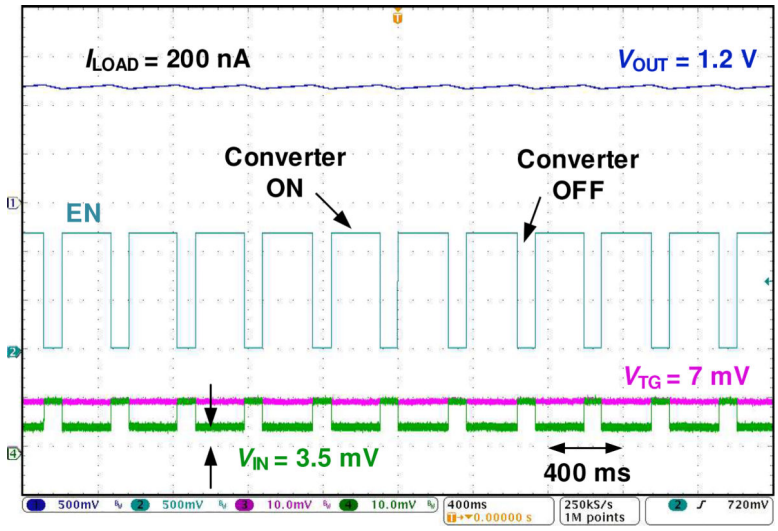

Fig. 15.

Measured transients showing operation of the converter at the lowest input voltage of 3.5 mV with an output regulated voltage of 1.2 V.

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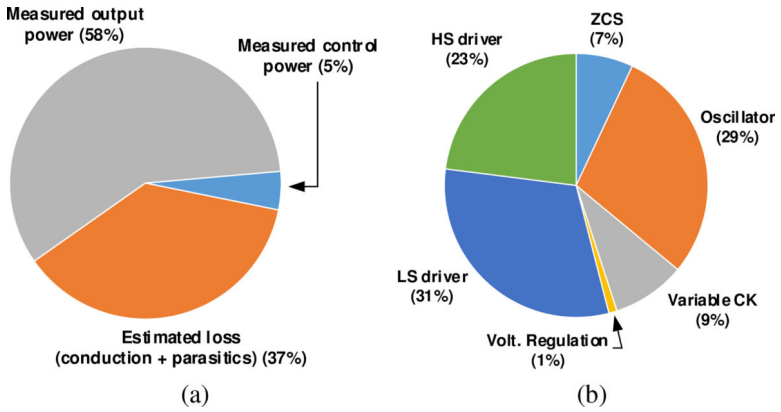

Fig. 16.

Power distribution at V_{TG} = 15 mV: (a) measured output power with estimated loss and (b) break-down of control power by block.

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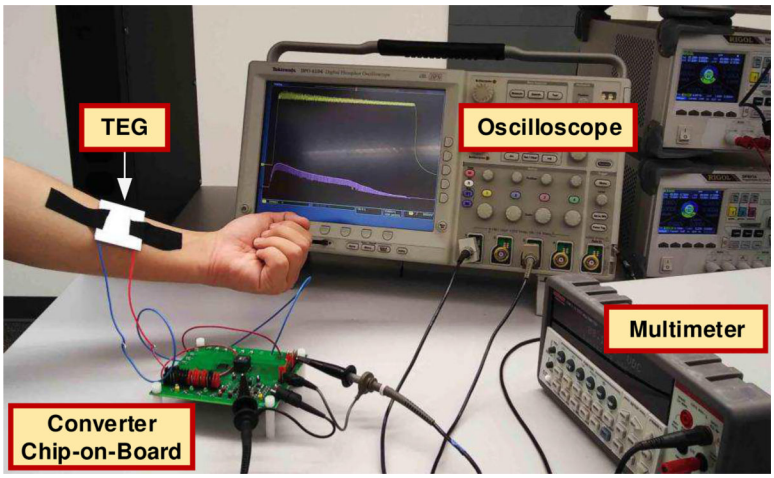

Fig. 17.
Measurement setup with a commercial TEG.

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TABLE I

STARTUP TIMES AT DIFFERENT SOURCE VOLTAGES

Source voltage	Startup time
50 mV	252 ms
75 mV	42 ms
100 mV	21 ms

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TABLE II

PERFORMANCE COMPARISON WITH STATE-OF-THE-ART THERMOELECTRIC ENERGY HARVESTERS

References	JSSC'13 [8]	JSSC'18 [9]	JSSC'12 [7]	JSSC'15 [4]	TCAS'18 [5]	JSSC'16 [10]	JSSC'19 [26]	This work
Process	65nm	65nm	0.13 µm	0.13 µm	65nm	0.13 µm	0.18 µm	**0.18 µm**
Start-up integration	Off-chip	Off-chip	Off-chip	On-chip	On-chip	On-chip	On-chip	**On-chip**
Min. V_{TG} for cold-start	50 mV	40 mV	40 mV	220 mV	210 mV	70 mV	129 mV	**50 mV**
Start-up time	22 ms *(1)*	180 ms *(1)*	22 s *(1)*	3.5 s *(1)*	2.3 s *(1)*	1.5 s	150 s *(1)*	**252 ms**
Min. V_{TG} for operation	30 mV	40 mV	-	20 mV	14 mV	-	50 mV	**7 mV**
V_{OUT}	1.2V	1.1 V	2 V	1.1 V	1.4 V	1.25 V	0.8 V	**1.2 V**
Regulation / MPPT	Yes/Yes	Yes/Yes	Yes/Yes	No/Yes	Yes/Yes	Yes/Yes	Yes/Yes	**Yes/Yes**
Peak harv. efficiency	73%	75%	61%	83% (2)	71.5%	59%	84%	**80%**
Efficiency @ low V_{TG}	45%	12%	32%	21% (2)	50%	-	23%	**58%**
No. of Inductors	3	2	1	1	1	1	1	**1**

(1) Estimated from transient plots

(2) Converter efficiency only.

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