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A Bidirectional Neural Interface SoC With Adaptive IIR Stimulation Artifact Cancelers

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Abstract

We present a 180-nm CMOS bidirectional neural interface system-on-chip that enables simultaneous recording and stimulation with on-chip stimulus artifact cancelers. The front-end cancellation scheme incorporates a least-mean-square engine that adapts the coefficients of a 2-tap infinite-impulse-response filter to replicate the stimulation artifact waveform and subtract it at the front-end. Measurements demonstrate the efficacy of the canceler in mitigating artifacts up to 700 mV_{pp} and reducing the front-end amplifier saturation recovery time in response to a 2.5 V_{pp} artifact. Each recording channel houses a pair of adaptive infinite-impulse-response filters, which enable cancellation of the artifacts generated by the simultaneous operation of the 2 on-chip stimulators. The analog front-end consumes 2.5 μW of power per channel, has a maximum gain of 50 dB and a bandwidth of 9.0 kHz with 6.2 μV_{rms} integrated input-referred noise.

Keywords

artifact cancellation; adaptive LMS; IIR filter; neural recording; neural stimulation

I. Introduction

BRAIN-computer interfaces (BCI) have become an integral component in both research and clinical settings [1]–[4]. Responsive neurostimulation (RNS) is an example of such a closed-loop system that monitors the brain activity continuously in patients with epilepsy using 4 recording channels [5]. When the onset of a seizure activity is detected, stimulation pulses are sent to specific regions of the brain to possibly prevent a seizure. For a chronic implantation of these bidirectional systems in patients suffering from neurodegenerative disorders (e.g. Alzheimer's and Parkinson's diseases), a customized low-power IC that can communicate bidirectionally with the neurons in the brain is needed [Fig. 1(a)]. This IC should be able to simultaneously stimulate different regions of the brain while amplifying and recording the neural activity through high-density micro-electrode arrays (MEA) [6], [7]. The MEAs incorporate metallic surfaces that are in contact with the biological tissue. The metal-electrolyte interface initiates complex electrochemical reactions. However, it has been shown that such an interface can be modeled with an RC network [refer to the inset in Fig. 1(b)] [8]. A double-layer capacitance (C_{DL}) mimics the formation of an ionic layer

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next to the exposed metallic surface and a charge-transfer resistance (R_{CT}) models the electron transfer between the metal and the solution. Fig. 1(b) depicts a simplified model of how the delivery of the stimulation current (I_{stim}) into the target tissue may lead to an undesirable artifact voltage. Since the tissue is conductive, the stimulation current that enters the electrode spreads into the medium (R_{s1} and R_{s2}). This creates a voltage profile in the surrounding tissue, which is received by the nearby recording electrode (Path 1). However, the scenario can become more complex when stimulation and recording are performed using shared electronics and electrode arrays. As shown in Fig. 1(b), due to the impedance which naturally exists at the electrode-tissue interface, the stimulation current induces a stimulation voltage (V_{stim}) at the stimulating electrode. V_{stim} may leak directly to the input amplifier through the parasitic elements that exist in the system, e.g. via a parasitic capacitance (C_p) across adjacent long wires connecting the stimulation and recording electrodes to the bidirectional interface electronics (Path 2). This artifact voltage may reach a few volts at the location of the stimulation, which can easily saturate the low-noise amplifier (LNA) that is conventionally designed to handle μV-level neural signals [9]–[17]. If a 1 V_{pp} artifact contaminates a 10 μV_p neural signal, the system will need to handle a dynamic range of at least 100 dB, which is equivalent to >16b of effective number of bits (ENOB). Different techniques have been proposed to address this issue, which can be categorized into the front-end and back-end mitigation solutions [18]. The front-end techniques aim to prevent the neural signal distortion by addressing the artifact before quantization. The back-end cancellation tries to restore neural information from the contaminated data by using data reconstruction [19] or component decomposition techniques such as the principle component analysis (PCA) and the independent component analysis (ICA) [20], which are computationally expensive and usually performed off-chip. As a more efficient method, back-end stimulation artifact rejection using adaptive digital filters has been implemented [21], [22]. It is critical to note that without any front-end artifact mitigation, the back-end data processing cannot restore the distorted or lost neural data. A straight-forward front-end mitigation technique is to disconnect the amplifier input when the stimulation current is applied, preventing the artifact to appear at the front-end [23]–[25], as shown in Fig. 2(a). However, the artifact blanking method suffers from slow transient settling due to the low high-pass cutoff frequency of the amplifier. A more severe drawback is the complete loss of the neural data during the stimulator activity, which worsens as the number of the stimulation channels increases. To prevent losing any neural signal, high resolution ADCs [26] can be implemented to accommodate the full range of the artifact voltage, as shown in Fig. 2(b). ΔΣ-modulator front-ends [27]–[29] use a high oversampling ratio (OSR) to achieve the required ENOB, which results in additional power consumption during the decimation and post-processing of the over-sampled data. As an alternative to the voltage-domain quantization, a front-end voltage-controlled oscillator (VCO) can translate the full-scale voltage variations into time-encoded data, which relaxes the analog front-end (AFE) circuitry design by removing the need for voltage amplification [30]–[32]. Since the voltage-to-frequency conversion is a highly nonlinear process, a nonlinearity correction block is needed to compensate for the added distortion. An alternative method to suppress the VCO nonlinearity is to embed the VCO and quantizer in a feedback loop [33]. High resolution ADCs with competitive power consumption (including the decimation circuitry) have been demonstrated mainly for input frequencies up to 500 Hz, which are only suited for recording

the local field potentials (LFP) and not the action potentials (AP). However, recording the AP or spikes, which occupy frequencies up to a few kHz, is critical for neuroscientists to understand how neuronal units and populations communicate with each other to function properly (e.g. short-term memory encoding [34]). Scaling these systems to handle a larger input bandwidth significantly adds to the power consumption and system complexity, since the switching frequency required at the front-end quantizer and the back-end digital circuitry for decimation and/or non-linearity correction scales linearly with the maximum bandwidth of the input signal. In another effort to handle a wide input dynamic-range, front-end differentiators and Δ-modulators have been proposed to take advantage of the $1/f^{1\sim3}$ power spectral density of the neural data [35]–[39]. As Fig. 2(c) shows, Δ-modulation flattens the signal power over the neural signal bandwidth by amplifying the low-power high-frequency components (AP) more than the high-power low-frequency components (LFP). This can relax the dynamic range requirement of the quantizer. The main drawback of this scheme for stimulation artifact cancellation is that the artifacts can have large fundamental and harmonic spectral components in the kHz range [40], which can not be mitigated by front-end Δ-modulation.

Past *in vivo* measurements have demonstrated a less than 10% variation in the artifact waveform during a stimulation session [41]. This suggests that a periodic stimulation signal would generate a periodic artifact, implying that the recording system does not necessarily need to quantize the full artifact waveform at every stimulation cycle. If a replica of the artifact waveform is periodically subtracted from the incoming contaminated signal before quantization, the DR requirements of the recording ADC can be significantly reduced. Consequently, adaptive artifact mitigation in the front-end has been proposed, which can potentially provide a flexible, scalable and low-power solution for artifact cancellation in a high-density neural-interface platform. It reduces the dynamic range at the AFE input and enables the use of conventional successive-approximation-register (SAR) ADCs with ENOB <11, while preserving both the LFP and AP neural data [42]–[46]. The concept of the adaptive filtering scheme is shown in Fig. 2(d). When the stimulation signal $s[n]$ is activated, the stimulation current enters the electrode-tissue interface, creating an artifact voltage at the stimulating electrode surface. This artifact voltage is picked up by the recording electrodes as $a[n]$, corrupting the received neural data $x[n]$. In order to suppress the undesirable large-signal artifact, which can potentially saturate the front-end amplifiers, an on-chip digital filter $H_m(z)$ is used to mimic the response of the electrode-tissue interface. This digital filter generates a replica of the artifact voltage $y[n]$ and applies it to the LNA input, suppressing the artifact waveform at the front-end. The cancellation filter $H_m(z)$ can be realized either with a finite impulse response (FIR) or an infinite impulse response (IIR) configuration. Before choosing the architecture, we should first investigate the possibility of developing a simple model that can mimic the artifact waveform.

II. Modeling the Stimulation Artifact

Fig. 3(a) shows the experimental setup that was used for characterizing the artifact voltage. A parylene-based micro-electrode array [47] was used to investigate the challenging case of stimulation and recording from electrodes on a single shank, spaced just 2 mm apart. A biphasic 35 μA stimulation current, with 330 μs per phase, was applied to electrode 4 (E_4,

with a diameter of 210 μm), while the waveform of electrode 2 (E_2, with a diameter of 60 μm) was measured as the target recording site in this example. Fig. 3(b) plots the stimulation voltage and the resultant artifact waveform. Due to the similarity between the waveform of the stimulation and artifact voltages, a simple series RC network (R_m,C_m) was examined as a potential model for the artifact waveform [Fig. 3(a)]. Through computer simulations, the optimized RC parameters that recreated the waveform of the artifact voltage were found [Fig. 3(c)]. The simulated response of the RC model (V_{model}) is plotted in Fig. 3(b). Examining the difference between V_{model} and V_{in} demonstrates that during the stimulation phase, the model can emulate the artifact with a maximum of 50 mV discrepancy (For 70% of the stimulation time, this discrepancy is less than 20 mV). Hence, in this example, if we could physically create V_{model} and subtract it from V_{in} before amplification, the dynamic range (DR) that the AFE needs to accommodate reduces from 380 mV to 50 mV, which is a factor of 7 or equivalently 3 bit improvement in the required DR for the AFE+ADC signal path. After the stimulation phase, due to the mismatch between anodic and cathodic currents, there is a residual charge on the stimulation electrode which discharges slowly as can be seen in Fig. 3(b). Charge balancing techniques [48] can be implemented to suppress this slowly decaying waveform, which is beyond the focus of this article.

An straightforward way to implement the model is to physically realize R_m and C_m on chip. However, implementing a nF-range capacitance on-chip and copying the stimulation current to regenerate the artifact waveform is not an efficient solution. It may be possible to implement the RC network in the digital domain with a more compact footprint. The transfer function of the RC model can be written as $H_m(s)=\frac{1+sR_mC_m}{sC_m}$ Through a bilinear transformation, by substituting s with $\frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$ (T_s: sampling period), the Z-domain transfer function can be derived as,

$$H_m(z) = \frac{b_0 + b_1 z^{-1}}{1 - z^{-1}}, \tag{1}$$

where b_0 and b_1 are functions of T_s, R_m and C_m. Approximating the continuous V_{model} with a discrete-time waveform ($V_{replica}$) introduces residual artifact. The value of T_s should be chosen small enough to reduce the residual artifact voltage [i.e. $V_{residue}$= V_{model} - $V_{replica}$, as shown in Fig. 3(d)] sufficiently below the level that would saturate the front-end LNA. This criterion sets the minimum required sampling speed of the digital filter as a function of the peak stimulation current and the electrode-tissue capacitance,

$$\frac{I_{peak}}{C_{DL}} T_s < \frac{VDD}{G}. \tag{2}$$

Assuming I_{peak} = 100 μA, C_m = 30 nF, the LNA supply voltage VDD = 1.0 V and the LNA gain G = 25, the upper limit for T_s can be derived as 12 μs.

Past work has implemented adaptive FIR filters to replicate and cancel the artifact waveform at the front-end. However, this topology requires a large number of taps [42] to reproduce the artifact waveform, which can be attributed to the existence of a pole in $H_m(z)$. In

high-density MEAs where recording and stimulation electrodes are close, the artifact level may reach a few volts, which is an order of magnitude above the performance limits of the existing FIR schemes [42]–[46]. However, an IIR implementation of the digital filter realizes a pole which can better approximate the electrode response and drastically improve the cancellation performance. The reduced number of coefficients in the IIR implementation carries the following additional advantages: (1) reduced silicon area for filter realization and (2) reduced computational power, both by an order of magnitude as shown in Fig. 4. Here we present an adaptive IIR stimulation artifact canceler; Section III discusses different aspects of the design strategy, section IV describes the system operation, and section V shows the AFE characterization and canceler performance in different scenarios.

III. System-Level Analysis

Fig. 5(a) shows the simplified configuration of the amplifier chain with the cancellation capacitive DAC (CDAC). An artifact waveform appearing at the amplifier input consists of differential-mode (DM) and common-mode (CM) components [Fig. 5(b)]. Since the cancellation filter injects the artifact replica ($y[n]$) to the LNA input differentially, the differential component of the artifact is canceled; however, the CM component is not affected, which can deteriorate the AFE linearity by perturbing the device biasing. To quantify the tolerable common-mode artifact, let us consider the front-end of an AFE with the cancellation DAC capacitors (C_{DAC}) connected to the virtual ground, as shown in Fig. 5(b). Assuming that the operational transconductance amplifier (OTA or g_m cell) has a low common-mode gain (<1), any input common-mode signal experiences a capacitive division at the virtual ground according to

$$V_{i,OTA,CM} = \frac{C_1}{C_1 + C_{DAC}} V_{in,CM}, \tag{3}$$

assuming negligible parasitic capacitance at the OTA input. Considering a conventional inverter-based g_m cell, the input common mode range can be given by,

$$V_{OV,6} + V_{GS,1} < V_{i,OTA,CM} < VDD - V_{OV,5} - V_{SG,3}. \tag{4}$$

Assuming $VDD = 1\,V$, $V_{OV,5} = V_{OV,6} = 100mV$ and $V_{GS,1} = V_{SG,3} = 350mV$, the input-common mode range of the OTA can be calculated as $0.45\,V < V_{i,OTA,CM} < 0.55\,V$. This sets a limit on the maximum input common-mode range that the amplifier can tolerate as shown below,

$$V_{in,CM,max} = \left(1 + \frac{C_{DAC}}{C_1}\right)(100mV). \tag{5}$$

Noise, area and power consumption should also be considered when adding additional circuitry to the front-end. Fig. 6(a) shows the simplified signal flow diagram and noise sources in the system. The total input referred noise can be derived as,

$$v_{n,in,total}^2 = v_{n,bio}^2 + v_{n,elec}^2 + v_{n,amp}^2 + \frac{v_{n,kT/C_{ADC}}^2 + v_{n,q}^2}{G^2}, \quad (6)$$

where $v_{n,bio}$ is the biological background noise, $v_{n,elec}$ corresponds to the electrode thermal noise, $v_{n,amp}$ is the input-referred noise of the amplifier, $v_{n,kT/C_{ADC}}$ captures the ADC sampling noise, $v_{n,q}$ is the ADC quantization noise and G is the gain of the amplifier. The amplifier noise $v_{n,amp}$ can be derived from the circuitry in Fig. 5,

$$v_{n,amp} = \frac{C_1 + C_{DAC} + C_{FB1}}{C_1} v_{n,OTA}, \quad (7)$$

$$v_{n,OTA} = \sqrt{\frac{4kT\gamma BW}{g_m}}, \quad (8)$$

where γ is the MOSFET noise factor, T is the temperature in Kelvins, k is the Boltzmann constant, BW is the system's effective bandwidth and g_m is the transconductance of $M_{1,2,3,4}$. Also, the flicker noise is considered negligible compared to the thermal noise, but should be included for a more thorough analysis. Assuming that the devices in the OTA are biased in weak inversion for maximum efficiency, $\frac{g_m}{I_1} = \frac{1}{nV_T}$, where I_1 is the DC current in each branch of the OTA, n is the subthreshold factor and V_T is the thermal voltage. The biological background and electrode noise depends on the electrode and the live tissue conditions, and not the electronics circuitry. Hence, in the following discussion, the focus will be on the noise contribution of the electronics, namely the amplifier and ADC. Assuming $C_{FB1} \ll C_1$ (LNA typically has a gain$\gg$1), $v_{n,in,total}$ can be rewritten as,

$$v_{n,in,total}^2 = \frac{\frac{2kT}{C_{ADC}} + \frac{\Delta^2}{12}}{G^2} + \left(1 + \frac{C_{DAC}}{C_1}\right)^2 \frac{4kT\gamma n V_T BW}{I_1}, \quad (9)$$

where C_{ADC} is the ADC single-sided sampling capacitance and Δ is the magnitude of the least-significant bit (LSB) of the ADC. The LSB is a function of the ADC full-scale differential voltage (in this case 2VDD) and resolution (N), as given by $\Delta = \frac{2VDD}{2^N}$. Fig. 6(b) shows that without stimulation artifact cancellation, the maximum input the system receives increases from the maximum desired signal (x_{max}, usually a few mV in the LFP band) to the maximum artifact level (a_{max}, up to a few Volts). Therefore, assuming that the minimum desired signal to be detected is as low as the noise floor, the additional required number of bits imposed by the artifact is $log_2(\frac{a_{max}}{x_{max}})$. However, if a replica of the artifact (y) is subtracted from the input signal, the swing of the input waveform reduces to the the magnitude of a residual artifact, $a_{res} = a - y$, which depends on the accuracy of the artifact prediction model. Using such an artifact mitigation approach reduces the required ENOB by $log_2(\frac{a_{max}}{a_{res,max}})$, as shown in Fig. 6(c). Therefore, reducing an artifact amplitude from 500 mV

to 50 mV at the front-end is equivalent to a 3.3-bit reduction in the required ENOB for the recording system.

On the other hand, the maximum residual artifact limits the maximum gain the AFE can accommodate before saturating the amplifier, as given by $G_{max} = \frac{VDD}{a_{res,max}}$. Under these conditions, (9) can be rewritten as,

$$v_{n,in,total}^2 = \frac{2kT}{C_{ADC}}\left(\frac{a_{res,max}}{VDD}\right)^2 + \frac{a_{res,max}^2}{3(2^{2N})} + \left(1 + \frac{C_{DAC}}{C_1}\right)^2 \frac{4kT\gamma n V_T BW}{I_1}. \quad (10)$$

Equation (10) provides the basis for evaluating the trade-off that exists between the noise floor, ADC resolution, AFE power, C_{DAC} and C_{ADC} values (area) and maximum residual artifact. $a_{res,max}$ depends on the accuracy of the training model, and depending on the target setup and experimental conditions, it should be measured early in the system design process. Larger residual artifacts (or equivalently the estimation error) require a higher ENOB and a larger sampling capacitor for the ADC to maintain the noise performance. On the other hand, if the amplifier noise is dominant, even though a larger C_{DAC} provides a higher input CM resilience as suggested by (5), the AFE should consume more power to maintain the target noise level. A larger C_{DAC} would also occupy more chip area. To evaluate the noise performance of the system, let us assume that the system should be resilient to CM artifacts up to 200 mV, which according to (5) requires $C_{DAC} = C_1$. For a target requirement of the area, noise and power consumption of the system, the design parameters should be optimized. In this work, the main focus is on the implementation of the proposed front-end cancellation scheme as a proof-of-concept, which by itself can potentially reduce the burden on the recording system as discussed before. Therefore, the design parameters were chosen based on the conventional front-ends: $N = 10$, $C_{ADC} = 2.5pF$, $VDD = 1\,V$, $I_1 = 1\mu A$, $n = 1.5$, $\gamma = 2/3$. Following the discussion in section II, $a_{res,max}$ is assumed to be 50 mV. Under these assumptions, the input-referred noise in (10) can be calculated as,

$$v_{n,in,total} = \sqrt{(2.9\mu V)^2 + (28.2\mu V)^2 + (4.2\mu V)^2}, \quad (11)$$

which yields $v_{n,in,total} = 28.6\mu V_{rms}$. In this scenario, the ADC quantization noise (28.2 μV) dominates the overall noise performance. Depending on the target application and the minimum signal level to be detected, higher resolution ADCs may be needed to reduce the quantization noise, preferably below the thermal noise of the amplifier. In fact, if an ADC with N-bit resolution is used, by adding the proposed front-end cancellation scheme, which can potentially reduce a 500 mV artifact to 50 mV residual artifact, the input-referred total ENOB accommodated by the system would increase to N+3.3 bits.

IV. Circuit Implementation

A. System Architecture

Fig. 7 shows the implemented SoC which consists of two identical subsystems, each having four recording front-ends (REC) and a biphasic neural stimulator 7b-current DAC (IDAC). A front-end switching matrix (SW_{i-}, SW_{i+}, i= 0–7) can reconfigure the stimulator connection to any of the recording electrodes on-the-fly. This enables reusing the electrodes for both recording and stimulation, which can potentially prevent additional electrode routing and placement in the brain and reduce the damage to the tissue. The digitized outputs of all the 8 recording channels are serialized, packetized and transmitted via 2 serial lines ($Serial_{out}$ and CLK_{out}). Fixed preamble and postamble bit patterns are added to the bit-stream to flag the start and end of the consecutive data packets. An on-chip 25 MHz RC digital relaxation oscillator generates a tunable core clock for the chip, which is used to create proper timing for the operation of the SAR ADC, stimulation circuitry, LMS-IIR filter and data transmission. Low-dropout regulators combined with the bandgap voltage circuitry generate 3 main supplies for proper chip operation, namely the core analog and digital supply voltages AVDD and DVDD (both equal to 1 V) in addition to the 3 V supply voltage AVDDST. Since the stimulation IDAC operates within 3 V and 0 V limits, the tissue should be biased to half this range to achieve the maximum headroom for source and sink transistors in the IDAC. Hence, a unity-gain buffer is designed to set the body voltage at V_{CMST} = 1.5 V, which is half AVDDST. IDAC is designed with 7-bit binary-weighted PMOS and NMOS current sources, providing up to 127 μA maximum current with 1 μA resolution.

B. Recording Channel Circuitry

The detailed block diagram of the REC block is shown in Fig. 9. All blocks are fully differential; but, for simplicity, the single-ended version is depicted. Each REC block incorporates a front-end 2-stage LNA, followed by a programmable gain amplifier (PGA). As shown in Fig. 8(a), the first stage of the LNA has an inverter-based topology to provide a power-efficient low-noise front-end. It is followed by a Miller-compensated active-load differential pair with a switchable tail current. To save the chip area, the LNA is reused during the training phase to amplify the difference between the artifact and its replica, which requires a faster settling in this phase. Hence, the LNA can be switched between regular-bandwidth and high-bandwidth modes. The PGA provides a tunable gain and also acts as an anti-aliasing filter for the ADC, by limiting the signal bandwidth to about 10 kHz to reject the out-of-band noise and distortions [Fig. 8(b)]. The low-pass corner of the PGA is determined by the mid-band gain $\left(\frac{C_2}{C_{FB_2}}\right)$, transconductance of the OTA (g_{m2}), and the capacitive load of the SAR ADC (C_{ADC}) as $\mathrm{BW} = \frac{g_{m2}}{2\pi\frac{C_2}{C_{FB2}}C_{ADC}}$. The transconductance is tunable to meet the minimum bandwidth requirement for different gain settings. The output stage of g_{m2} accommodates a wide-swing differential output during the signal acquisition. To ensure that the PGA can maintain the maximum output swing (V_{FS}= 1V) in the available tracking time of the ADC, which is about 70% of the sampling period in this design

(T_s=50μs), the DC current of its output stage (I_o) should be at least $\frac{C_A DC \frac{V_{FS}}{2}}{0.7T_s}$, which requires I_o>34 nA. Since the artifact voltage may appear with different amplitudes at the input of each recording channel depending on the distance of the electrode to the stimulation site, each recording channel is equipped with an independent adaptive cancellation filter. A 10b binary-weighted split-array capacitive DAC (CDAC) converts the digital filter output to a differential artifact replica, which is applied to the LNA input terminals, as illustrated in Fig. 8(a). Since the digital blocks operate at 1 V, level-shifters are needed to provide 3 V control signals for driving the switches in the CDAC. The CDAC output capacitance at the virtual ground terminals of the LNA degrades the input-referred noise. Therefore, during the acquisition phase and in the absence of any stimulation signal, the CDAC capacitors can be open-circuited to improve the AFE noise performance.

C. Operation of the AFE with the Adaptive IIR Filter

We used the simplified transfer function of the electrode-tissue interface as our system model to be trained: $H_m(z)=\frac{b_0 + b_1 z^{-1}}{1 - z^{-1}}$. The implemented adaptive algorithm adjusts the filter coefficients using the equation-error approach [49]. Such configuration guarantees global convergence as with an adaptive FIR filter.

1) Learning (Training) Phase: During the training phase the PGA is disconnected, as shown in Fig. 9(a). The input voltage V_{in} is directly buffered to the ADC through the ADC driver [Fig. 8(c)], generating the quantized artifact signal $a[n]$. The unity-gain ADC driver is used to isolate the recording electrodes from the switching transients during the sampling period of the SAR ADC operation. The driver also removes the input common-mode component and provides a differential waveform at the ADC input. In this phase, the ADC operates with $V_{reference}$ = 3 V to accommodate the high-voltage artifact. Its sampling rate should match the clock frequency of the digital filter and the CDAC switching speed, which is set to $F_{s,train}$ = 78.4 kHz. This high sampling rate reduces the residual artifact at the AFE input below the saturation limit of the amplifier, as was derived in (2). Moreover, the chosen $F_{s,train}$ reduces the quantization noise power injected by the CDAC in the ADC's Nyquist bandwidth (f < 10 kHz) during the acquisition phase. To accommodate a high slew-rate during comparison, the LNA is switched to the high-bandwidth mode. It operates as a pre-amplifier for the equation-error comparator, which generates the 1-bit equation-error $e[n]$ based on the comparison between V_{in} and $V_{replica}$. To simplify the hardware implementation of the LMS algorithm, a sign-sign scheme is realized [42], [43]. For each stimulator, the sign of each stimulation signal is represented with 2 bits ([s_{10}, s_{11}] for stimulator 1 and [s_{20}, s_{21}] for stimulator 2), to accommodate 3 possibilities of anodic (positive), cathodic (negative) and disabled current stimulation. All the mathematical operations are performed in a 2's complement system to accommodate negative numbers. To enable simultaneous cancellation of 2 independent stimulation signals, each channel has 2 pairs of 10b coefficients [b_{10}, b_{11}] and [b_{20}, b_{21}], which are independently adapted to their corresponding stimulation signals $s_1[n]$ and $s_2[n]$. In a general scheme with N stimulators, the coefficients are updated according to,

$$\begin{pmatrix} b_{j0}[n] \\ b_{j1}[n] \end{pmatrix} = \begin{pmatrix} b_{j0}[n-1] \\ b_{j1}[n-1] \end{pmatrix} + \mu \; sign \begin{pmatrix} s_j[n] \\ s_j[n-1] \end{pmatrix} e[n], \tag{12}$$

where j is the stimulator index (j= 1…N). In this implementation, the adaptation constant μ is set to 1 for hardware simplification. It should be emphasized that for a guaranteed coefficient convergence, the coefficients corresponding to each stimulator need to be trained separately, when all other stimulators are disabled. However, during the acquisition phase the stimulators can be activated simultaneously and there is no timing constraint. In the example shown in Fig. 9(a), [b_{10}, b_{11}] are being adapted to [s_{10}, s_{11}], while the second stimulator is disabled, [s_{20}, s_{21}]= 0. The artifact replica $y[n]$ at each cycle is estimated by the summation of the delayed quantized artifact $a[n-1]$ and the digital filter output, according to,

$$y[n] = a[n-1] + \begin{pmatrix} b_{j0}[n] & b_{j1}[n] \end{pmatrix} \cdot \begin{pmatrix} s_j[n] \\ s_j[n-1] \end{pmatrix}. \tag{13}$$

Since the adaptation constant is fixed, the training time scales linearly with the artifact peak-to-peak voltage, at a rate of 20 mV_{pp} per stimulation pulse applied to a resistive load. For instance, for a 200 mV_{pp} artifact, 10 stimulation cycles are needed to train the filter coefficients.

2) Acquisition Phase: When the training phase is complete and the filter coefficients are adapted to their corresponding stimulation signals, the system enters the acquisition phase [Fig. 9(b)]. The IIR filter generates the artifact replica waveform in response to the stimulation signals, given by

$$y[n] = y[n-1] + \sum_{j=1}^{N} \begin{pmatrix} b_{j0,\,opt} & b_{j1,\,opt} \end{pmatrix} \cdot \begin{pmatrix} s_j[n] \\ s_j[n-1] \end{pmatrix}, \tag{14}$$

where [$b_{j0,opt}$, $b_{j1,opt}$] are the converged filter coefficients. The LNA is switched back to the regular-bandwidth mode and the PGA is switched into the amplification chain, connecting the LNA output to the ADC. The equation-error comparator and the ADC driver are disabled and disconnected from the rest of the circuitry. In this phase, the sampling rate of the SAR ADC reduces to $F_{s,acq}$ = 19.6 kHz, which is sufficient to accommodate the neural signal bandwidth, while preventing any excess power consumption for digitization and data transmission. The ADC also operates with $V_{reference}$ = 1 V, which is sufficient to accommodate the amplified neural signal and the residual stimulation artifact.

V. Measurements

A. System Performance

The 0.18μm CMOS SoC microphotograph is shown in Fig. 10. The chip occupies 11.4 mm^2 of area and consumes a total of 206 μW of power when all the recording channels are in the acquisition mode and one stimulator is delivering a biphasic 40 μA peak current with cathodic and anodic pulse widths of 300 μs and a period of 2 ms. The power

consumption breakdown is shown in Fig. 11(a). The current consumption of different supply voltages in different operation modes is also plotted in Fig. 11(b). Fig. 12 shows the measured frequency response of the AFE (LNA in the regular-bandwidth mode+PGA) and its input-referred noise spectral density. The AFE achieves a 9 kHz bandwidth, an integrated input-referred noise of 6.2 μV_{rms} and a common-mode-rejection-ratio (CMRR, defined as the ratio of the differential gain to the CM-to-differential conversion gain) of 43.2 dB at the maximum differential gain of 50.0 dB. Analysis and simulations suggest that an imbalance between the parasitic capacitances at the virtual ground nodes of the LNA dictates the maximum CMRR in our design. A more careful layout of the LNA with a better routing symmetry should achieve a higher CMRR. The AFE was originally designed to achieve sub-Hz high-pass cutoff frequency by using switchable pseudo-resistors around the g_m cells [refer to Fig. 8(a)]. However, the n-well to p-substrate leakage current disrupted the feedback DC path around the LNA and PGA when the pseudo-resistors were enabled (V_R= 1 V). For proper DC biasing, the pseudo-resistors had to be shorted (V_R= 0 V), which resulted in a high-pass cutoff frequency of 200 Hz (sufficient to record the AP but not the LFP). The increase in the high-pass corner also contributed to the degradation of the input-referred noise. For future designs, especially those with TΩ-range effective resistances, substrate leakage compensation techniques should be implemented [50]. The dynamic linearity performance of a stand-alone SAR ADC was measured in 2 different settings corresponding to the different modes of operation: (1) Sampling speed $F_s = F_{s,train}$ and $V_{reference}$ = 3 V, (2) $F_s = F_{s,acq}$ and $V_{reference}$ = 1 V. At the Nyquist frequency, the ADC maintains an SFDR and ENOB of 62 dB and 8.6b for $F_{s,acq}$ and 56 dB and 7.6b for $F_{s,train}$. The stand-alone CDAC could not be characterized with the available setup; however, the parasitic extracted simulations showed that it maintained a spurious-free dynamic range (SFDR) of 68 dBFS for a 10 kHz output signal.

B. Stimulation Artifact Canceler Performance

1) Single Channel Stimulation: Depending on the relative location of stimulation and recording sites in the tissue, the stimulation artifact can couple into the amplifier input in 3 different modes: differential, common-mode and single-ended, as demonstrated in Fig. 13. In the following benchtop characterization, an off-chip circuitry was implemented to artificially generate each mode, as shown in Fig. 13. The functionality of the adaptive IIR filter was first investigated in the presence of single-ended artifact generated from a single-channel stimulation, as shown in Fig. 14(a). An arbitrary function generator (AFG) generated a 400 μV_p, 3.05 kHz sinusoidal signal $x(t)$ (mimicking the neural signal), which was applied to all the recording channels with the AFE gain programmed to 27.6 dB. With this setting, the signal-to-noise ratio (SNR) of the recorded signal is about 10 dB, when averaged across channels. In the training phase, the AFG was disconnected and the stimulation signal (stim_en) enabled stimulator 1 to apply a balanced biphasic 19 μA stimulation current, with 330 μs duration per phase and repetition rate of 140 Hz, into an off-chip 9.5 kΩ resistor to generate a biphasic artifact waveform. The generated artifact waveform $a(t)$ was fed to the recording channels and all the 8 REC blocks were allowed sufficient time for training their IIR filter coefficients during Φ_{train}. At the beginning of the acquisition phase during Φ_{acq1}, the chip output, which carried the residual artifact $V_{residue}$, was stored in MATLAB. During Φ_{acq2}, which was the final phase of the testing cycle, the

AFG and stimulator 1 were both active and $x(t)$ was summed with $a(t)$ artificially using an off-chip op-amp circuitry shown in Fig. 14(b). The stored $V_{residue}$ was subtracted from the chip output (V_{acq}) and divided by the system AFE gain in this phase to recover the input-referred sinusoidal signal (V_{rec}). The resultant artifact and input sinusoidal signals are depicted in Fig. 15(a)–(b). The goal of the experiment was to recover the 3.05 kHz signal with minimal distortion, while maintaining the signal amplitude. The functionality and efficacy of the implemented front-end adaptive cancellation was investigated by comparing the recovered signal when the canceler IIR filter was enabled (canceler ON) versus when the filter was disabled (canceler OFF), while the back-end cancellation remained active in both cases. Fig. 15(c) demonstrates that the front-end IIR filter is mitigating the artifact, resulting in a minimal $V_{residue}$. The ADC output during the acquisition phase shows a reduced artifact on top of the sinusoidal signal [Fig. 15(d)]. The recovered signal in Fig. 15(e) shows that without the front-end canceler, the sinusoidal waveform is completely lost in the background noise during the stimulation phase. A time window of 32 samples, equivalent to 1.6 ms starting from the onset of the stimulation signal, was chosen for spectral analysis. By comparing the Fourier transform of the recovered signals in Fig. 15(f), a complete recovery of the fundamental tone was observed when the IIR filter was active. When the front-end canceler is off, the large-swing artifact saturates the LNA, which results in increased distortion and failure to detect any underlying signal. It is important to note that the selected 1.6 ms duration for the time window is about the average duration of a neural spike. Hence, without the canceler, any neural spike which is coincident with the stimulation signal could be easily lost in this scenario.

The same characterization steps were performed for differential and common-mode stimulation artifacts as well. To evaluate the efficacy of the proposed cancellation scheme in suppressing different artifact intensities, the stimulation current was swept from 1 μA to 35 μA, while the load impedance was an off-chip 9.5 kΩ resistor. Figure. 16(a) plots the measured system effective gain (defined as the ratio of the intensity of the recovered fundamental tone to the input signal) as a function of the artifact peak-to-peak voltage. To quantify the signal distortion and noise introduced by the artifact, the SNR was also measured using the frequency spectrum of the recovered signal, which is shown in Fig. 16(b). Both the effective gain and SNR metrics were measured for all the 8 channels and the average values with $\pm 1\sigma$ variation across the channels are shown in Figure. 16. For differential and single-ended modes, at medium-level artifact amplitudes (< 200 mV_{pp}), the effective gain of the system is slightly improved (< 2 dB) when the front-end canceler is enabled. SNR also shows similar behavior with an improvement of < 4 dB for small artifact amplitudes. As the artifact level increases to about 400 mV_{pp}, for both the single-ended and differential modes, the amplifier is significantly saturated and the effective gain drastically drops by about 10 and 6 dB, respectively. However, enabling the canceler restores the effective gain and prevents signal attenuation. Moreover, the front-end canceler also improved the SNR by more than 8 dB for artifact amplitudes above 200 mV_{pp}. Assuming a 0-dB SNR is the limit for a likely detection of spikes [51], these measurements suggests that the canceler can recover 400 μV high-frequency signals in the presence of 600 mV_{pp} single-ended and > 700 mV_{pp} differential artifacts. Preserving the gain for large artifacts (> 700 mV_{pp}) also suggests that the canceler is suppressing the artifact and preventing

the saturation of the amplifier. In this region, the SNR degradation can be attributed to the increased noise and distortion introduced by the cancellation CDAC. All these measurements were performed under the challenging scenario of exact alignment of the artifact with the signal. As discussed earlier, in the current implementation, the cancellation filter cannot capture and cancel the common-mode artifact. The only suppression that occurs is the capacitive division at the LNA input. Common-mode artifacts larger than 100 mV_{pp} degrades both the gain and SNR. Any CM stimulation artifact converted to a differential mode due the low CMRR of the front-end, will be automatically included in the pattern stored for the residual artifact in the back-end during the acquisition of the residual artifact [Φ_{acq1} in Fig. 14(c)]. During the acquisition phase, this stored waveform, which includes both the residual differential artifact and the CM-to-differential converted component of the stimulation artifact, is subtracted from the recorded signal and cancels the CM-to-differential converted artifact.

In a closed-loop neural interface, recording an evoked potential is critical since it carries information about the response of the neuronal network to the stimulation pulse. An evoked neural response can occur as early as 1 ms following the stimulus [52]. Therefore, it becomes critical for the front-end amplifier to recover from saturation and restore its linearity soon after the stimulation phase. To investigate the canceler's performance in such scenarios, a 2.5 V_{pp} artifact was emulated (30 μA stimulation current delivered to a 41 kΩ resistor) and applied to the recording channel inputs in a single-ended configuration. The acquired waveform at the ADC output and the recovered signals are shown in Fig. 17(a–b). It can be observed that the amplifier recovery from saturation happens almost two times faster when the canceler is active. Fourier transform of sliding time windows of the recovered signals also suggest that during window B, the amplifier is still recovering from a deep saturation state in the absence of the front-end cancellation [Fig. 17(c)]. In the same time window, the canceler has recovered both the effective gain and SNR, as shown in Fig. 17(d–e). This suggests that if a neural spike happens just after the stimulation signal, without the front-end cancellation, it can go undetected.

The dependence of the IIR filter coefficients on different stimulation parameters was also studied using the test bench in Fig. 14(a). Fig. 18(a) shows a linear relationship between the adapted filter coefficients and the artifact amplitude, as is suggested by (13). On the other hand, the coefficients have no significant dependence on the stimulation current duty cycle and pulse width, as can be observed in Fig. 18(b)–(c). Since the IIR filter is based upon the empirical model in (1), it resembles an LTI RC network and is therefore independent of the timing properties of the applied balanced biphasic stimulation signal.

2) Dual Channel Stimulation: In a high-density neural interface platform, concurrent multi-channel neural stimulation is inevitable in order to investigate how neuronal populations respond to timing differences of such stimuli and map the brain networks in more detail [53]. The past implementations of the adaptive-filter techniques for artifact mitigation [42], [43] were designed to train the filter coefficients to only 1 independent stimulation channel. To demonstrate cancellation of an artifact due to the simultaneous operation of independent stimulation channels, the 2 on-chip stimulators were activated and programmed in such a way that their output currents overlap in time. Stimulator 1 was

connected to an RC load and stimulator 2 was tied to a resistive load. The 2 artifacts and a sinusoidal signal were summed off-chip, and were applied to all the 8 recording inputs as shown in Fig. 19. The stimulation currents (I_{stim1}=19 μA and I_{stim2}=10 μA, with 330 μs pulse width) and the resultant artifact are shown in Fig. 20(a). The recovered signal and its Fourier transform are shown in Fig. 20(b) and (c) respectively. The effective gain increased by more than 10 dB when the front-end canceler was activated, suggesting that the canceler was able to keep the AFE in its linear region of operation. Fig. 20(d) shows the effective gain and SNR for the 8 recording channels. The average effective gain was boosted from 18.1 to 27.6 dB. The SNR was also improved from −3.8 to 5.0 dB in average.

3) In Vitro Measurements: Fig. 21 shows the *in vitro* measurement setup for testing the performance of the artifact canceler in 1x phosphate-buffered saline (PBS), which can mimic the brain tissue electrical properties. A metallic wire with <1 mm exposed tip was inserted in the solution for injecting the desired signal into the solution (a single tone at 3.05 kHz in the first experiment and a pre-recorded neural waveform in the second experiment). The solution was biased to V_{CMST} via another piece of wire with a few cm of exposed tip. Two sets of flexible parylene-based micro-electrode arrays (MEA) with platinum disc electrodes [47], [54], [55] were used to interface the 8 recording channels with the solution. The microelectrodes had different exposed diameters ranging from 30 to 160 μm. A biphasic 35 μA stimulation current with 330 μs pulse width was injected into the solution via the largest electrode (diameter=210 μm). The artifact waveforms received at different electrodes are shown in Fig. 22(a). A counter-intuitive observation is that channel 0, which is farther away from the stimulation electrode compared to channel 2, experiences a larger artifact. This suggests that, as we mentioned earlier, the artifact coupling mechanisms and pathways are not limited to the solution and tissue itself, but they may arise from the hardware and device properties. The recovered signal and their corresponding frequency spectrum are also shown in Fig. 22(a). For channels 0 and 1 which experience the largest artifacts, the cancellation scheme recovered the underlying signal, with 10 dB improvements in both gain and SNR, as shown in Fig. 22(b–c). As the amplitude of the artifact reduces below 10 mV_{pp}, which is the case for channels 3–7, the amplifier is not saturated with the artifact and the cancellation circuitry has negligible effect on the system performance.

Finally, pre-recorded neural spikes were generated and injected into the solution, without changing the existing test bench. Therefore, the artifact waveforms are the same as those shown in Fig. 22(a). The output of the function generator and the overlapping stimulation current is shown in Fig. 23(a). Similar to the single-tone experiment, for channels 0 and 1 the neural signal is lost due to the amplifier saturation, as shown in Fig. 23(b). However, the cancellation filter can recover the neural spike in these channels, which experience the largest artifact levels (up to a 900 mV_{pp} artifact).

Table I compares the performance of the chip with the state-of-the-art bidirectional neural interfaces. Since the performance of the artifact cancellation depends on a diverse set of experimental conditions such as the stimulation parameters (current intensity, pulse duration and frequency, charge balancing, etc), the electrode impedance, hardware setup and the time window that the spectral analysis is performed, it may be hard to provide a fair comparison between different architectures solely based on their maximum peak-to-peak

artifact level handling. Nonetheless, with the presented measurement setup and conditions, the implemented SoC suppresses stimulation artifacts with amplitudes measured up to 700 mV_{pp}, while maintaining competitive noise and power performance. About half of the area of the recording channels is occupied with the digital circuitry, which is all designed and laid out manually. Implementation in a more advanced node and utilizing an automated logic synthesis tool can significantly shrink the area of the digital blocks and routing. Moreover, for an area-optimized design, multiplexing ADCs between channels should be considered. In fact, it may be possible to integrate the cancellation technique discussed here in a fully digital front-end, following the trends suggested in [56]. The 2-tap IIR filter implementation demonstrated in this work can potentially reduce the silicon area needed for storing the filter coefficients, compared to an FIR implementation with 30 or more taps. In a scaled-up system with N recording and M stimulation channels, the proposed scheme requires storing $2MN$ IIR digital coefficients, which can be conveniently accommodated by the technology scaling. All the recording channels can be trained simultaneously with respect to each stimulation channel, which adds up to a total training time of $\frac{MI_{stim}R_m}{f_{stim}(10\frac{mV}{cycle})}$, where f_{stim} is the repetition frequency of the stimulation current waveform (cycles/s), R_m is the series resistance in the empirical model in Fig. 3(a), and I_{stim} is the stimulation current. If the stimulation artifact shows an LTI response in the target *in vivo* environment [41], the coefficients can be trained with a scaled-down stimulation current to prevent an undesirable neural response. Moreover, the decreased stimulation intensity carries an additional advantage of reducing the training time. During the learning phase, the frequency of the stimulation signal can also be increased to further shorten the training time. During the acquisition phase, the coefficients should be linearly scaled up with the same ratio as the stimulation currents are scaled [Fig. 18(a)], and the stimulation pattern can be tuned to the desired duty cycle and pulse duration without the need to retrain the filter coefficients [Fig. 18(b)–(c)]. This was verified experimentally in the same *in vitro* setup as before (Fig. 21) but with a larger ground electrode. The recording channels were initially trained to a stimulation current of 20 μA with a pulse width of 100 μs applied at a rate of 1.22 kHz. In the acquisition phase, the stimulation current was doubled to 40 μA, while the pulse width and frequency were tuned to 400 μs and 152 Hz respectively, as demonstrated in Fig. 24(a). To test the scalability of the canceler as was discussed before, the trained coefficients were multiplied by 2 and the performance of the artifact cancellation to recover a single-tone signal was measured [Fig. 24(b)–(c)]. The response of the canceler directly trained to the scaled-up current was also measured for comparison. Comparing the gain and SNR of the recovered signal in Fig. 24(d) shows that a linear scaling of the filter coefficients is sufficient to cancel the artifact generated by a stimulation current with different amplitude, pulse duration and duty cycle. This suggests that the stimulation parameters can be tuned on-the-fly without the need to retrain the filter coefficients of the canceler.

VI. Conclusion

A multi-channel bidirectional neural interface with an adaptive stimulation artifact canceler was implemented in a 180-nm CMOS process. The fabricated SoC demonstrated a 2-tap IIR filter, which was trained with a sign-sign LMS algorithm and could extend the dynamic

range of the existing neural recording front-ends by accommodating stimulation artifacts up to 700 mV_{pp} while retaining competitive noise and power performance. The canceler could also reduce the recovery time of a saturated front-end amplifier from a 2.5 V_{pp} artifact by a factor of 2, which allows for the detection of a fast evoked potential. The implemented front-end canceler could mitigate up to 2 concurrent and independent stimulation artifacts appearing on all the 8 recording channels. The IIR implementation of the active filter significantly reduced the required number of filter coefficients compared to an FIR filter, which in a high-density neural interface, can potentially lead to a substantial decrease in the computational power consumption and chip area for local storage of the filter coefficients. Moreover, the IIR filter coefficients are independent of the timing properties of the stimulation current, while they scale linearly with the stimulation amplitude. This allows for the on-the-fly tuning of the stimulation waveform without the need to retrain the filter coefficients.

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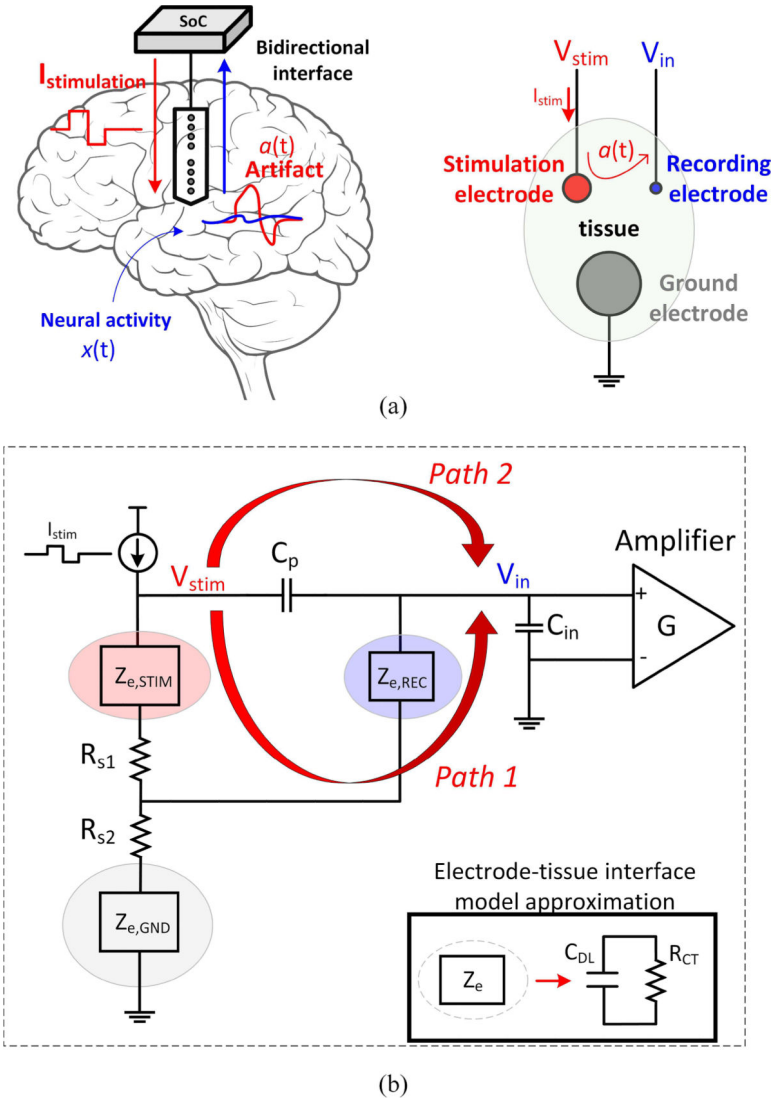


Fig. 1.

(a) Conceptual diagram of a bidirectional neural interface and the source of stimulation artifact. (b) A simplified diagram of artifact coupling to to amplifier input (REC: recording, STIM: stimulation, GND: ground).

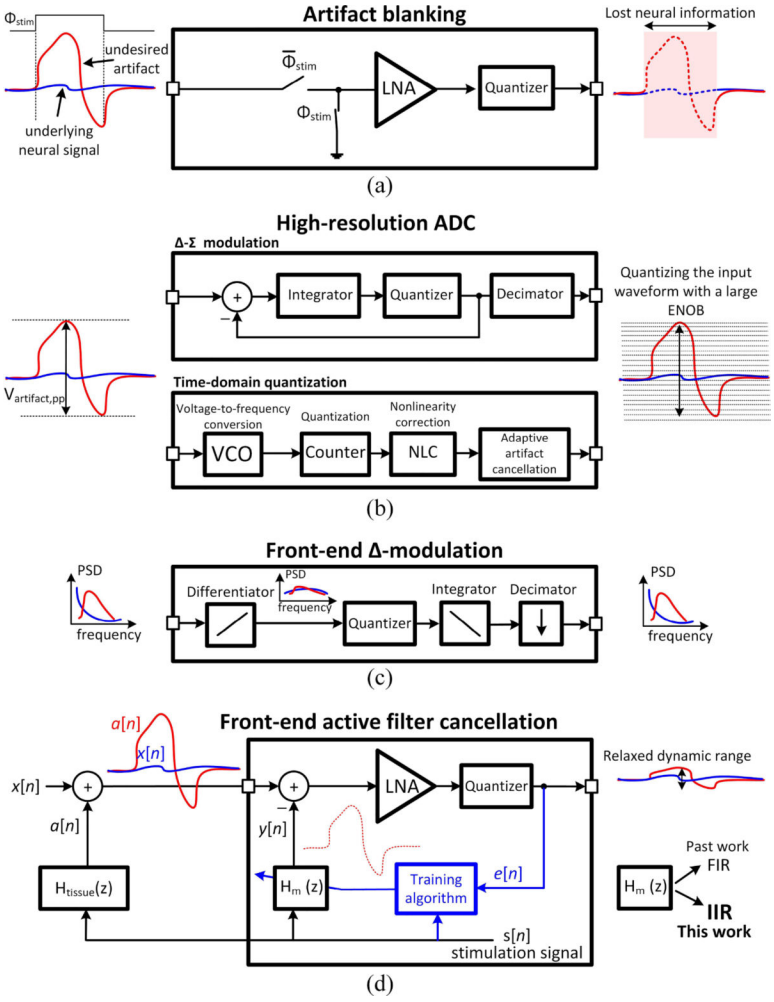
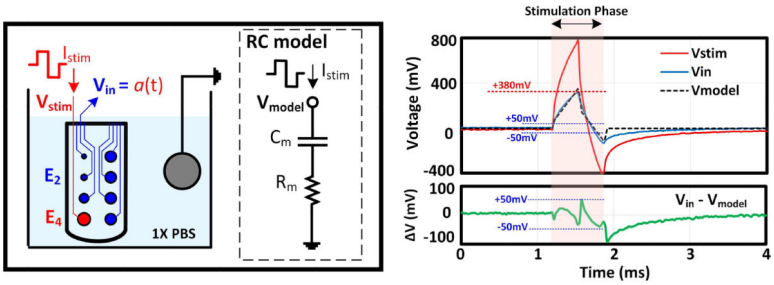


Fig. 2.

Stimulation artifact front-end mitigation techniques. (a) Artifact blanking. (b) High resolution ADCs. (c) Delta-modulated front-ends. (d) Front-end adaptive filters.



Fitted RC parameters

Parameter	Estimated value
C_m	34 nF
R_m	2.4 kΩ

(c)

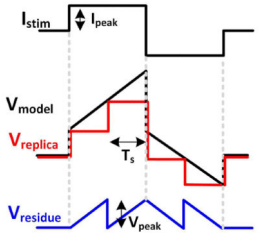
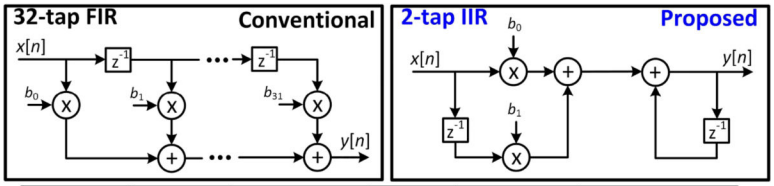


Fig. 3.

(a) Artifact measurement test bench and proposed RC model. (b) RC model output displayed with the measured stimulation and artifact voltages. (c) Fitted RC model parameters. (d) Stimulation artifact waveform and filter response.



Specification	# filter taps	# delay elements	# adders	# multipliers	# operations/cycle
FIR	32	31	31	32	63
IIR	2	2	2	2	4

Fig. 4.
Block diagram and comparison of the FIR and IIR cancellation filters.

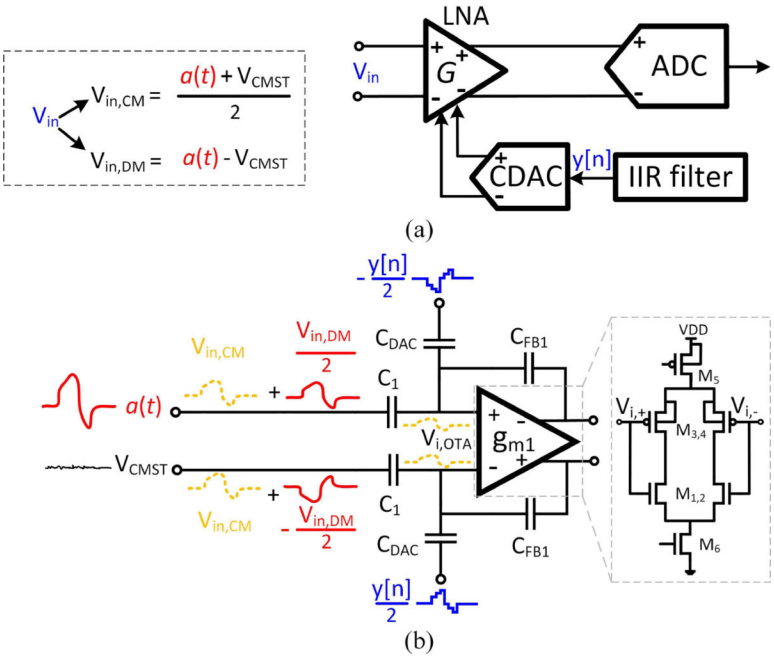


Fig. 5.

(a) Simplified block diagram of the front-end configuration. (b) Differential-mode artifact cancellation at the LNA input and common-mode limitation (V_{CMST}: body bias voltage).

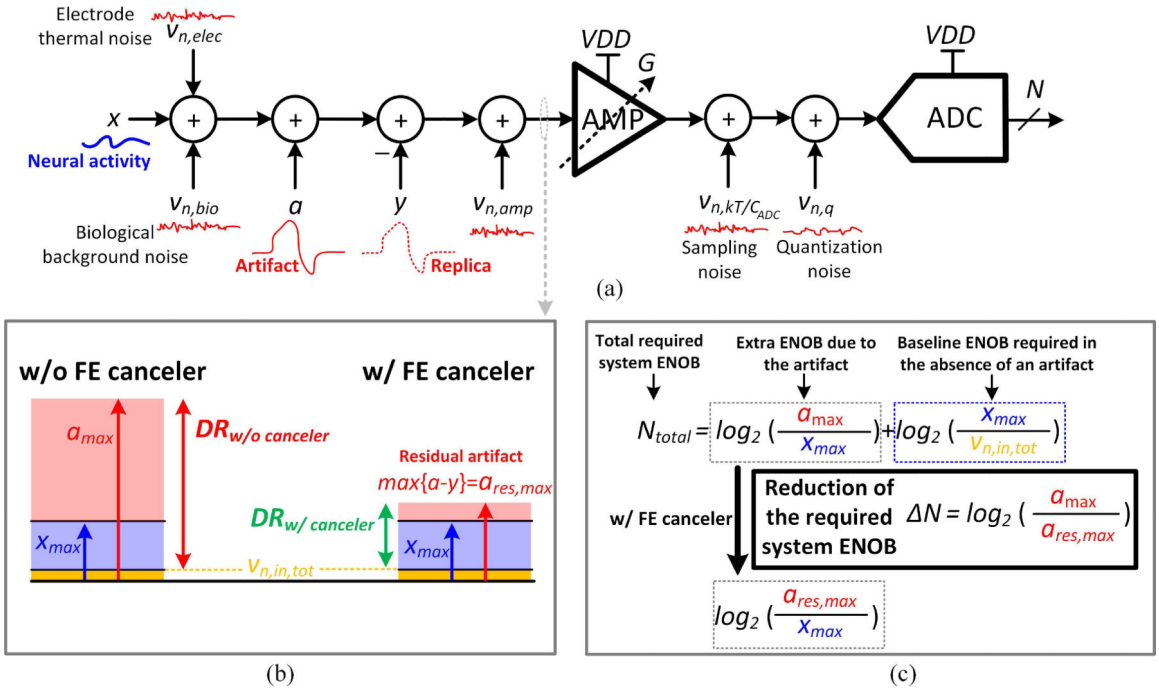


Fig. 6.

Noise and dynamic range analysis. (a) Signal flow diagram of the artifact, desired signal and noise. (b) Effect of the front-end (FE) cancellation on the dynamic range (DR). (c) Required DR for the recording system.

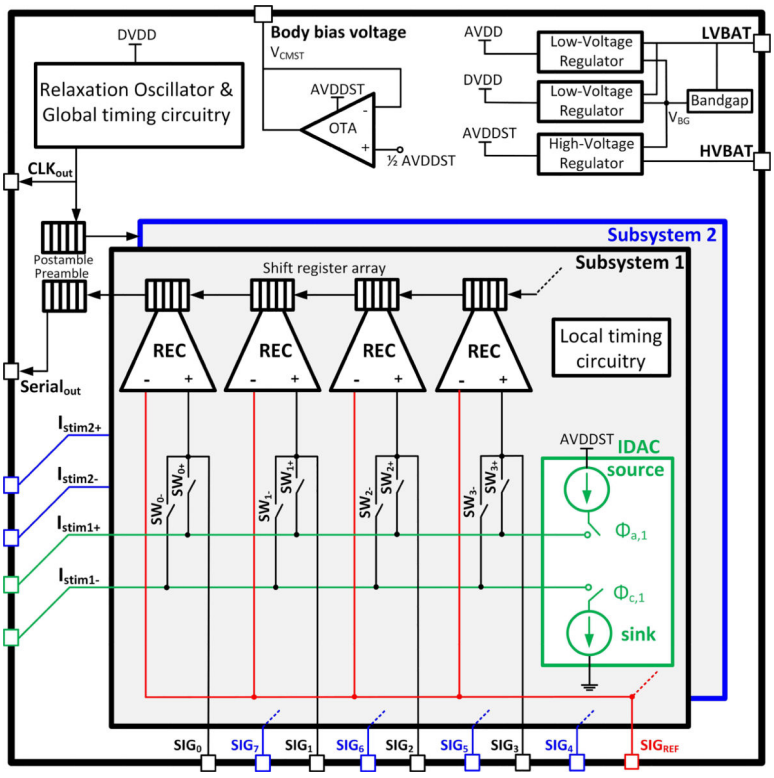


Fig. 7.
Neural interface SoC block diagram.

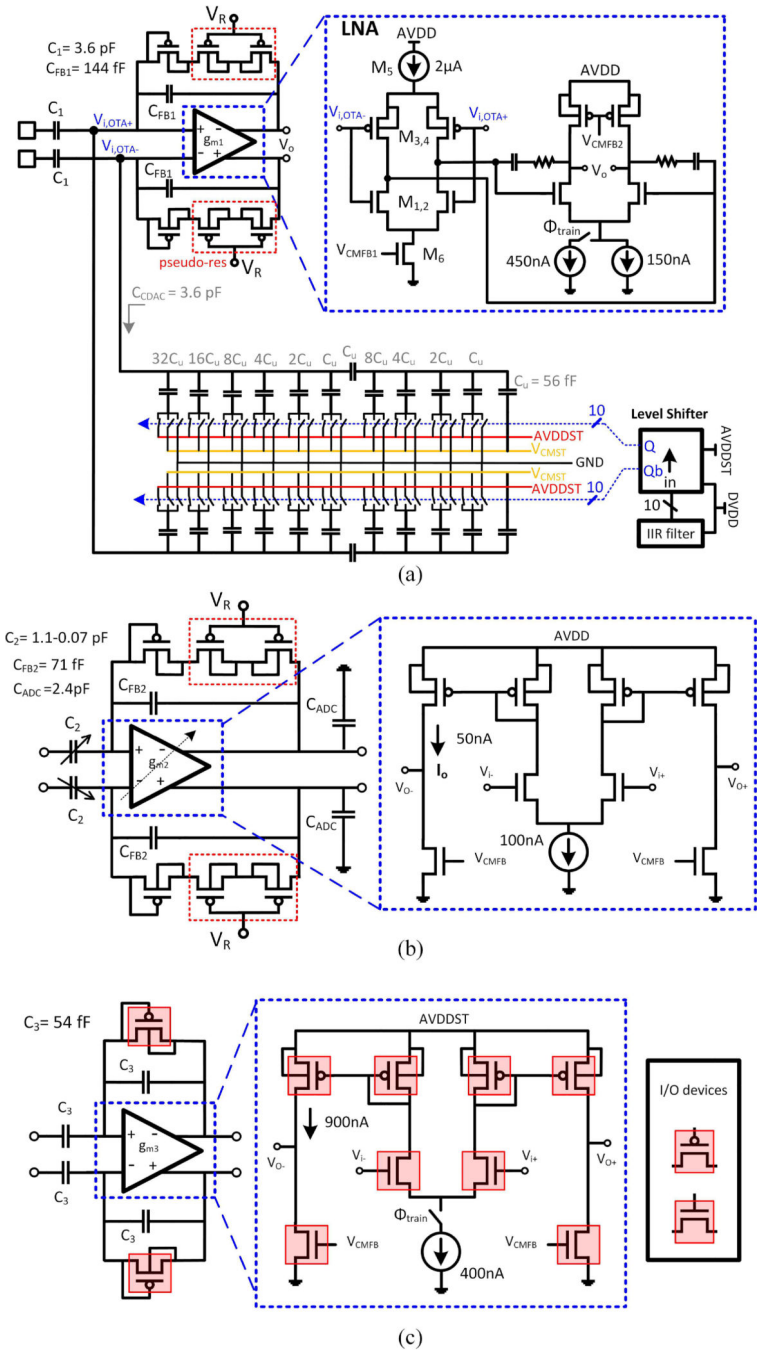


Fig. 8.
Detailed circuitry of the AFE. (a) LNA and CDAC configuration (b) PGA (c) ADC driver.

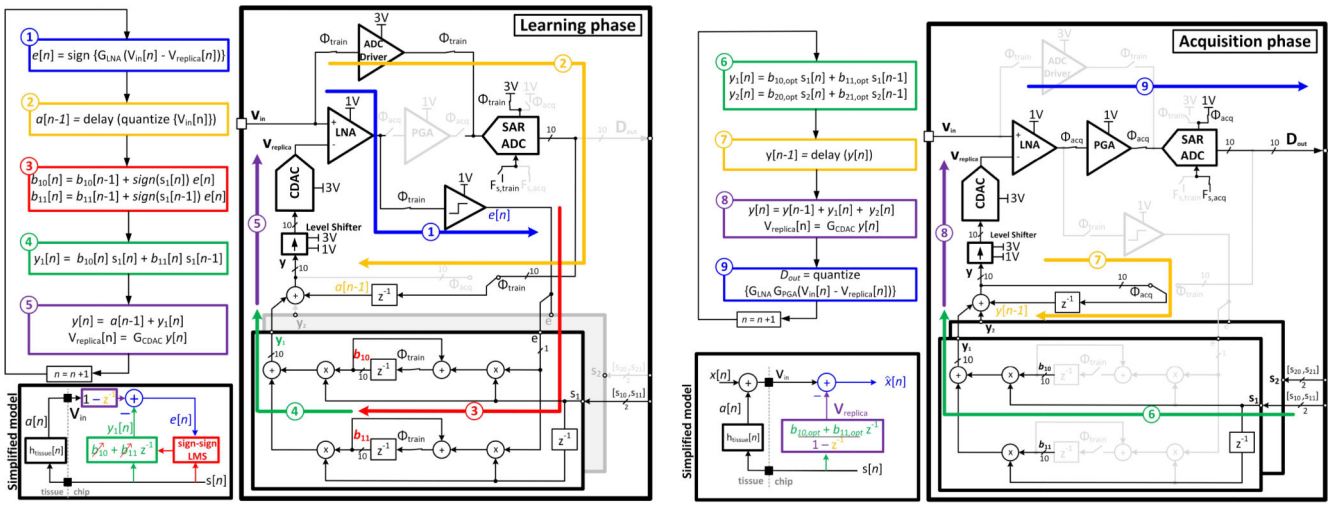


Fig. 9.

Front-end IIR LMS filter principle of operation. (a) Learning phase. (b) Acquisition phase. The disabled blocks are shown in a light gray color.

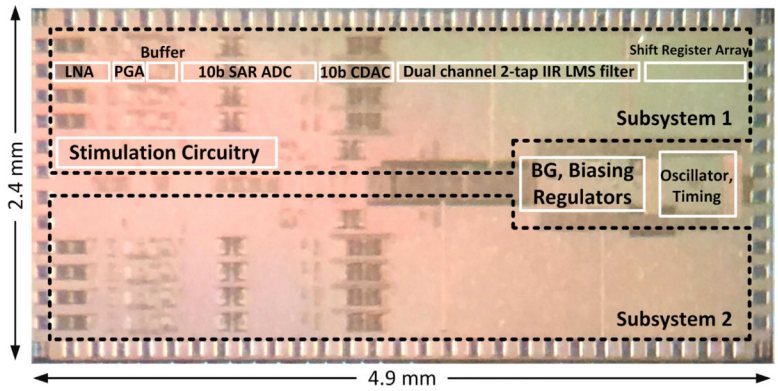


Fig. 10.
Die microphotograph.

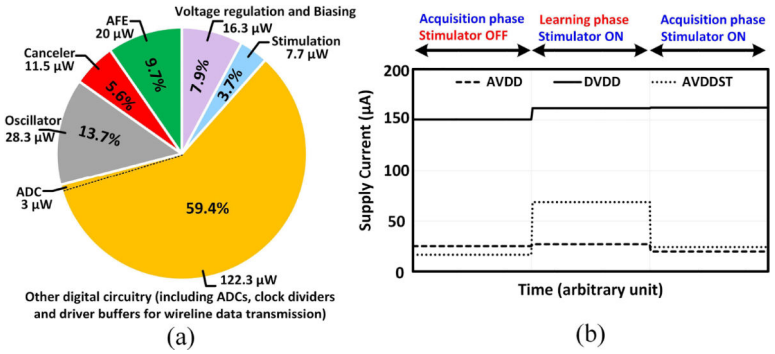


Fig. 11.

(a) Chip total power consumption breakdown. (b) Supply voltage currents in different operation modes.

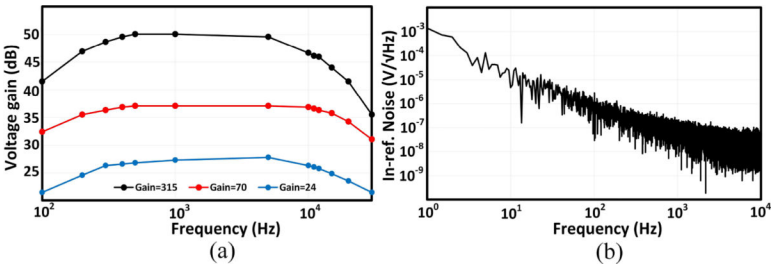


Fig. 12.

(a) AFE frequency response. (b) AFE input-referred noise for the maximum gain setting.

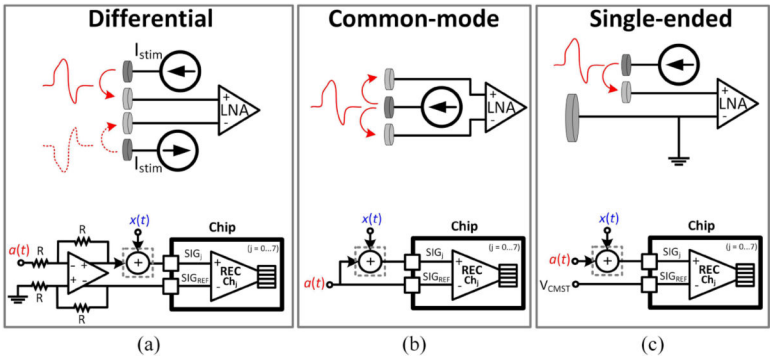


Fig. 13.

Different modes of stimulation artifact coupling into the amplifier input (a) Differential (b) Common-mode (c) Single-ended. The off-chip circuitry that generates each mode is also included.

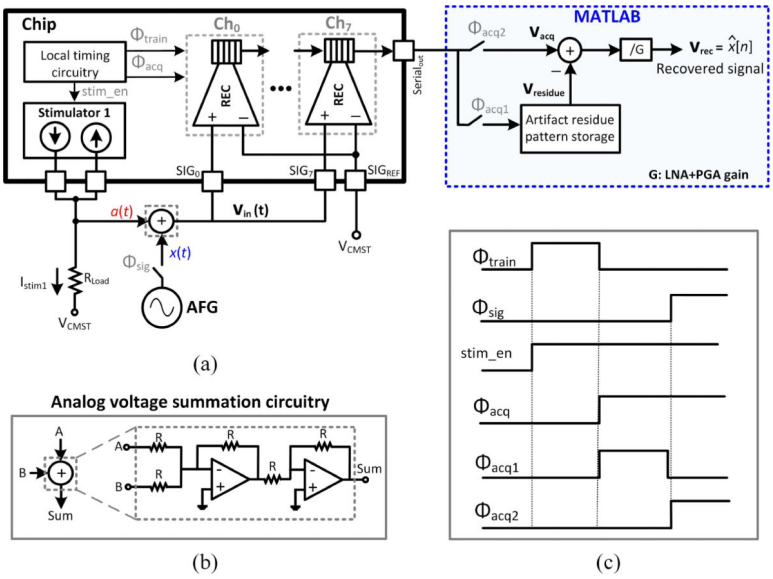


Fig. 14.

(a) Measurement setup for testing the performance of the artifact canceler. (b) Off-chip voltage summation circuitry. (c) Timing diagram of the successive operation cycles and phases.

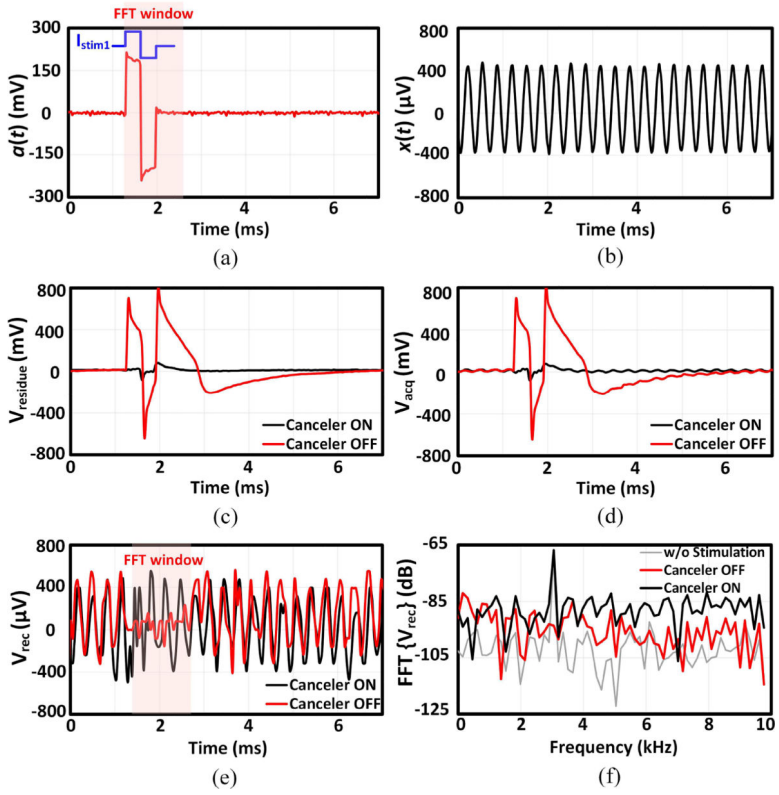


Fig. 15.

(a) Stimulation artifact. (b) Single-tone input signal. (c) Residual artifact waveform recorded during Φ_{acq1}. (d) Recorded signal contaminated with the residual artifact during Φ_{acq2}. (e) The recovered amplified input signal (The time window that the FFT is performed on is shown with a red rectangle). (f) Frequency spectrum of the recovered signal. The FFT of the recorded signal in the absence of the stimulation signal is also plotted. The representative waveforms are shown for channel 0.

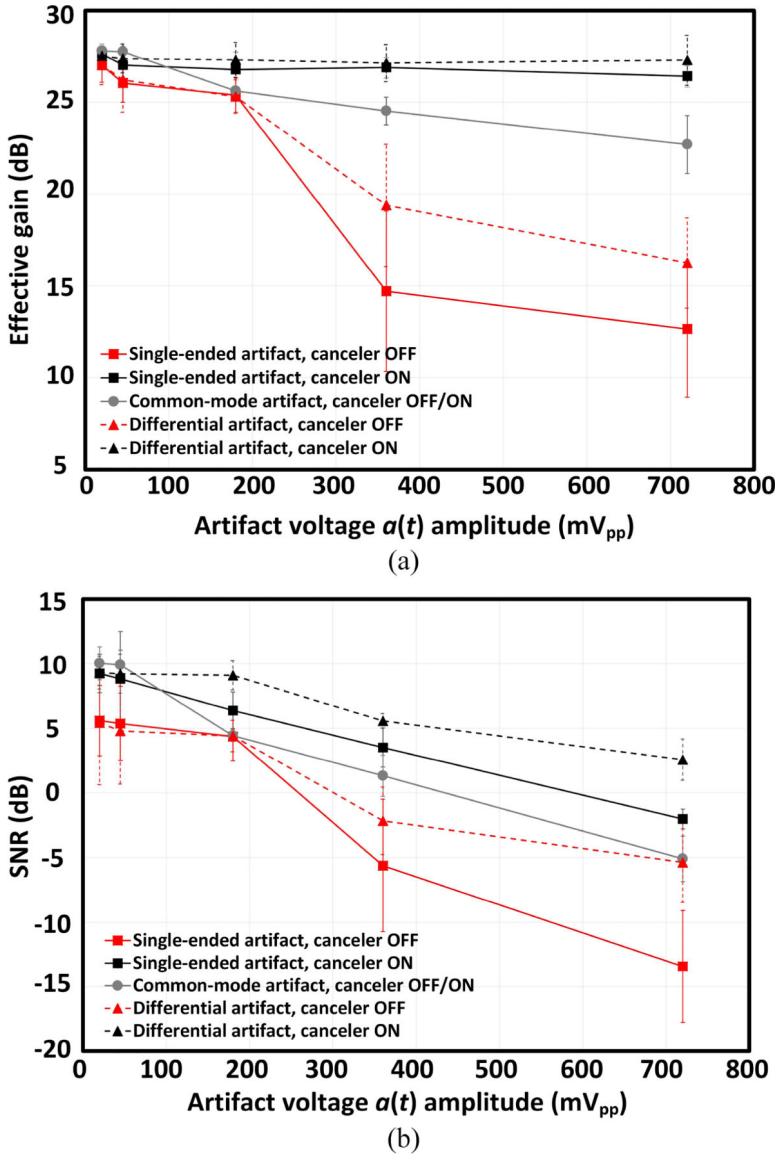


Fig. 16.

(a) Effective gain and (b) SNR as a function of the input artifact peak-to-peak voltage, measured for single-ended, differential and common-mode artifact waveforms. The error-bars show $\pm 1\sigma$ variation across the 8 recording channels.

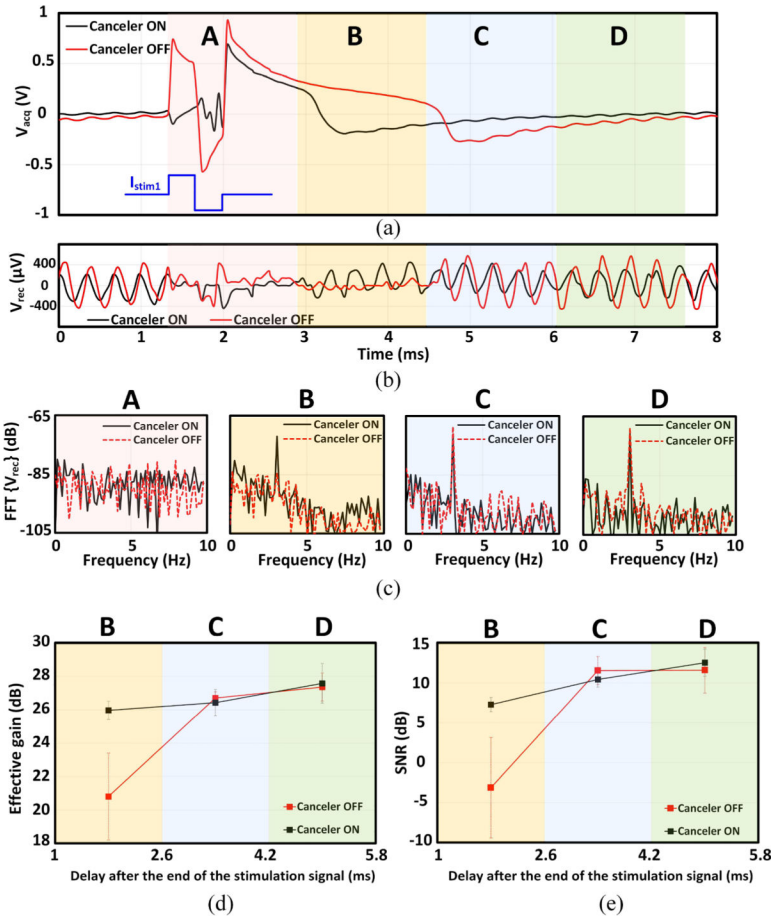


Fig. 17.

Effect of the canceler on the amplifier recovery time from saturation due to a 2.5 V_{pp} artifact (a) Recorded signal contaminated with the residual artifact (Sliding time windows are labeled as A-D). (b) Recovered signal. (c) Frequency spectrum of the recovered signal in different time windows. (d) Effective gain and (e) SNR measured in different time windows following the stimulation event.

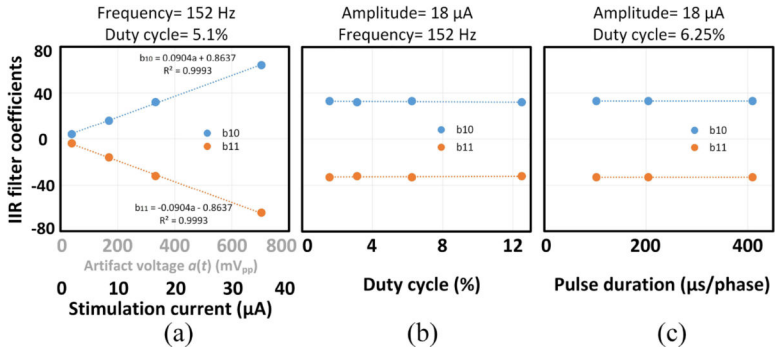


Fig. 18.

Dependence of the IIR filter coefficients on the stimulation signal parameters. (a) Amplitude (b) Duty cycle (c) Pulse width.

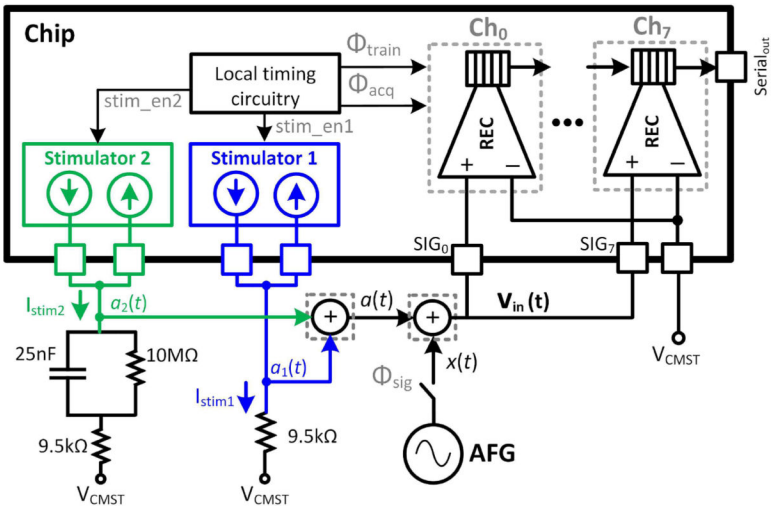


Fig. 19.

Test bench for measuring the cancellation performance in the presence of 2 overlapping stimulation signals.

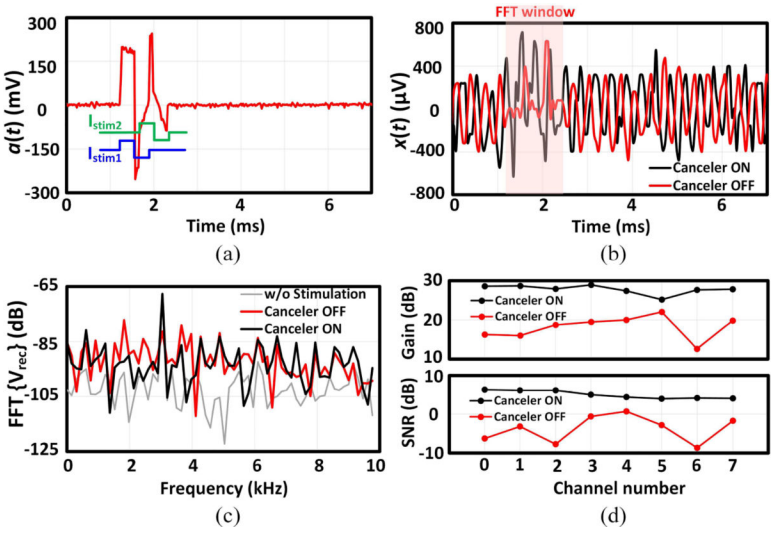


Fig. 20.

(a) Stimulation currents shown on top of the resultant artifact waveform. (b) The recovered amplified input signal (shown for channel 0). (c) Frequency spectrum of the recovered signal. (d) Effective gain and SNR measurement of the recovered signal across different channels.

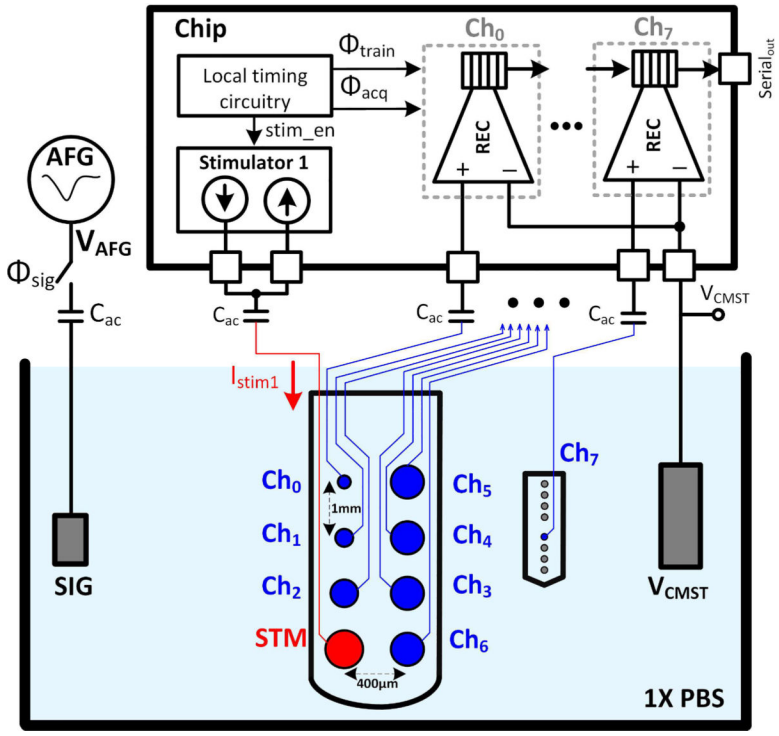


Fig. 21.

In vitro measurement setup for testing the performance of the artifact canceler in 1x PBS. The ac-coupling capacitance C_{ac}= 220nF prevents any DC leakage current through the electrodes, which can potentially deteriorate the electrode performance or even result in its failure. 2 microelectrode arrays were used in this testbench to investigate the artifact coupling in different configurations.

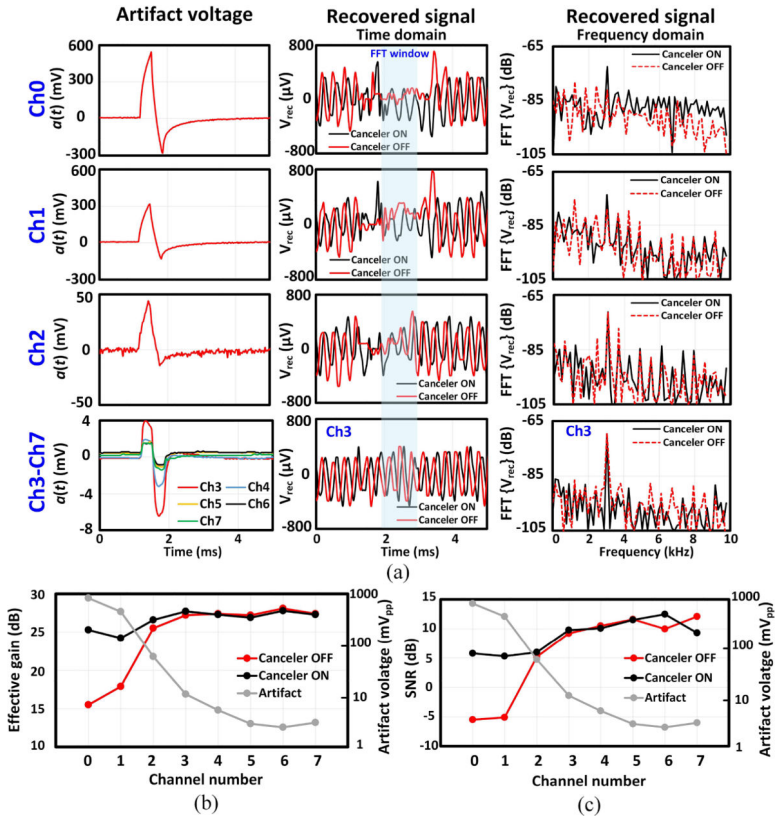


Fig. 22.

Performance of the canceler on a single-tone signal *in vitro*. (a) Stimulation artifact waveform, recovered signal and its frequency spectrum cross different channels. (b) Effective gain and (c) SNR across different channels. The input artifact amplitude is also shown for each electrode.

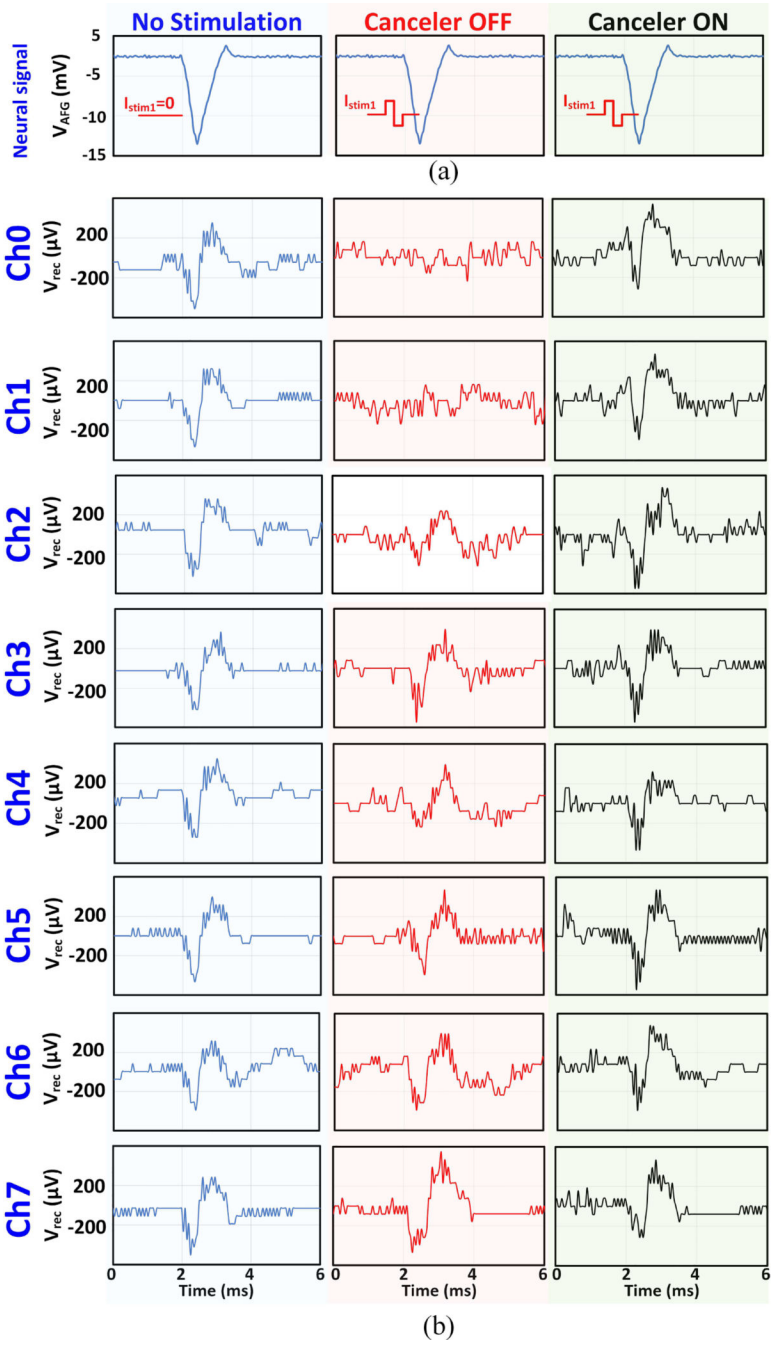
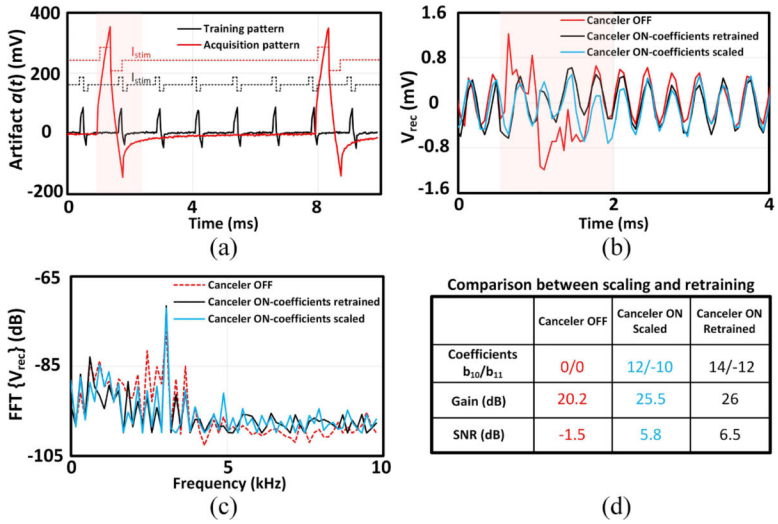


Fig. 23.

Performance of the canceler on a pre-recorded neural signal *in vitro*. (a) The neural signal generated by a function generator. The timing of the stimulation current is also shown. (b) Recovered signal across different channels in 3 conditions: stimulation OFF, stimulation ON + canceler OFF, stimulation ON + canceler ON. The test bench and the artifact levels are the same as the *in vitro* single-tone test.



	Canceler OFF	Canceler ON Scaled	Canceler ON Retrained
Coefficients b_{10}/b_{11}	0/0	12/-10	14/-12
Gain (dB)	20.2	25.5	26
SNR (dB)	-1.5	5.8	6.5

Fig. 24.

Scalability of the IIR filter output in response to stimulation with different parameters *in vitro*. (a) Stimulation current and artifact during training and acquisition. (b) Recovered signal in 3 conditions: canceler OFF, canceler ON + filter retraining, canceler ON + coefficient scaling. The FFT window is highlighted with a shadow. (c) Frequency spectrum of the recovered signal. (d) Performance summary of the artifact cancellation scheme. The representative plots are from channel 0.

TABLE I

Performance Summary and Comparison with the State-of-the-art Bidirectional Neural Interfaces

	This work	**[28] VLSI' 17**	**[39] JSSC' 20**	**[42] SSCL' 18**	**[43] JSSC' 16**	**[32] TBCAS' 18**	**[17] VLSI' 16**	**[38] VLSI' 17**	**[24] JSSC" 6**	**[15] JSSC' 18**
Technology (nm)	**180**	180 HV	130	65	180	40/HV 180[a]	180	65	180	130
Supply voltage (V)	**1, 3**	1, 3~12	0.6, 1.2, 3.3	1	-	0.6, 1.2, 1.8, ±5	0.8, 3.3	0.5, 2.5	1.8, 2, 3~12	1.2, 3.3
IRN[b] (μV_{rms})	**6.2**[c]/**11**[d,e]	1.6	1.6	7.5[c]/8.2[d]	3.05	2.2	5.9[f]	2.78	2.09	12.0
Signal BW (Hz)	**200**[g]**-9k**	DC-500	1–500	10–8.3k	1–2k	1–250	17–1.65k	1–1k	0.59–117	0.5–10k
Voltage gain (dB)	**27.6–50.0**	NA	NA	45–65	40–60	NA	42	NA	50–70	6–69.5
ADC res./ENOB(b)	**10/8.6**	15/10.2	12/11.3	10/-	10/-	NA/12.8	8/-	14/-	10/7.8[i]	10/-
THD[j]	**0.9%** **2mV$_{pp,in}$** **1kHz 50dB**	0.7% 0–1V$_{pp,in}$ 60Hz	-	0.4% 1.2mV$_{pp,in}$ 1kHz 65dB	-	0.009[k]% 0–1V$_{pp,in}$ 203Hz	-	-	0.4[i]% 8.9mV$_{pp,in}$ 97Hz 50dB	0.89% 20mV$_{pp,in}$ 10kHz 54dB
AFE power/Ch(μW)	**2.5**	NA	NA	1.8	0.24	NA	0.8	2.98[i]	3.75	25.2
ADC power/Ch(μW)	**0.38**	8.0	1.7	-	0.09	8.2	-	-	-	0.88
Canc. power/Ch(μW)	**1.42**	NA	NA	0.9	-	NA	NA	-	NA	NA
Rec. area/Ch (mm^2)	**0.66**	-	0.023	0.18	0.17	0.12	0.04	0.15	0.56	0.1[h]
# Rec front-ends / Stimulation cores	**8 / 2**	64 / 4	32 / 32	64 / 2	8 / 4	32 / 8	16 / 1	1	16 / 16	1024 / 64
# Artifact cancelers	**8**	0	0	8	8	4	0	1	0	0
Artifact cancellation method	**FE filter**	NA	NA	FE filter	FE filter	BE filter	NA	FE template subtraction	-	-
# Filter taps, type and learning algorithm	**2, IIR, sign-sign LMS**	NA	NA	32, FIR, sign-sign LMS	8, FIR, sign-sign LMS	16, FIR, normalized LMS	NA	NA	NA	NA
Max # uncorrelated stimulation artifacts mitigated by each canceler	**2**	NA	NA	1	1	1	NA	1	NA	NA
Die size (mm^2)	**11.76**	11.52	1.0[h,l]	5.14	1.74[l]	9.88/16.43[a]	1.1[l]	-	25.0	192[m]

AFE: LNA+PGA, FE: front-end, BE: back-end

IEEE J Solid-State Circuits. Author manuscript; available in PMC 2022 July 01.

NA: Not applicable

-: Not reported

[a] Separate neural recording and stimulation chips in different technologies were fabricated.

[b] Integrated input referred noise measured for the reported bandwidth.

[c] Standalone AFE w/o the front-end CDAC.

[d] w/ the front-end CDAC.

[e] AFE (max gain setting)+ADC quantization noise.

[f] Measured for 10Hz-10kHz.

[g] The high-pass corner was limited because the pseudo-resistors in the amplifier had to be shorted to prevent any disruption in the biasing due to the substrate DC leakage currents.

[h] Estimated.

[i] AFE+ADC.

[j] THD measured for the given single-tone input amplitude, frequency and AFE gain.

[k] Reported HD3, the design uses a nonlinearity correction block.

[l] Active area (excluding pads).

[m] Includes 16k electrode sites and active pixels.