Flexible complementary circuits operating at sub-0.5 V via hybrid organic–inorganic electrolyte-gated transistors

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Electrolyte-gated transistors (EGTs) hold great promise for next-generation printed logic circuitry, biocompatible integrated sensors, and neuromorphic devices. However, EGT-based complementary circuits with high voltage gain and ultralow driving voltage (<0.5 V) are currently unrealized, because achieving balanced electrical output for both the p- and n-type EGT components has not been possible with current materials. Here we report high-performance EGT complementary circuits containing p-type organic electrochemical transistors (OECTs) fabricated with an ion-permeable organic semiconducting polymer (DPP-g2T) and an n-type electrical double-layer transistor (EDLT) fabricated with an ion-impermeable inorganic indium–gallium–zinc oxide (IGZO) semiconductor. Adjusting the IGZO composition enables tunable EDLT output which, for In:Ga:Zn = 10:1:1 at%, balances that of the DPP-g2T OECT. The resulting hybrid electrolyte-gated inverter (HCIN) achieves ultrahigh voltage gains (>110) under a supply voltage of only 0.7 V. Furthermore, NAND and NOR logic circuits on both rigid and flexible substrates are realized, enabling not only excellent logic response with driving voltages as low as 0.2 V but also impressive mechanical flexibility down to 1-mm bending radii. Finally, the HCIN was applied in electrooculographic (EOG) signal monitoring for recording eye movement, which is critical for the development of wearable medical sensors and also interfaces for human–computer interaction; the high voltage amplification of the present HCIN enables EOG signal amplification and monitoring in which a small ∼1.5 mV signal is amplified to ∼30 mV.

electrolyte-gated transistor | complementary circuit | flexible electronics | EOG sensing

Electrolyte-gated transistor(EGT) microelectronics offer great promise, taking advantage of low power consumption, mechanical flexibility, and excellent biocompatibility. They are envisioned to play a major role in the future development of the flexible electronics, medical applications in clinical diagnostics/therapeutics, and electronic skins (1–6). To fully take advantage of the potential of EGTs for signal amplification in applications enabled by unique ionic–electronic interactions (7–10), integration into various logic gates and especially inverters, the basic building blocks of modern logic circuitry, is essential. To date, EGT-based circuits have mainly been constructed with unipolar inverters comprising either organic electrochemical transistors (OECTs) having an ion-permeable semiconducting polymer as the channel layer (11–13) or electrical double-layer transistors (EDLTs) based on ion-impermeable semiconductors (14–16). However, the vast majority of OECT organic (semi)conducting polymers for OECTs are hole-transporting (p-type), while electron-transporting (n-type) semiconducting polymers are sparse, typically unstable, and yield far lower performance than their p-type counterparts (17). In contrast, n-type oxide semiconductor mobilities as high as ∼100 cm^2/Vs are known, and indium–gallium–zinc oxide (IGZO) has been commercialized in displays and flexible electronics (18–20). This is not the situation with oxide p-type semiconductors (21, 22), where mobilities far lower than 10 cm^2/Vs are typical (23), and there are long-term stability issues (24, 25). Consequently, circuits based on both kinds of EGTs constructed with unipolar inverters and a resistor as load (26, 27) operated with constant power dissipation and low voltage gain (28, 29). Thus, the goal of complementary logic circuits for low power consumption and high voltage gain with sub-1 V driving voltage for bioelectronics, portable electronics applications, and low power dissipation had not been achieved with these materials (30, 31). Furthermore, devices with complementary circuits based on p- and n-type OECTs only delivered limited performance (voltage gain <11 for a driving voltage of 0.6 V) and required large device footprints for the n-type EGTs due to the mismatched transistor performance (11).

In this work, for the reasons cited above, we investigate integrating in a single device the intrinsically high performance of p-type OECTs with n-type oxide EDLTs. It will be seen that well-matched p- and n-type EGTs are realized, enabling their

Significance

Electrolyte-gated transistor (EGT)–based inverter circuits are the basic building blocks of next-generation flexible electronic devices. However, constructing high-performance complementary inverters is challenging due to the unbalanced electrical performances of available p- and n-type EGT semiconducting materials. Here we report high-performance EGT complementary inverters achieved by combining p-type organic electrochemical transistors based on an ion-permeable semiconducting organic polymer and n-type electric double-layer transistors based on an ion-impermeable metal oxide semiconductor. The resulting closely balanced complementary inverters achieve ultrahigh voltage gain (>110) under a low supply voltage of only 0.7 V and have been successfully used to achieve flexible logic circuits and sensitive electrophysiological signal amplification suitable for ophthalmologic diagnostics and measuring eye movement.

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integration into high-performance hybrid organic/inorganic complementary circuitry. Specifically, DPP-g2T (*SI Appendix*, Fig. S1) having a honeycomb film microstructure is adopted as the channel of the p-type OECT, while IGZO (In:Ga:Zn = 10:1:1 at %) acts as the channel material of an n-type EDLT. The resulting optimized hybrid inverters deliver a high voltage gain of more than 110 under driving voltage of only 0.7 V and static power consumption as low as 15 nW. Furthermore, successful construction of mechanically flexible NAND and NOR logic gates on both rigid and flexible substrates are demonstrated operating at a voltage as low as 0.2 V. Most importantly, real-time monitoring of human electrooculogram (EOG) signals is demonstrated using the present inverter exhibiting voltage amplification gain of ~20, which makes the inverter suitable for the development of wearable EOG sensors for medical research.

Results and Discussion

Hybrid Inverter Based on p-Type OECT and n-Type Oxide EDLT. The structure of the hybrid complementary inverter (HCIN) consisting of a p-type DPP-g2T OECT and an n-type IGZO EDLT is shown in Fig. 1*A*. Details of HCIN fabrication can be found in *Materials and Methods* and *SI Appendix*. Briefly, as illustrated in *SI Appendix*, Fig. S2, a spin-coated IGZO film was first patterned on a Si/SiO_2 substrate. Then, 50-nm Au electrodes with a 3-nm Cr adhesion layer were patterned with a lift-off process. Next, an SU-8 layer was patterned on the electrode while leaving the p- and n- type transistor channel area open; a porous DPP-g2T film prepared by the breath figure method (*SI Appendix*, Fig. S3) was then transferred on top of the p-type transistor channel area. Finally, an aqueous electrolyte (0.1 M KPF_6) and an Ag/AgCl gate electrode were applied. Note that the OECT DPP-g2T film has a porous morphology to enhance device performance by favoring ion intercalation in/extrusion from the semiconductor layer bulk. In contrast, in an EDLT the electrolyte ions remain at the interface with the semiconductor, and thus a smooth/dense IGZO semiconductor film morphology is optimal for maximizing this device's performance.

Before fabricating HCINs, the p- and n-type transistor characteristics were first evaluated individually and optimized to balance overall device performance. A representative transfer plot of the DPP-g2T OECT (channel length L = 10 μm; channel width W = 100 μm) is shown in Fig. 1*B*. Due to the porous DPP-g2T film morphology, minimal hysteresis (~0.05 V) and a large on/off current ratio (I_{on}/I_{off} = 10^5) are achieved. In contrast, OECTs based on dense DPP-g2T films of similar thickness (~100 nm) exhibit far larger hysteresis (~0.4 V) and a lower I_{on}/I_{off} of 10^3 (*SI Appendix*, Fig. S4). A peak transconductance ($g_{m,p}$) of 2.5 ± 0.8 mS is obtained for the porous DPP-g2T OECTs,

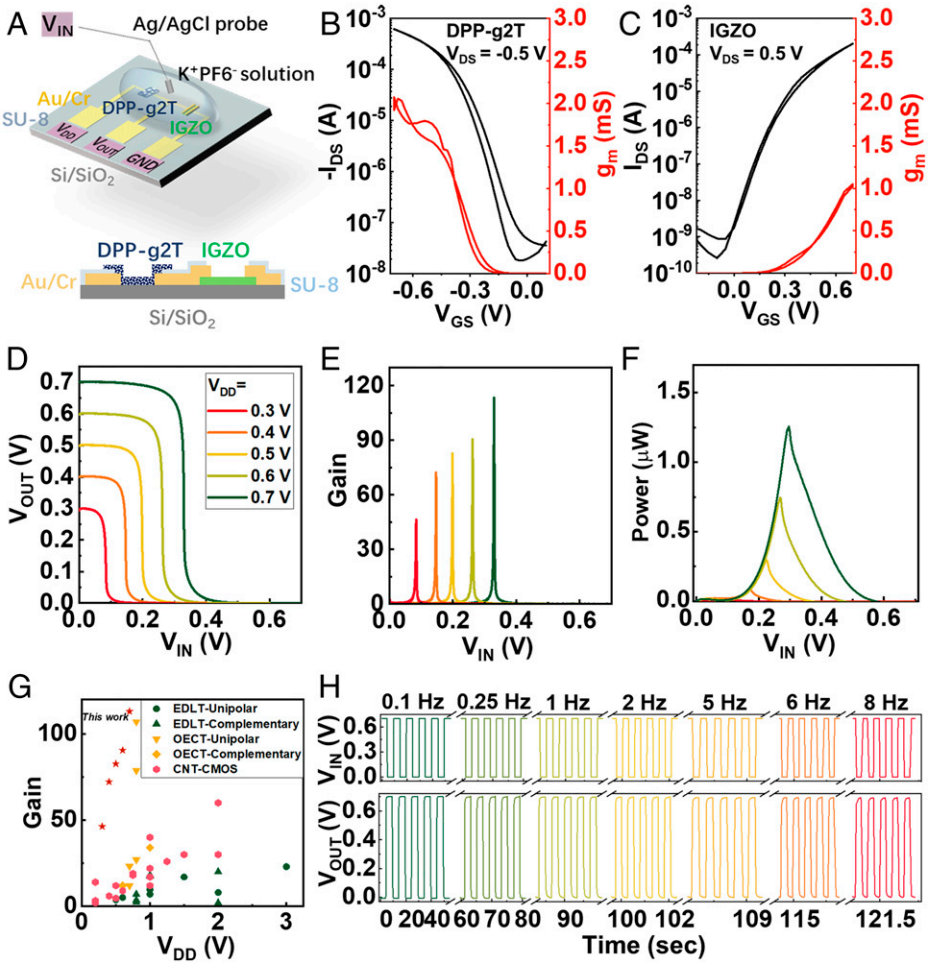

Fig. 1. Hybrid inverter design and performance. (*A*) Illustration of the hybrid inverter on rigid Si/SiO_2 substrate with top and cross-section views. Representative transfer and transconductance data for (*B*) p-type OECT and (*C*) IGZO EDLT. (*D*) Voltage transfer curves of the HCIN with V_{DD} from 0.3 to 0.7 V, and the corresponding (*E*) voltage gain and (*F*) power consumption. (*G*) Comparison of device voltage gain and V_{DD} of this work to literature EGT-based inverters (EDLT-based unipolar inverters, EDLT-based complementary inverters, OECT-based unipolar inverters, and OECT-based complementary inverters). (*H*) Dynamic performance of the HCIN with V_{DD} = 0.7 V over a frequency range from 0.1 Hz to 8 Hz.

which is ~250 times greater than that of the corresponding dense film-based devices (0.010 ± 0.006 mS) and comparable to that of other reported high-performance p-type OECTs (32). The enhanced OECT performance with porous DPP-g2T reflects greater wettability and surface area of the channel, which facilitates the ion diffusion from the electrolyte to the semiconductor bulk (33). Representative output curves of the OECT based on porous DPP-g2T (*SI Appendix*, Fig. S5) demonstrate distinct linear and saturation regions, indicating excellent charge injection from the source/drain electrodes (34).

To match the performance of the p-type OECTs, a series of IGZO EDLTs (L = 10 μm, W = 300 μm) with systematically varied In/Ga/Zn atomic ratios were fabricated and characterized. Previous research demonstrated that as the indium atomic ratio is increased, negatively shifted transfer curves and increased IGZO EDLT on-currents are observed, which is attributable to the increased electron concentrations and enhanced mobilities (35, 36). Thus, as the In/Ga/Zn atomic ratio is varied from 7:1:2 to 10:1:1 the on-current increases from 5.0×10^{-5} A to 8.9×10^{-4} A, and the turn-on voltage (V_{ON}) shifts from ~0.1 V to ~0.0 V. The optimal composition (In:Ga:Zn = 10:1:1) (Fig. 1*C* and *SI Appendix*, Fig. S6) affords a small turn-on voltage (V_{ON}) of ~0.0 V and a higher $g_{m,p}$ of ~0.6 mS. Note that the data presented in *SI Appendix*, Fig. S6 are based on unpatterned IGZO channels, which exhibit relatively high off-currents (I_{off}, 10^{-6}~10^{-5} A). However, upon patterning the IGZO and using SU-8 passivated source/drain electrodes, a substantially reduced I_{off} of only 10^{-9} A and a slightly enhanced $g_{m,p}$ of 1.2 ± 0.3 mS are realized (Fig. 1*C*). Note that the performance of the present IGZO-based EDLTs includes far larger g_m values than those of n-type OECTs with similar channel W/L ratios (37). For example, a recently reported high-performing n-type PgNaN OECT has a $g_{m,p}$ = 0.21 mS for W/L = 10 (38).

Benefiting from the more balanced p- and n-type EGT performance (V_{ON} ~0.0 V, I_{off} = 10^{-9}~10^{-8} A, I_{on} = 10^{-4}~10^{-3} A) in the same operational voltage range (< ±0.7 V; Fig. 1 *B* and *C* and *SI Appendix*, Figs. S5 and S7), the combined DPP-g2T OECT + IGZO EDLT is ideal for complementary inverters. Here the characteristic response curves (Fig. 1*D*) exhibit an ideal rail-to-rail voltage behavior with a switching voltage (V_{SW}) centered in a narrow range near V_{DD}/2 (for 0.3, 0.4, 0.5, 0.6, and 0.7 V V_{DD}, the V_{SW}s are 0.08, 0.15, 0.20, 0.26, and 0.33 V, respectively), due to the balanced p- and n-type EGT performance. Moreover, a voltage gain up to 113 is obtained with a V_{DD} = 0.7 V (Fig. 1*E*), which exceeds previously reported values for either unipolar or complementary inverter EGTs and carbon nanotube-metal oxide complementary metal–oxide–semiconductor circuits (Fig. 1*G*) (11, 15, 16, 28, 29, 39–56). Note that while the above unipolar OECT inverter reaches a voltage gain > 100 with V_{DD} = 0.8 V (46), the static power consumption, caused by the leakage current that exists when the inverter is not switching and on a steady state, is > 7×10^{-6} W, which is far higher than that of the present HCIN reported in Fig. 1*F*. Due to the low driving voltage of both EGTs, the HCIN has a very low static power consumption of only 2×10^{-9} W at V_{DD} = 0.3 V. Note that the static power consumption rises with increasing V_{DD} from 0.3 to 0.7 V, so that it is 1.5×10^{-8} W at V_{DD} = 0.7 V. Fig. 1*H* shows the present HCIN dynamic performance where V_{IN} is a square input of 0.7 V (logic state of "1") and a low voltage input of 0.0 V (logic state of "0") over the frequency range of 0.1~8 Hz. V_{OUT} shows typical inverter characteristics with "0" or "1" V_{OUT} obtained with "1" or "0" V_{IN}, respectively. Moreover, stable rail-to-rail V_{OUT} swings between 0 V and 0.7 V is obtained at a V_{IN} frequency of ~8 Hz. A stage delay of 0.025 s is achieved by measuring the time between the input falling edge and the point where V_{OUT} = 95% V_{DD}. Such a stage delay is relatively slow compared to ion-gel-gated EGTs but is above the average (0.9 s) reported for EGT inverters with aqueous electrolytes (15, 28).

Real-Time EOG Monitoring and Logic Gates Using HCINs. The high voltage gain of the HCIN developed here should be ideal for wearable/skin-compatible electrophysiological single amplification and monitoring, since these signals are weak in nature (millivolt range) (57). Here we apply the HCIN for real-time monitoring of EOG signals (Fig. 2 and *SI Appendix*, Fig. S8*A*).

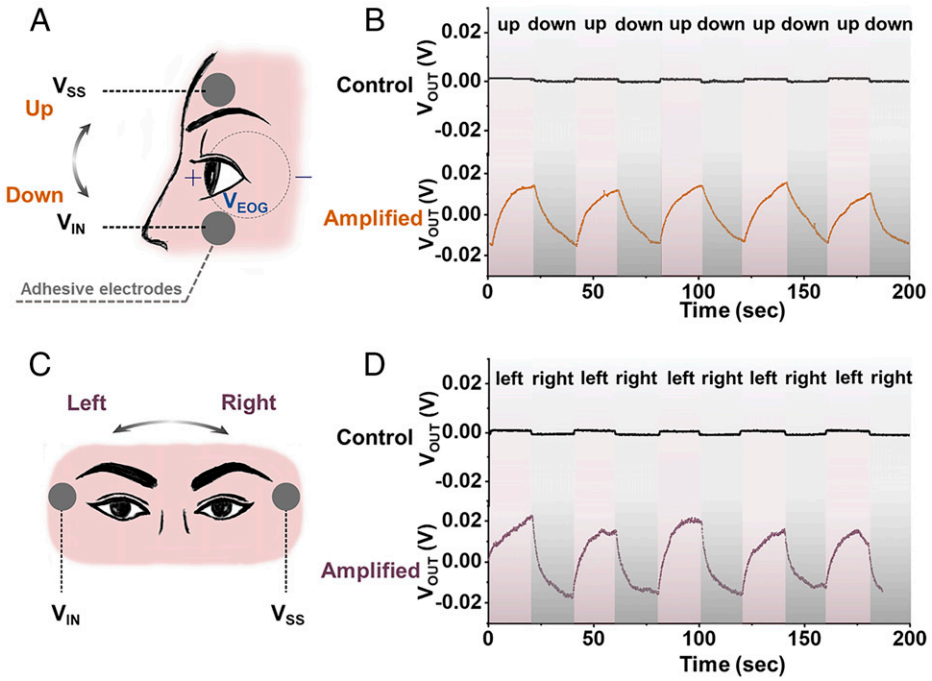

Fig. 2. EOG signals monitored by hybrid complementary circuits. Operating principle of the hybrid circuit in EOG signals monitoring during (*A*) up–down and (*C*) left–right eye movements. EOG signals obtained from the control group and the hybrid circuits during (*B*) up–down and (*D*) left–right eye movements.

As an example, EOG signal is of great significance for virtual and augmented reality, as well as medical research, such as the monitoring of reading speed, drowsiness detection, and diagnosis of sleep disorders (58, 59). Various current monitoring methods achieve cost-effective wearable sensing and high signal amplification metrics (60). However, these techniques require complex circuitry and/or specialized instrumentation for processing the recorded EOG signals (61, 62). In contrast, our HCIN can measure and amplify EOG signals simultaneously, which is advantageous in terms of directness of evaluation, fabrication simplicity, and low cost.

The EOG signal originates from the potential difference between the cornea and retina (V_{EOG}), where eye movement leads to potential variations along vertical or horizontal directions of the eye on the nearby skin with up/down or left/right eye movement (Fig. 2) (63, 64). By placing two 3M-2560 electrodes on the top and bottom sides of the eye, V_{EOG} is directly measured and exhibits small voltage fluctuations (1~1.5 mV) with up and down eye movement (Fig. 2*B*). However, by connecting one electrode to V_{IN} and the other to V_{SS} (*SI Appendix*, Fig. S8*B*), the HCIN V_{OUT} exhibits voltage variations as large as 30 mV (Fig. 2*B*). Note that V_{DD} and V_{SS} are properly adjusted to ensure V_{SW} is ~0 V (see *Materials and Methods* for details). Moreover, horizontal eye movement is also tracked, showing less than a 1.5-mV variation by direct voltage measurement (Fig. 2*D*). However, an amplified voltage variation of up to ~40 mV is achieved by the HCIN in monitoring horizontal eye movement (Fig. 2*D* and *SI Appendix*, Fig. S8*C*). The proposed hybrid circuit exhibits satisfactory performance in tracking eye movement, which demonstrates the signal amplification capacity of the HCIN and its potential for further applications in wearable integration systems for health monitoring.

Based on the high HCIN performance, we next explored the integration of complementary NAND and NOR gates; the circuit diagrams and circuit photographs are shown in Fig. 3. From the voltage input–output characteristics of the NAND gate in *SI Appendix*, Fig. S9*A*, V_{OUT} remains at a high voltage (logic "1"), as long as V_{IN} A and/or V_{IN} B are at low voltage state (logic "0"), while V_{OUT} switches to logic "0" only when both of the inputs are at logic "1." *SI Appendix*, Fig. S9*B* shows the dynamic output of a NOR gate with V_{DD} = 0.7 V, in which V_{OUT} switches to logic "1" only when both of the inputs are at logic "0." These logic gates exhibit correct V_{OUT} with a rail-to-rail behavior corresponding to their V_{IN}, which then suggests the possibility of operating the logic gates at lower driving voltages. Fig. 3 *C* and *D* illustrate the dynamic performance of both NAND and NOR logic circuits with V_{DD} from 0.5 to 0.2 V. Typical rail-to-rail behavior of outputs are obtained even for driving voltage as low as 0.2 V, which is attributable to the well-balanced transistor performance, especially near 0 V V_{ON} in both EGTs. This is among the lowest reported driving voltage of EGT-based logic circuits and is comparable to technologically mature Si technologies

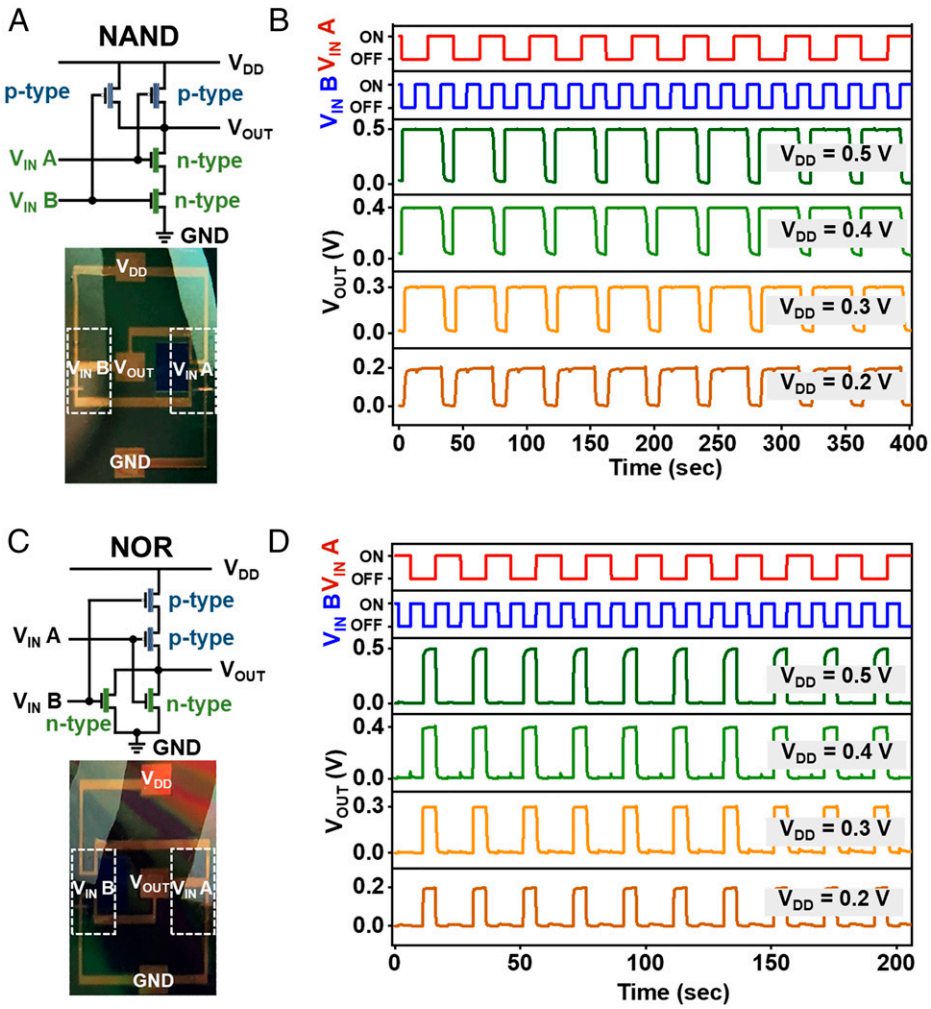

Fig. 3. Logic gates based on hybrid complementary circuits. Circuit diagrams and corresponding images of the (*A*) NAND and (*C*) NOR logic gates. Voltage input–output characteristics of the (*B*) NAND and (*D*) NOR logic gates, with V_{DD} = 0.2, 0.3, 0.4, and 0.5 V, respectively.

(15, 28, 65). Low driving voltages are essential for electronics where the power source is limited, indicating that the hybrid complementary circuit holds great potential for next-generation applications including bioelectronics, wearable/portable electronics, and artificial intelligence.

Flexible Hybrid Complementary Circuits. Since HCIN fabrication is compatible with flexible substrates (66, 67), and considering the need for mechanical flexibility in bioelectronics and wearable/portable electronics (19), complementary circuits are constructed here on flexible polyimide (PI) substrates (Fig. 4*A*; details in *SI Appendix*). First, the DPP-g2T OECT and IGZO EDLT on PI transistor performances were individually assessed (*SI Appendix*, Fig. S10) and indicated performances similar to these EGTs on Si/SiO_2 substrates. The transfer curve of the porous DPP-g2T OECT (L = 10 μm; W = 100 μm) (*SI Appendix*, Fig. S10) shows an I_{on}/I_{off} of 10^4 and V_{ON} of ∼0.0 V, with $g_{m,p}$ = 1.7 ± 0.5 mS, while the IGZO EDLT (L = 10 μm; W = 300 μm) (*SI Appendix*, Fig. S10*B*) exhibits an I_{on}/I_{off} of 10^5 and V_{ON} of ∼ −0.3 V, with $g_{m,p}$ = 0.6 ± 0.3 mS. The corresponding HCIN performance on PI (*SI Appendix*, Fig. S11) demonstrates good voltage transfer properties for V_{DD} from 0.3 V to 0.7 V. Moreover, a voltage gain of 95 is achieved at 0.7 V, slightly lower than 113 on a rigid substrate. The static power consumption is 3.3×10^{-9} W with V_{DD} = 0.3 V and increases to 2×10^{-8} W with V_{DD} = 0.7 V.

For flexible electronics applications, circuit electrical metrics should remain stable under mechanical deformation. Thus, a single EGT and HCIN electrical response was next investigated on bending about radii (R) from ∞ (no bending stress) to 1 mm (stress ∼1.3% for EGT active layers) both parallel and perpendicular to the channel length direction as flexible electronics. As shown in Fig. 4 *B* and *C*, representative transfer curves for DPP-g2T OECTs and IGZO EDLTs on different degrees of bending along the direction parallel to the channel length indicate that transistor performance is extremely stable after bending down to 1 mm. For example, V_{ON} of the DPP-g2T OECT and IGZO EDLT shift slightly from −0.03 to −0.02 V and from −0.15 to −0.18 V, respectively. The OECT I_{on} (from 3.2×10^{-5} to 1.1×10^{-5} A) and I_{off} (from 8.5×10^{-9} to 1.1×10^{-8} A) exhibit negligible variations. Similarly, the IGZO EDLT I_{on} and I_{off} after bending deteriorate minimally from 1.17×10^{-4} to 1.14×10^{-4} A and from 2.4×10^{-9} to 1.2×10^{-9} A, respectively. Similar stable transistor behaviors are also obtained on bending along the direction perpendicular to the channel length (*SI Appendix*, Fig. S12). Specifically, the DPP-g2T OECT exhibits stable operation performance on bending (*SI Appendix*, Fig. S12*A*), while slightly positive shifted IGZO EDLT transfer curves are evident for bending radii smaller than 1.5 mm, where V_{ON} shifts from −0.14 to −0.04 V and I_{on} and I_{off} decrease substantially from 1.5×10^{-4} to 5.0×10^{-5} A and from 1.0×10^{-9} to 4.5×10^{-9} A, respectively (*SI Appendix*, Fig. S12*B*). Nevertheless, the IGZO EDLT remains functional

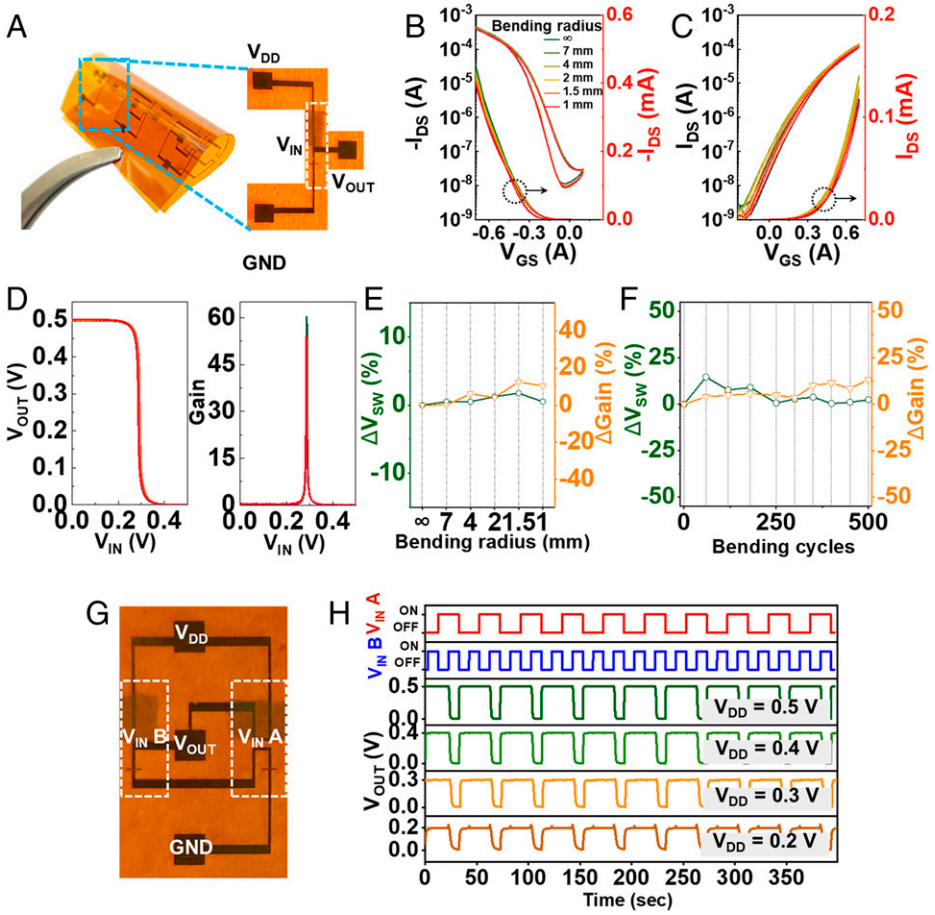

Fig. 4. Mechanically flexible hybrid complementary circuits. (*A*) Photo of the flexible hybrid circuits, along with a zoomed-in part of the inverter. Transfer curves of the flexible (*B*) DPP-g2T OECT and (*C*) IGZO EDLT when bended at the indicated radius (from 7 mm to 1 mm) along the direction perpendicular to channel length. (*D*) Corresponding voltage transfer characteristics and voltage gain of the flexible complementary inverter after bended under the indicated radius (from 7 mm to 1 mm). Switch voltage (V_{SW}) and voltage gain variation of flexible hybrid inverter (*E*) after different bending radius and (*F*) after multiple bending cycles (bending radius = 4 mm) along the direction perpendicular to channel length. (*G*) Photo of the NAND gate on PI substrate, along with (*H*) the dynamic performance of the NAND logic gate with V_{DD} from 0.2 V to 0.5 V.

after bending to a 1-mm radius along the direction perpendicular to the channel length. Thus, the above transistor performances after bending indicate that circuits based on such transistors should also show stable performance down to ∼1.5-mm radii. As shown in Fig. 4*D* and *SI Appendix*, Fig. S12*C*, HCIN voltage transfer curves after bending to different radii exhibit identical characteristics, where the voltage gains only fall from 60 to 54 and from 50 to 43, after bending from ∞ to 1 mm in the parallel and perpendicular direction, respectively (V_{DD} = 0.5 V). Variations of V_{SW} and voltage gain (gain) of the circuit (normalized value) as a function of bending radius are summarized in Fig. 4*E* and *SI Appendix*, Fig. S13*A*. No significant changes are observed on bending in both directions, with the V_{SW} and voltage gains of hybrid circuit varying only ∼0.5% and ∼10%, respectively, after bending to a 1-mm radius (Fig. 4*E*). For the bending direction perpendicular to channel length, ∼2.8% and ∼13.9% variations in V_{SW} and voltage gain are observed after bending at R of 1 mm (*SI Appendix*, Fig. S13*A*).

Performance stability of the flexible HCIN was further investigated by bending the device in both directions at R = 4 mm (stress ∼0.3%) for 500 cycles, and the variation of V_{SW} and voltage gain were recorded (Fig. 4*F* and *SI Appendix*, Fig. S13*B*). V_{SW} and voltage gain variations are within ∼2.4% and 13.1%, respectively, in the bending direction parallel to channel length, while ∼9.3% and 3.6% variations on V_{SW} and voltage gain, respectively, are observed in the bending direction perpendicular to the channel length. The present HCIN shows satisfactory stability on flexible substrates under dynamic bending stresses, as a result of the amorphous nature of the IGZO (*SI Appendix*, Fig. S14) and SU-8 encapsulated Au electrodes, preventing them from cracking under bending (*SI Appendix*, Fig. S15) (68). Finally, mechanically flexible NAND and NOR logic gates were demonstrated on PI (Fig. 4*G* and *SI Appendix*, Fig. S16*A*). The corresponding dynamic performances are shown in Fig. 4*H* and *SI Appendix*, Fig. S16*B*. Both NAND and NOR logic gates exhibit full rail-to-rail behavior, where good logic responses to two square-wave input signals (V_{IN} A and V_{IN} B) are obtained with a power supply as low as 0.2 V. These results further illustrate the potential of implementing the hybrid OECT/IGZO EGT configuration in flexible integrated circuits and wearable sensing electronics.

Conclusions

Here we demonstrated an approach to achieving high-performance complementary circuits by integrating an organic p-type OECT and an inorganic n-type IGZO EDLT. Balanced transistor performances thereby afford an inverter with ultrahigh voltage gain (∼113) under a low operating voltage of 0.7 V. Diverse logic circuits on both rigid and flexible substrates are fabricated, demonstrating stable performance output under ultralow driving voltages (0.2 V), and utility is demonstrated in the high-sensitivity monitoring and amplification EOG signals, which is critical for the development of useful diagnostic tool for human health and wearable human–computer interfaces. These results demonstrate considerable potential for the further development of hybrid porous organic OECT/nonporous inorganic EDLT circuits in low-power flexible electronics and wearable sensors.

Materials and Methods

Precursor Preparation. All chemicals were purchased from Sigma-Aldrich; 354.8 mg $In(NO_3)_3{\cdot}xH_2O$, 399.6 mg $Ga(NO_3)_3{\cdot}xH_2O$, and 297.2 mg $Zn(NO_3)_2{\cdot}xH_2O$ were dissolved in 10 mL deionized (DI) water to achieve a concentration of 0.1 M. Then, the well-dispersed precursor solutions were mixed to obtain the IGZO precursor solutions with the desired In:Ga:Zn molar ratio of 7:1:2, 8:1:1, 9:1:1, and 10:1:1, followed by continuous stirring for 8 h. DPP-g2T was synthesized following the procedure described in *SI Appendix*, Scheme S1 and Fig. S1. DPP-g2T (8 mg) was dissolved in 1 mL solvent mixture of chloroform:methyl alcohol = 9:1 in volume, and the prepared DPP-g2T solution was stirred for at least 12 h before use.

Device Fabrication and Evaluation. n^{++}-silicon wafers with 300 nm SiO_2 coating or 25-μm PI films as substrates were first ultrasonically cleaned in isopropyl alcohol and then treated with an oxygen plasma for 15 min. Next, the IGZO precursor solution was filtered through a 0.2-μm polytetrafluoroethylene syringe filter and spin-coated on the Si/SiO_2 substrate at 3,000 rpm for 20 s and annealed at 300 °C for 30 min. This spin-coating and annealing process was repeated for three times on Si/SiO_2 substrate or seven times on the PI substrate. Then, patterning of the IGZO layer was achieved by spin coating on S1813 photoresist at 4,000 rpm for 45 s, followed by annealing at 110 °C for 60 s and then exposing in a maskless aligner system (MLA150; Heidelberg Instruments). Next, the sample was developed in AZ400k (Microchemicals) for 40 s, cleaned with DI water, and dried by an N_2 flow. The exposed oxide film was then etched in an aqueous oxalic acid solution (10% wt/vol) for 40 s and rinsed with DI water. Residual S1813 photoresist was removed by sonicating the sample in acetone and then isopropyl alcohol for 2 min each. The obtained patterned IGZO was further annealed at 300 °C for 5 min to remove residual solvent. The Au/Cr electrodes were next patterned with S1813 in a lift-off process, where S1813 was first patterned with the same process as described above but with a different pattern. Then, 3 nm Cr and 30 nm Au were deposited by thermal evaporation and developed by soaking in acetone for 5 min to remove the S1813. Here, the patterned Au electrodes define the channel dimensions, which for the IGZO EDLT were W = 300 μm and L = 10 μm, while those for the DPP-g2T OECT were W = 100 μm and L = 10 μm. Next, the device was encapsulated by spin coating SU-8 (2002) at 3,000 rpm for 30 s, followed by exposing to a mask aligner (Suss MABA6) for 15 s through a photo mask. After developing the SU-8 developer, only the channel areas for both transistors were exposed to air. The porous DPP-g2T films were first deposited on polyvinyl alcohol (PVA; ∼30 nm thick)–coated glass by spin coating the prepared DPP-g2T solution at 5,000 rpm for 10 s in a high-humidity atmosphere (relative humidity = ∼94%). Next, the free-standing porous DPP-g2T film was obtained by immersing the DPP-g2T/PVA/glass multilayer in water, and the detached DPP-g2T was transferred to the p channel area of the circuit electrodes. Finally, the device was annealed at 110 °C for 5 min before applying the 0.1 M KPF_6 aqueous electrolyte and Ag/AgCl as gate electrode.

Electrical characterization of the transistors and circuits was performed with an Agilent 1500 semiconductor parameter analyzer on a probe station. For the logic circuit measurements, pulse input signals were generated by a waveform generator (Keysight 33500B).

Thin Film Characterization. For the IGZO film characterization, GIXRD measurements were carried out with a Rigaku Smart Lab Thin-film Diffraction Workstation using a high-intensity 9-kW copper rotating anode X-ray source which is coupled to a multilayer optic. The scanning electron microscope (SEM) characterization of the porous DPP-g2T films was carried out on a Hitachi SU8030 FE-SEM.

EOG Monitoring. For the EOG monitoring of up–down eye motion (*SI Appendix*, Fig. S8*A*), a 26-y-old healthy female participated in the experiments and all testing procedures were conducted safely without any external stimulus. Before the experiments, the human subject was trained on the experimental protocol which including vertical and horizontal eyeball movements and was also instructed not to speak to avoid any interference from other body movements. During the testing, two adhesive electrodes (3M Red Dot 2560-5) were placed on the upper and lower sides of the eye socket, respectively. The upper one was connected to the V_{SS} of the proposed inverter, and the lower one was directly connected to the V_{IN}. The V_{DD} and V_{SS} were supplied by an Agilent 1500 semiconductor parameter analyzer and properly adjusted to make sure that V_{SW} was ∼0 V. Next, in a relaxed state, the human subject followed instructions to look up and down (*SI Appendix*, Fig. S8*B*). First, the subject was asked to look horizontally, then asked to move the eyeballs up and then down. This procedure was repeated during the measurements. The amplified EOG signal was recorded by monitoring V_{OUT} using a Bio-Logic SP-150. The left–right eye movement tracking was similar to the above operation (*SI Appendix*, Fig. S8*C*), except that the two adhesive electrodes were placed on the left and right temples, and the human subject was asked to move the eyeballs in the horizontal direction to the left and next to the right directions. The left electrode was connected to V_{SS}, and the right one was connected to V_{IN}. This procedure was repeated during the measurements. The EOG experiment involving human subjects described in this research was assigned as "Not Human Research" by the Institutional Review Board at the Northwestern University. A subject consent was signed before participating in the research, and the authors are very grateful to the participant for involvement in this study.

Data Availability. All study data are included in the article and/or *SI Appendix*.

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