


Communication

# A New Cell Topology for 4H-SiC Planar Power MOSFETs for High-Frequency Switching

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**Abstract:** A new cell topology named the dodecagonal (a polygon with twelve sides, short for Dod) cell is proposed to optimize the gate-to-drain capacitance ( $C_{gd}$ ) and reduce the specific ON-resistance ( $R_{on,sp}$ ) of 4H-SiC planar power MOSFETs. The Dod and the octagonal (Oct) cells are used in the layout design of the 650 V SiC MOSFETs in this work. The experimental results confirm that the Dod-cell MOSFET achieves a  $2.2\times$  lower  $R_{on,sp}$ ,  $2.1\times$  smaller high-frequency figure of merit (HF-FOM), higher turn on/off  $dv/dt$ , and 29% less switching loss than the fabricated Oct-cell MOSFET. The results demonstrate that the Dod cell is an attractive candidate for high-frequency power applications.

**Keywords:** SiC power MOSFET; cell topology; dodecagonal cell; octagonal cell; gate-to-drain capacitance ( $C_{gd}$ ); specific ON-resistance ( $R_{on,sp}$ ); high-frequency figure of merit (HF-FOM); switching performance



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## 1. Introduction

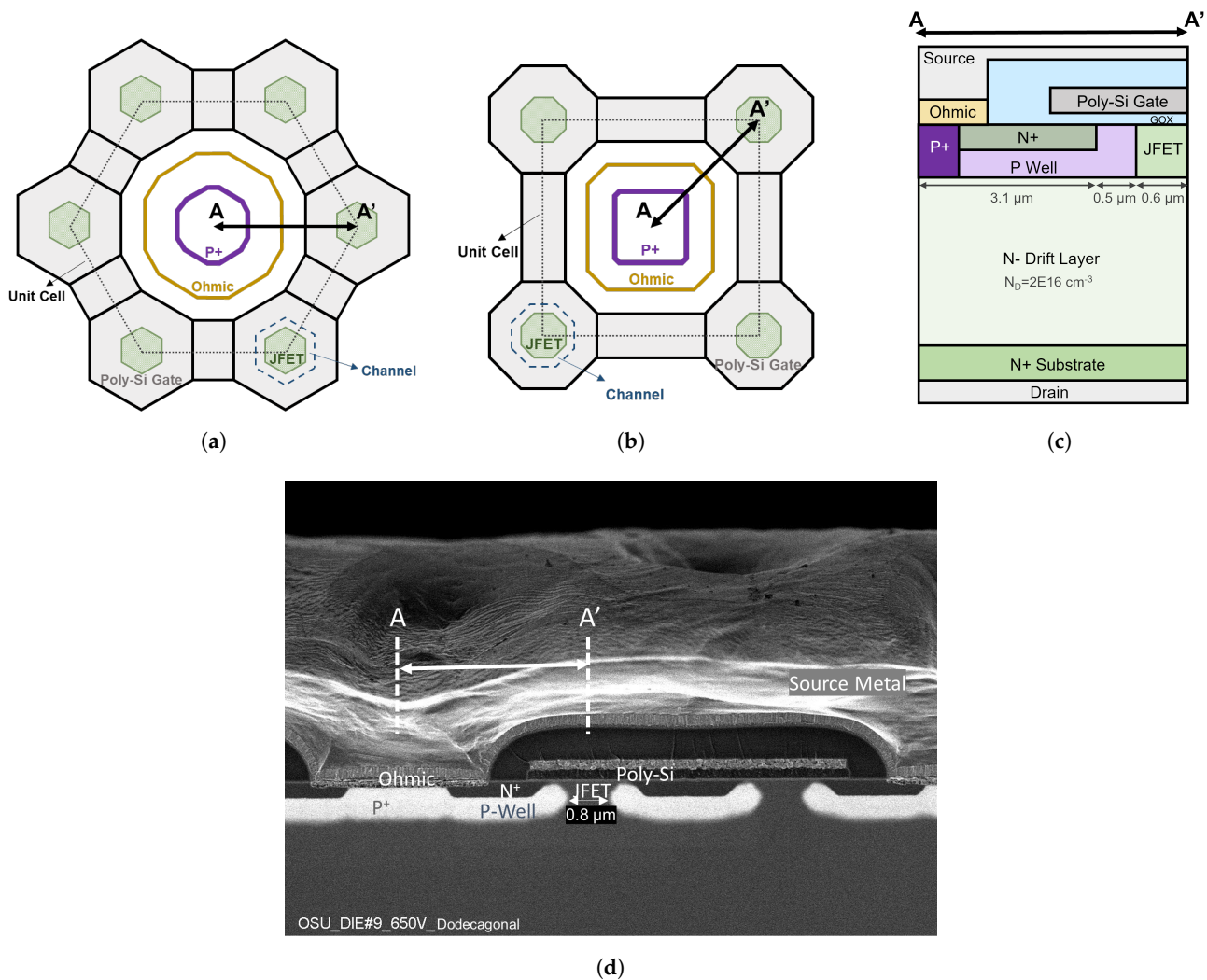
The silicon carbide (SiC) power MOSFET has been expected to be the alternative to silicon power devices in multiple applications, such as renewable energy, drivers for electrical machines, and power converters for hybrid and electric vehicles, due to its various advantages, including a low power loss, high switching frequency, and high operating temperature [1–3]. Improving energy efficiency (reducing power dissipation) is the driving force for the commercialization of SiC power MOSFETs [3]. The total power loss of a SiC power MOSFET consists of an on-state conduction loss and switching loss. The conduction loss can be reduced by reducing the ON-resistance ( $R_{on}$ ). The switching loss of a SiC power MOSFET can be reduced by decreasing device capacitances [4,5]. Studies show that the layout topology design affects the on-state and dynamic performances of SiC power devices [6,7]. Different cell topologies (Linear, Hexagonal, Square, and Octagonal) were used on 600 V SiC planar MOSFETs [7]. All the figure of merits (FOMs) for the Octagonal cell topology are comparable to those of the state-of-the-art Si COOLMOS and are much better than the ROHM SiC MOSFET product [7]. In addition, simulations show that the oxide electric field for an Octagonal cell is much lower in comparison to other topologies [7]. The Linear, Hexagonal, and Octagonal cell topologies were used on 650 V SiC planar JBSFETs and reported in [8]. It is demonstrated that the Hexagonal cell topology provides the lowest specific ON-resistance ( $R_{on,sp}$ ) but a higher gate–drain charge than Linear and Octagonal cells [8]. It indicates that the Hexagonal cell is suitable for power-switching applications at a nominal frequency. However, for applications where a faster switching frequency is desired, such as reducing the size of power converters, the layout, such as the Octagonal (Oct) cell, is preferred, which tends to reduce the  $C_{gd}$  at the cost of a higher  $R_{on}$  [9].

In this work, a new cell topology named the dodecagonal (Dod) cell is proposed and compared with the Oct cell. Additionally, 650 V SiC power MOSFETs with the Dod

and Oct cells have been designed, fabricated, and characterized. The static and dynamic performances of the fabricated 650 V SiC power MOSFETs are compared.

## 2. Device Design and Fabrication

Figure 1a shows the structure of the proposed Dod cell. A twelve-sided P<sup>+</sup> region with the ohmic contact on top is surrounded by six hexagonal poly-Si gate regions. The hexagonal gate regions are connected by poly-Si bars. The hexagonal JFET regions are placed inside gate regions. This Dod cell is applied to 650 V SiC power MOSFETs. The Oct cell is shown in Figure 1b. The cross-sectional views along the AA' direction for both Dod-cell and Oct-cell MOSFETs in this work are shown in Figure 1c. All MOSFETs have the same edge termination design and die size. The die size is 1.15 × 1.15 mm<sup>2</sup>, including the termination. The MOSFETs are fabricated on a 6-inch SiC wafer by X-Fab using the same SiC power MOSFET process. Figure 1d shows the cross-sectional SEM image of the fabricated Dod-cell MOSFETs. Due to the lateral straggle of Aluminum implantation in the P-well, the narrowest portion of the JFET region is reduced by 0.2 μm on each side. Five Dod-cell and five Oct-cell MOSFETs are packaged into open-cavity TO-247 packages for device characterization. Design parameters and experimental results are listed in Table 1.



**Figure 1.** (a) Dodecagonal cell topology, (b) Octagonal cell topology, (c) A-A' cross-sectional view of the 650 V SiC power MOSFET. (d) Cross-sectional SEM image of the fabricated 650 V SiC power MOSFET with the Dod cell.

**Table 1.** Design parameters and experimental results.

	Cell Topology	Oct	Dod
Design parameters	Cell pitch ( $\mu\text{m}$ )	8.4	8.4
	Active area ( $\text{mm}^2$ )	0.643	0.634
	Channel density ( $\mu\text{m}^{-1}$ )	0.113	0.181
	JFET density	0.034	0.055
Experimental results	$V_{\text{th}}$ (V)	$4.09 \pm 0.09$ *	$4.35 \pm 0.10$
	BV (V) @ $I_{\text{D}} = 100 \mu\text{A}$	$756.3 \pm 22.6$	$753.4 \pm 23.6$
	$R_{\text{on,sp}}$ ( $\text{m}\Omega \cdot \text{cm}^2$ ) @ $V_{\text{D}} = 1.5 \text{ V}$	$24.4 \pm 7.52$	$10.9 \pm 3.06$
	$C_{\text{gd}}$ (pF) @ $V_{\text{D}} = 400 \text{ V}$	$1.59 \pm 0.01$	$1.63 \pm 0.04$
	HF-FOM ( $\text{m}\Omega \cdot \text{pF}$ ) ( $R_{\text{on}} \cdot C_{\text{gd}}$ )	$6031 \pm 1896$	$2817 \pm 749$
	dv/dt turn-on (V/ns)	6.1	12.5
	Switching loss turn-on ( $\mu\text{J}$ )	29.4	20.1
	dv/dt turn-off (V/ns)	8.4	10.7
	Switching loss turn-off ( $\mu\text{J}$ )	5.7	4.7
	Total switching loss ( $\mu\text{J}$ )	35.1	24.8

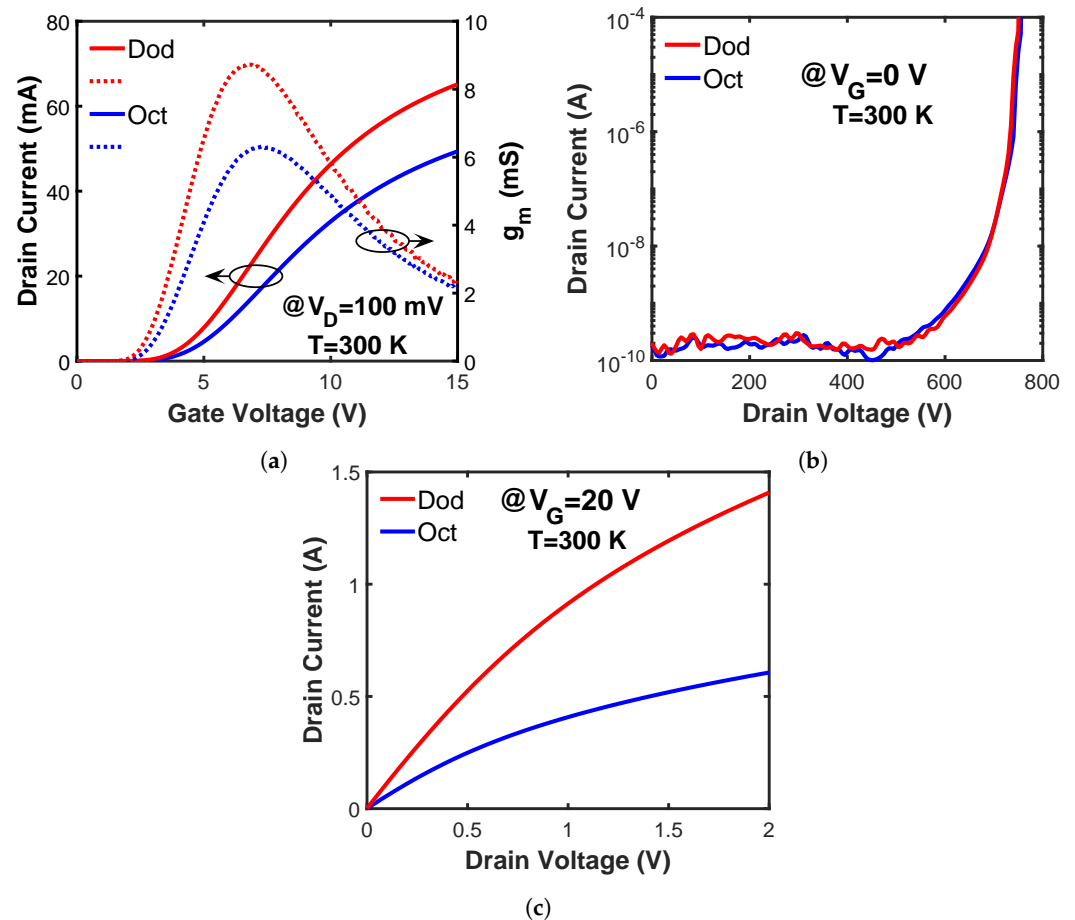
\*  $\pm$  refers to the standard deviation of the value.

### 3. Experimental Results and Discussion

#### 3.1. Statistic Performance

The static performance, including the transfer, blocking, and output characteristics, is measured using a Keysight 1506A power semiconductor analyzer at room temperature. The results of one MOSFET from each cell type are shown in Figure 2. The threshold voltages ( $V_{\text{th}}$ ) of all packaged MOSFETs are extracted using the linear extrapolation method from the transfer curves, as shown in Figure 2a. The average value and the standard derivation are shown in Table 1. A minimal  $V_{\text{th}}$  difference ( $<0.3 \text{ V}$ ) is observed between the MOSFETs with Dod and Oct cells. The transconductances ( $g_{\text{m}}$ ) are also plotted in Figure 2a. The peak  $g_{\text{m}}$  value for the Dod-cell MOSFET is  $1.5\times$  higher than the fabricated Oct-cell MOSFET, indicating a higher current-driving capability. The blocking characteristics (Figure 2b) show less than  $1 \text{ nA}$  leakage current up to  $600 \text{ V}$  for both the Dod-cell and Oct-cell MOSFETs. The breakdown voltage (BV) is defined at the drain current of  $100 \mu\text{A}$ . Similar average BVs and BV standard derivations are obtained for the Oct-cell and Dod-cell MOSFETs, as shown in Table 1. Therefore, the Dod cell does not degrade the blocking capability of the fabricated power MOSFET.

The output characteristics are shown in Figure 2c. A  $2\times$  higher drain current is observed on the fabricated Dod-cell MOSFET than on the Oct-cell MOSFET, which can be explained by the higher channel density and JFET density of the Dod cell. A higher channel density (total channel width in a unit cell/unit cell area) implies a larger total channel width and more current conduction within a specific die size. The channel densities for the Dod and Oct cells are calculated according to the geometry with the known cross section and cell pitch. The results are listed in Table 1. A  $1.6\times$  higher channel density is obtained for the Dod cell than the Oct cell. The higher channel density allows more current conduction for the fabricated Dod-cell MOSFET, resulting in a lower  $R_{\text{on,sp}}$  than the fabricated Oct-cell MOSFET. The higher JFET density (JFET area/unit cell area) indicates a lower JFET region resistance, which contributes to the lower  $R_{\text{on,sp}}$  [10]. The  $R_{\text{on,sp}}$  of all the measured MOSFETs is calculated at a drain–source voltage ( $V_{\text{D}}$ ) of  $1.5 \text{ V}$ . The mean values and standard derivations are listed in Table 1. A  $2.2\times$  reduction in the  $R_{\text{on,sp}}$  is achieved for the Dod-cell MOSFET compared to the fabricated Oct-cell MOSFET.



**Figure 2.** (a) Transfer characteristics at  $V_D = 100$  mV (solid line: drain current vs. gate voltage; dash line: transconductance vs. gate voltage), (b) blocking characteristics at  $V_G = 0$  V, and (c) output characteristics at  $V_G = 20$  V, for the 650 V SiC power MOSFETs with Dod and Oct cells.

### 3.2. Dynamic Performance

The  $C_{gd}$  vs. drain voltage characteristics are shown in Figure 3. The  $C_{gd}$  significantly affects the dynamic behavior of SiC MOSFETs due to the well-known Miller effect [11,12]. The  $C_{gd}$  of a SiC planar MOSFET consists of the gate oxide capacitance on the top of the JFET region and the depletion capacitance of the JFET region and drift layer [13]. The results in Figure 3 show that the Dod-cell MOSFET has a higher  $C_{gd}$  than the fabricated Oct-cell MOSFET under any drain bias. Because the Dod-cell and Oct-cell MOSFETs are fabricated following the same process flow, their gate oxide thickness, JFET doping profile, and drift-layer doping profile are the same. Thus, the difference in the  $C_{gd}$  is caused by the different overlap areas of the gate and drain terminals (JFET region area) within a die. The calculated JFET density of the Dod cell is  $1.6 \times$  higher than the Oct cell, which causes a higher  $C_{gd}$  of the Dod-cell MOSFET. The  $C_{gd}$  values at  $V_D = 400$  V are extracted for all the measured MOSFETs. Additionally, the HF-FOMs, which are defined as the product of  $R_{on}$  and  $C_{gd}$ , are calculated. The HF-FOM of the Dod-cell MOSFET is  $2.1 \times$  smaller than the fabricated Oct-cell MOSFET, indicating a better high-frequency performance.

A Double-Pulse Test (DPT), which provides straightforward data on the switching behavior of SiC MOSFETs [14], is conducted to investigate the switching performance of the fabricated MOSFETs. The results are shown in Figure 4. During the turn-on process (Figure 4a), the Dod-cell MOSFET shows a shorter transient time (higher turn-on speed) than the fabricated Oct-cell MOSFET. The turn-on and turn-off  $dv/dt$ , switching energy, and total switching energy of the measured MOSFETs are extracted and listed in Table 1. The Dod-cell MOSFET has a higher  $dv/dt$  and less switching energy than the measured

Oct-cell MOSFET during both the turn-on and turn-off processes. The Dod-cell MOSFET obtains a 29% reduction in total switching loss compared to the measured Oct-cell MOSFET.

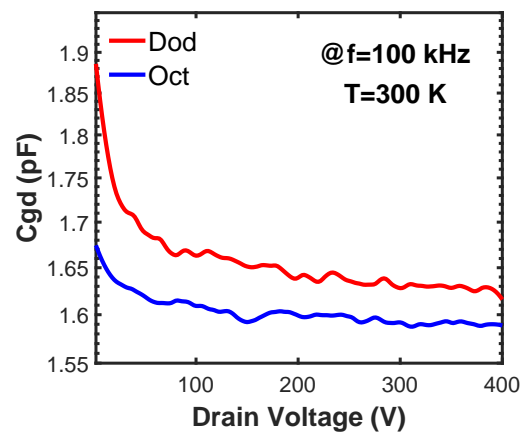


Figure 3. The  $C_{gd}$  of 650 V SiC MOSFETs with the Dod and the Oct cells.

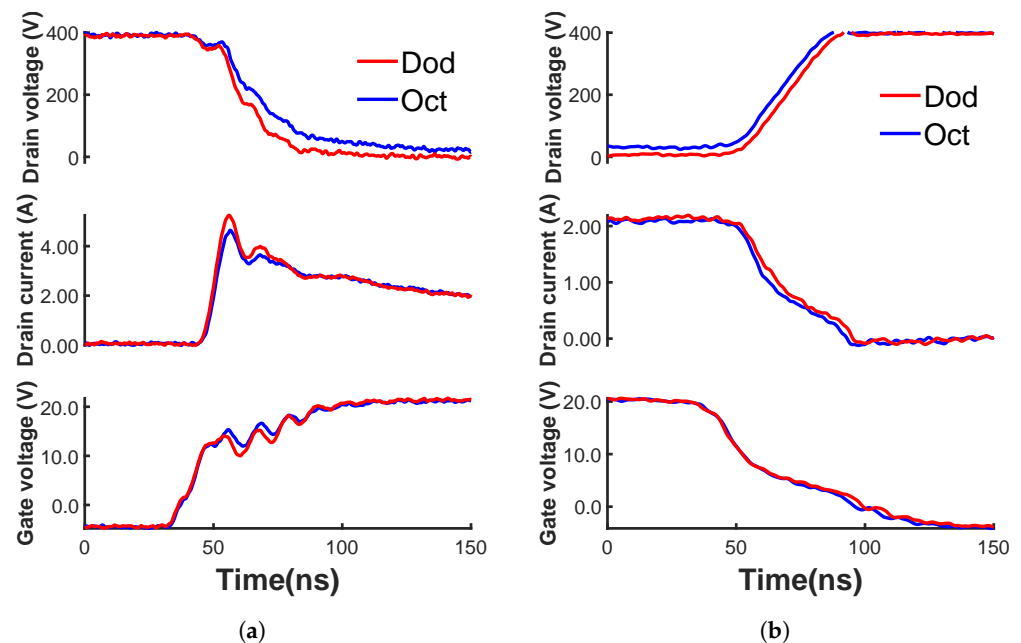


Figure 4. (a) Turn-on and (b) turn-off waveforms of the fabricated 650 V SiC power MOSFETs with the Dod and the Oct cells.

#### 4. Conclusions

A new cell topology named the Dod cell is proposed for SiC planar power MOSFETs. The Dod cell minimizes the JFET region area to achieve a low  $C_{gd}$  and improves the channel density to reduce the  $R_{on,sp}$ . A low  $C_{gd}$  indicates a higher switching speed and makes the Dod-cell MOSFET an attractive candidate for high-frequency applications. The reduced  $R_{on,sp}$  decreases the conduction loss. The Dod cell and a recently published Oct cell (designed with minimal JFET region area) have been used for the layout design of 650 V SiC power MOSFETs. The fabricated Dod-cell MOSFET achieves a higher  $C_{gd}$ , but a  $2.2\times$  lower  $R_{on,sp}$ ,  $2.1\times$  smaller HF-FOM, and 29% less switching losses compared with the fabricated Oct-cell MOSFET.

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## Abbreviations

The following abbreviations are used in this manuscript:

SiC	Silicon Carbide
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
JFET	Junction Field-Effect Transistor
JBSFET	Junction Barrier Schottky (JBS) diode-integrated MOSFET
HF-FOM	High-Frequency Figure of Merit
DPT	Double-Pulse Test

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